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A Transient Enhanced Capacitor-less Low dropout Regulator Using 180nm CMOS technology

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Abstract— Demand for system on-chip (SoC) designs and portable electronics has risen quickly in recent years. The dual loop architecture serves as the foundation for the capacitorless LDO described in this research. In order to overcome the difficulties in establishing stability, including quick transient performance and minimal voltage spikes under rapid loadcurrent fluctuations, the regulator uses two feedback loops. The suggested design runs with a 0-100 pF capacitive load and does not require a decoupling capacitor to be placed at the output. A 0.18 µm CMOS technology is used for performing the simulations on the design. The Capacitor-less LDO is given an input voltage of 1.0 - 1.4V, and it gives an output of 0.9 V. Line and Load Regulation obtained are 0.821 mV/V and 0.1122 mA/V respectively. The Capacitor-less LDO has a phase margin of 87.55^o , making it more stable whereas phase margin of Conventional LDO is just 43.78^o . The transient response of Capacitor less LDO is enhanced succesfully. The overshoot and undershoot of the Capacitorless LDO are 16.38 mV and 16.9 mV respectively while the conventional LDO shows 27 mV and 33.6 mV respectively. Settling time of Capacitor-less LDO is 1.54 µs, which is much better than settling time of conventional LDO, which is 8 µs

Keywords- PMIC, Low dropout, Transient response, Stability

I. INTRODUCTION

System-on-chip (SoC) design solutions that are comprehensive are being pushed by the industry [1].When a powerful power management system is in place then chip size needs to be reduced [2]. An integral component of an power management integrated circuit (PMIC) is a low dropout regulator (LDO) . The huge off-chip capacitor used in a typical LDO is being replaced in a number of studies to ensure stability and the right transient response [7]. The battery life may be increased and the utilisation of portable devices may rise with better power management. When different supply voltages are employed for on-chip power management, low drop-out (LDO) voltage regulators play a crucial role. A circuit that produces a well-defined, steady dc voltage with a small input to output voltage differential is known as a low dropout regulator. In portable devices like mobile phones, PDAs, and laptops, Low Dropout Regulators are frequently employed. The manufacturing of an off-chip capacitor takes up too much space on an IC, which prevents it from being used in traditional LDOs to preserve stability and eliminate overshoot and undershoot in transient response. Designing an LDO circuit that can accomplish self-stabilization and quick transient response without the requirement for an output capacitor has been a common technique for today's LDO designs, since capacitor-less LDOs assist to minimize chip size and cost [11]. In this work, the simulation results of both the conventional and capacitor-free LDOs are compared.

II. CONVENTIONAL LDO

Figure 1 shows the usual LDO structure. A conventional LDO consists of a large output capacitor with equivalent series resistance (ESR) [1], a pass element, an error amplifier, a band gap reference, a feedback network, and other components. The band gap reference, feedback network, pass element, and error amplifier are all located on the same chip. It needs a second pin to connect to the massive output capacitor with ESR because it is off-chip.

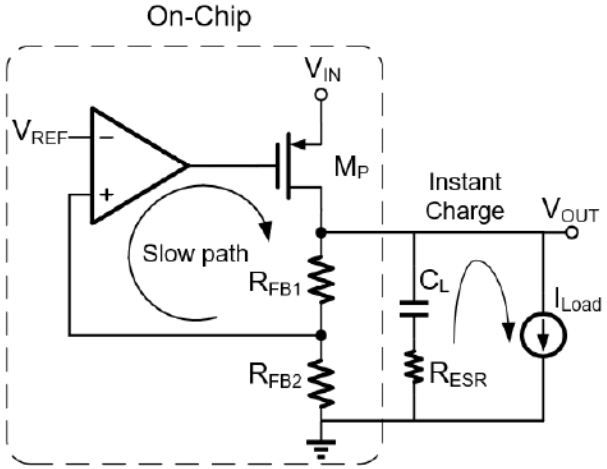

Fig. 1. Block Diagram of Conventional LDO

A high gain op-amp called the error amplifier compares the output voltage, which has been scaled down by the feedback resistors, with the band gap reference value.

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A. Stability Analysis

Because of the left half plane (LHP) zero that the output capacitor's ESR introduces, the typical LDO design may achieve high stability. Figure 2 illustrates how, under the assumption that the ESR is properly chosen to ensure the system has a reasonable phase margin, which is often bigger than 60^o , The second pole, P2, will no longer have any effect due to the LHP zero. According to equation 1, the dominant pole ωp1 shifts significantly when the load varies, leading to varied bandwidth under various load situations. This is because the dominant pole is negatively correlated with the output load resistor stated in the equation 2.

$$H = \frac{A_{ol}(1+\omega_z)}{(1+\omega_{p1})(1+\omega_{p2})} \quad (1)$$

$$\omega_{p1} \frac{1}{R_o C_o} \quad (2)$$

This typical LDO also has the benefit of having a fairly strong transient response as there is a substantial off-chip capacitor. The fast transient response is one of the important performance metric of a regulator [3].The large capacitor provides a direct current channel into the load prior to changing the gate of the pass element due to the rapid load transient. The quick path connects the output capacitor to the load, whereas the slow path travels from the error amplifier and feedback network to the pass element.

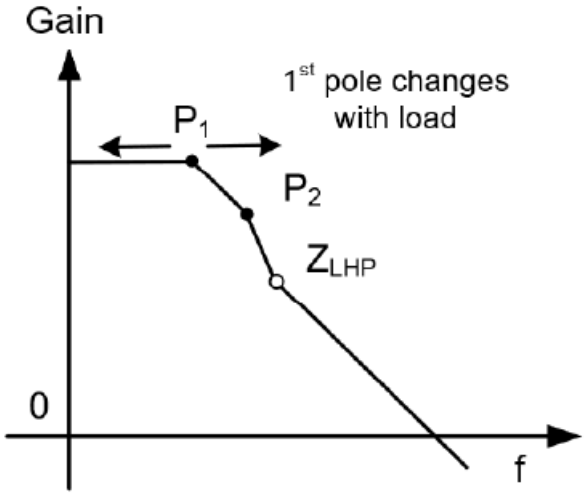

Fig. 2. Frequency response of the conventional LDO.

Utilizing a large off-chip capacitor will help the traditional LDO's stability and also with transient responsiveness [10]. However, the enormous off-chip capacitor takes up a lot of space and the chip's external pin requires a lot of space on the printed circuit board (PCB).

III. PROPOSED CAPACITOR-LESS LDO

By adding more feedback loops, an LDO's stability can be improved [5]. Two regulation loops similar to [4] with an improved performance are presented in this paper. The difference between the proposed design and the one in [4] lies in the implementation of 2-stage Opamp. The 2 stage opamp used in our design is fully compensated with improved Slew Rate and Bandwidth. This LDO circuit employs a PMOS pass transistor configured as a common source (CS) amplifier. There is a second stage that uses a differential amplifier. The regulator shows an output voltage of 900 mV and is powered by a voltage of 1.2 V. I_L, the load current, ranges with in 250 to 500 µA and 1 ns rise time and fall time. The load up to 100 pF is represented by the capacitance C_L.

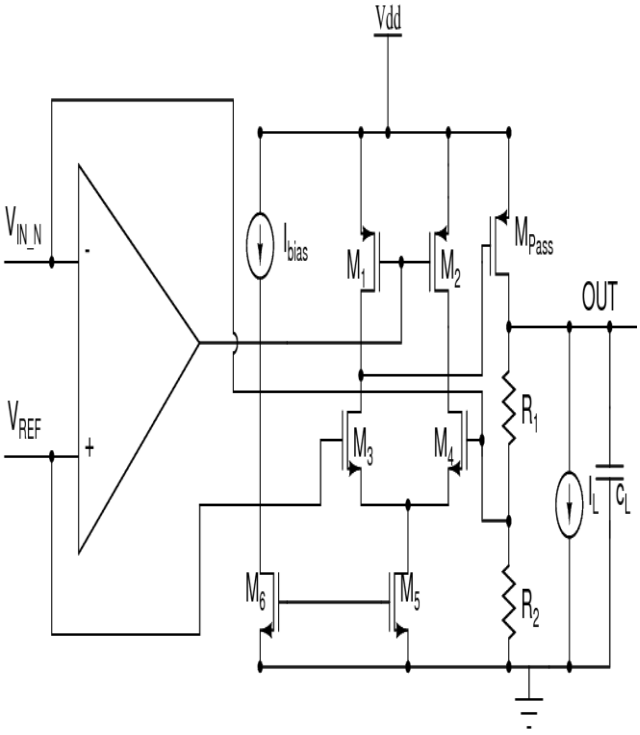

Fig. 3. Proposed Capacitor-Less LDO

A. Fast loop

The Fast loop regulates the gate of the Pass transistor. The fast loop gain is regulated by the differential stage and the common source stage.

The frequency response is dominated by the gate capacitance and the transconductance. The gate voltage of M4 is set using the resistors R_1 and R_2 to maintain the transistor in saturation region. The values of the feedback resistance network are R_1 = 300 kΩ and R_2 = 600 kΩ.

With the loop response having small phase margin, ringing may be seen on the regulator's output during the application of current step loads. Therefore, at maximum predicted load capacitance, most preferable way is to maintain a phase margin for fast loop over 75^o [4].

B. Slow loop

The slow loop's job is to maintain the DC level at Vout by controlling the gate voltages of transistors M1 and M2. A fully compensated two-stage operational amplifier (OpAmp) is used for slow loop. Reduced quiescent current consumption in the slow loop translates into low power usage [6].

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A big Miller capacitor to lower the dominant pole's frequency without affecting the second pole is used. To avoid slewing during the transient, the OpAmp is designed carefully so as to drive the gates of transistors M1 and M2.

IV. IMPLEMENTATION

A. *Conventional LDO*

Figure 4 depicts the transistor-level design of the traditional LDO. The schematic shown was designed, and the chosen dimensions of the transistors present in the schematic are shown in table I.

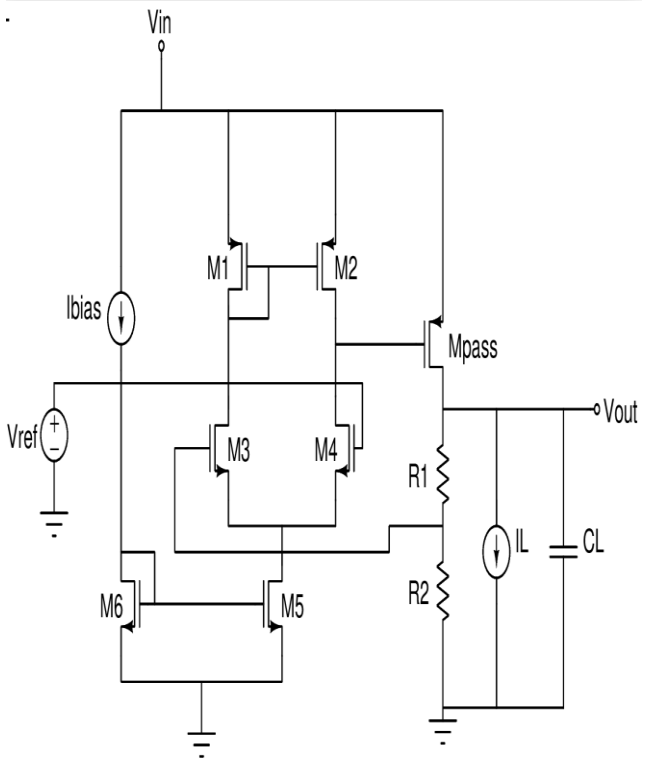

Fig. 4. Transistor level diagram of Conventional LDO

TABLE I. DIMENSIONS OF THE TRANSISTOR IN CONVENTIONAL LDO

Transistor	*W (µm)*	*L(µm)*
M1	84	1
M_2	84	1
M_3	10	1
M_4	10	1
M_5	9	1
M_6	9	1
M_{pass}	399.95	1

B. *Capacitor-less LDO*

Figure 3 depicts the circuit of proposed capacitor-less LDO. . The schematic shown in Figure 3 was designed, and Simulated in Cadence Virtuoso 180nm technology.

V. SIMULATION RESULTS

The Conventional LDO shown in Figure 4 was simulated using Cadence Virtuoso 180nm CMOS technology. The Conventional LDO is able to operate at a Supply of 1.8V. Figure 5 shows the Load transient response of the Conventional LDO. It is observed that the Overshoot Voltage is 27mV and Undershoot Voltage is 33.6mV with a settling time of 8µs.

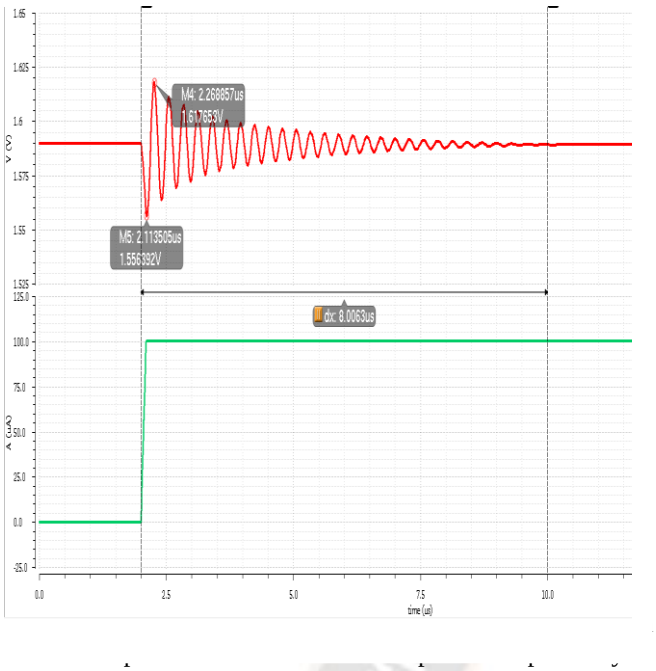

Fig. 5. Load Transient Response of Conventional LDO

The Gain and phase plot of the loop gain in the presence of load capacitor is shown in Figure 6. The following results are obtained:

- Phase margin = 43.78º
- Unity gain frequency = 55.19 KHz

The Gain and phase plot of the loop gain without load capacitor is shown in Figure 7. The following results are obtained:

- Phase margin = 1º
- Unity gain frequency = 2 MHz

The simulation results of the conventional LDO show that the transient response is very poor. The only method to improve this is by increasing the load capacitance. But we cannot increase it beyond a certain value due to size constraint of a large capacitor. It is also seen that even in presence of the load capacitor, the phase margin is a mere 43.78º , which guarantees stability, but

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is not sufficient. Hence compensation techniques are needed. The Capacitor less LDO shown in Figure 3 was

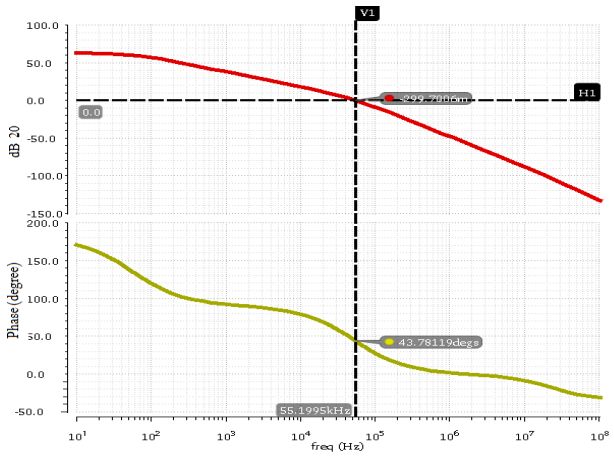

Fig. 6. Gain and Phase Response of Conventional LDO with Capacitor

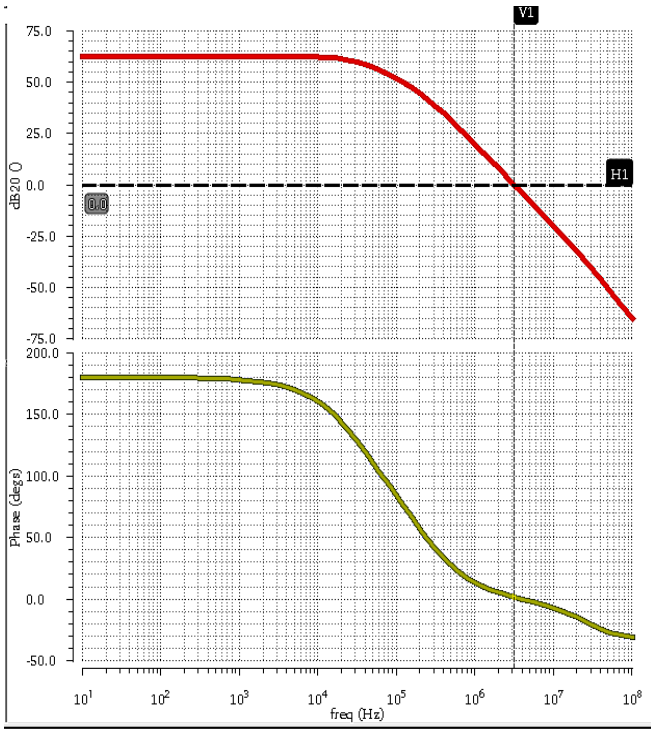

Fig. 7. Gain and Phase Response of Conventional LDO without Capacitor

simulated using Cadence Virtuoso 180nm CMOS technology. Input voltage of 1.0 - 1.4 V was used. The circuit operates with a load current of 250 - 500 µA and with a load capacitance of 100pF.

A. Line Regulation

The input voltage is varied from 0V to 3.5V, with load current kept constant and output voltage is evaluated. The output waveform can be seen in Figure 8.

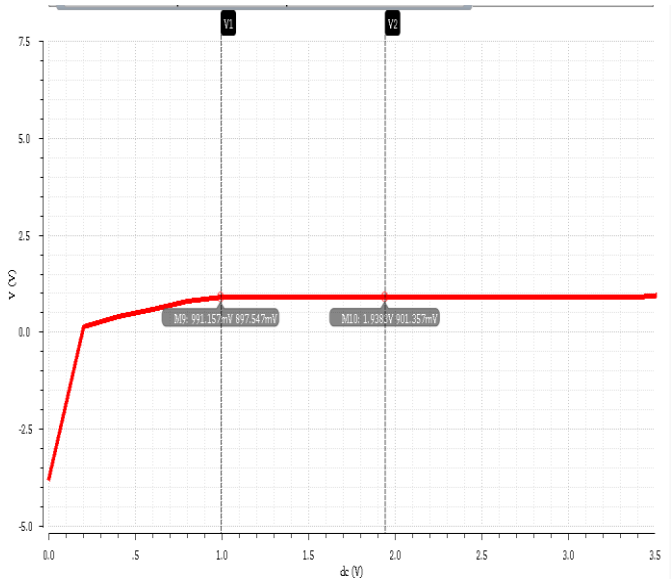

Fig. 8. Line regulation of capacitor-less LDO

As seen in Figure 8, regulation starts when input is 1.0V and a constant output of 0.9V is obtained. Hence dropout voltage is 100mV. Line regulation is 0.821 mV/V

B. Load Transient

The load current is a pulse of 500µA. The load capacitance has a fixed value of 100pF. The output voltage shown in Figure 9 shows an undershoot and an overshoot before reaching its steady state value. Parameters obtained are:

- Overshoot = 16.38 mV, Settling time = 2.12 µs
- Undershoot = 16.9 mV, Settling time = 1.54 µs

Fig. 9. Load Transient Response of Capacitor Less LDO

C. Stability Analysis

The Bode plot of the loop gain transfer function gives a summary of the stability of the system. The feedback loop is broken at a point, and a probe is attached at this point to evaluate the Bode plot. Figure 10 displays the Bode Magnitude and Bode

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Phase plots of the loop gain in the presence of load capacitor. The following results are obtained from the Bode Plot:

- Phase margin = 87.55°
- Unity gain frequency = 292.6 KHz

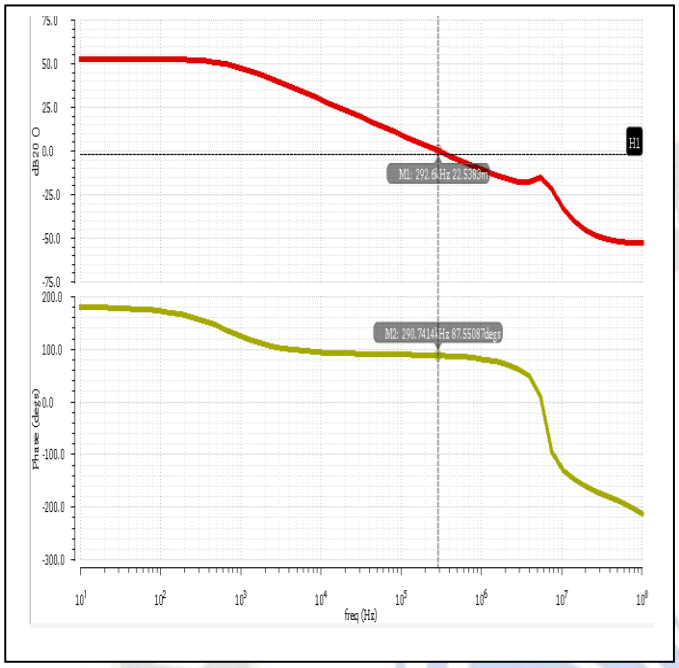

Fig. 10. Gain and Phase Response of Capacitor Less LDO

VI. COMPARISON OF RESULTS

Table II shows the Comparison of results obtained for Conventional LDO and Capacitor less LDO. It is seen that the transient response showed much improvement in the CL-LDO. The undershoot and overshoot lie within 2% error band of the output voltage. Capacitor-less LDO operates at a smaller input, and has a lower dropout as well. Even though both the LDOs used the same load capacitor, phase margin of Capacitor-less LDO is better than phase margin of the Conventional LDO, thus ensuring stability while simultaneously getting rid of the ringing effect.

VII. CONCLUSION

This work has presented an alternative method to ensure a good transient response while getting rid of the large external capacitor. This was done by introducing an additional feedback loop consisting of a differential amplifier to provide dominant pole compensation and improve stability. The comparison of this work with similar research works is shown in table III. As seen from table III, this paper shows an improved overshoot and undershoot as compared to other works reported. The dropout voltage obtained in this paper is same as dropout in [4] and [6]. The settling time presented in this paper is better than all papers except [5], which can be improved in future works.

TABLE II. COMPARISON OF RESULTS

Parameter	Conventional LDO	Capacitor-less LDO
Error Amplifier used	1-stage differential amplifier	2-stage op-amp
I_{load} (μA)	10 - 100	250 - 500
C_{load} (pF)	100	100
V_{in} (V)	1.8 - 2.0	1.0 - 1.4
V_{out} (V)	1.6	0.9
$V_{dropout}$ (mV)	200	100
Line Regulation (mV/V)	0.406	0.821
Load Regulation (mA/V)	2.73	0.1122
Overshoot (mV)	27	16.38
Undershoot (mV)	33.6	16.9
Settling time (μs)	8	1.54
Phase Margin (°)	With load cap: 43.78 Without load cap: 1	87.55
UGF (KHz)	With load cap: 55.19 Without load cap: 2000	292.6

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COMPARISON WITH RESEARCH PAPERS

	Units	[9]	[8]	[5]	[7]	[6]	[4]	This work
Technology	[µm]	0.35	0.09	0.11	0.18	0.5	0.18	0.18
Vin	[V]	0.95 - 1.4	0.75 - 1.2	1.82 - 3.8	1.4 - 1.8	2.3 -5.5	1.0 - 1.4	1.0 - 1.4
Vout	[V]	0.7 - 1.2	0.5 - 1	1.2	1.2	1.2 - 5.4	0.9	0.9
Vdropout	[mV]	200	200	200	200	100	100	100
Undershoot	[mV]	70	73	385	110	96	26	16.9
Overshoot	[mV]	70	114	200	85	120	26	16.38
Settling time	[µs]	3	5	0.65	30	3	3.5	1.54
Cout	[pF]	100	50	40	100	470	100	100