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Round Robin based Arbitration Mechanism for Signaling Approach based Router Architecture

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Abstract— In Network-on-Chip the effectiveness of the network resource allocation is demonstrated by the flow control mechanism. There are two types of flow control mechanisms: buffered and bufferless. Compared to buffered flow control methods, buffer less flow control mechanisms are easier to use, need less power, and take up less space. When there are congestion and resource conflicts, it experiences higher packet loss and packet misrouting inside the network. A good buffered control mechanism useful as it overcomes the limitations of buffer less mechanism. There are numerous buffered and bufferless flow control methods available. In this paper, signaling-based Virtual Output Queue Router Arbiter Mechanism is used to explore credit-based flow control. This mechanism worked on new concept that is "stress value". This information is generated in the form of credit whenever any input buffer has free space. Then, using this credit data, the node's stress value is determined. Free buffer space takes precedence over stress value if it is bigger. The stress value will increase if there is less available buffer space. To handle the congestion problem, the signaling block then sends this stress value to a neighboring router. To help the arbitrator make a more accurate decision, the crediting system constantly operates in tandem with arbitration.

Keywords- NoC, SoC, VoQ, Router,Stress value, Signaling block.

I. INTRODUCTION

It is common practice to raise a chip operational frequency in order to boost computing performance in SoCs. It forces the designers to consider different methods for improving performance without doubling power consumption. The NoC design separates computing and communication via a network of connected packet-based devices. It permits buffer size, bandwidth, and topology customization, in contrast to the shared bus. It is possible to achieve scalability without the need for lengthy physical cables. The NoC infrastructure, which is used to distribute packets using layered protocols, is made up of routers and cables [1]. A router establishes a connection between each NoC node and a processing element (PE) and memory unit. If there is a router fault, the linked healthy core will not be reachable.

Virtual channels are logical channels that have been created by subdividing a physical channel into numerous logical channels [4]. When many packets demanded for the same network path, then it generates congestion. Virtual channel is one of method to give the solution to control such types of congestion problem. Before the invention of the Virtual Queue buffer mechanism, FIFO buffer system was used to store the packets inside router. The needs of buffer system inside the network are for proper routing of packets and avoid loss of packets because in network packets are inserted like Poisson distribution methods [5]. A system where the packet is temporarily stored before being forwarded to its target node is called a buffer. FIFO is very simple method where a continuous memory block is assigned for data storing. Entering and exiting of data happens as first in first out queue fashion. This method needs very less memory requirement. So, space requirement for the router is very less. But, this method has very poor performance. It does not support for removing the head of blocking problem which is a major disadvantages of FIFO buffering mechanism. So, a new buffering method is invented known as Virtual Channel buffer. Instead of keeping

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all packets in a single queue buffer, a multiple buffer system has been created. The memory space is distributed into a multiple buffer. So, packet has another alternate choice to store. Virtual Channel gives better results as compared to FIFO buffer method. For the small-scale application, single VC is sufficient for holding the packets data. But, when the large or big data application is needed to run on SoC, the single VC mechanism does not provide the desirable results. So, modification in VC system is been done in last few years. Number of Virtual Channel is gradually increasing in router for the fast computing applications requirements. We have developed Virtual output queue based router architecture. In this router architecture, four virtual channels per port are preferred. Therefore, the supporting mechanism mainly arbitration mechanism also needs to be changed. If there are four VC, then allocation of four VC is again a complicated task. The job of VC allocation is done under the guidance of arbitration mechanism. The VC allocation for the incoming packets is done by the arbiter on the priority basis. Since the VC provides an exceeding performance for packets load handling, so, the implementation cost of arbitration mechanism becomes affordable. The depth of the VC is fixed for router. Generally, the depth of the Virtual Channel is equal to length of flit size.

VC is again separated into three primary categories: Virtual Channel of Input side of router, Virtual Channel of output side of the buffer, and Virtual Channel of Input Output side of router. In Input VC, virtual channel is available in input side of the router whereas in output VC, virtual channel is present at output side. The combination of input and output buffering system is called the input output VC buffering mechanism. Actually, VC buffering has a solution for avoiding the head of the blocking problem but it cannot avoid the deadlock problems for packets. Input VC is easy to design and its speed of operation is as good as compared to output VC. But, still there is a limitation because of its non-supporting behavior for deadlock avoidance. Input Output VC method has both features but is not easy to design and it requires more space inside router. Space is also a major factor when designing the NoC architecture. If space requirements are more, its power requirements for network also increase. From this discussion it can say that it is a major need to focus on dead lock and congestion parameters while considering the improvement of QoS. Both these parameters play a very crucial role while designing NoC. Deadlock avoidance is a one of favorable method for QoS improvements. Suppose, the NoC is deadlock free, then it can be concluded that it supports QoS. On the basis of detailed study of all the VC buffering system, Output port VC buffering system is finalized for the current NoC framework. The research work uses a virtual output queue buffer technology. To prevent deadlocks, separate queues will be kept for each output port at each input side. For this reason, it is referred to as a Virtual output Queue (VoQ) buffer. VoQ architecture, where each Output port has its own dedicated VC on the input side. In this study, the deadlock problems are eliminated using a signaling block and buffering system combination.

The remaining sections of this paper are: Part II of the overview of relevant studies. Section III offers a thorough discussion of the router architecture based on the Virtual Output Queue mechanism. Described in Section IV is the Router Arbitrator Mechanism. The Round Robin Arbitration functioning details are presented in Section V and our conclusion is made at the end of this paper.

II. AN OVERVIEW OF RELATED RESEARCH

In the field of multi core SoC and NoC, congestion is a widely studied issue. The management of congestion is seen as an effective measure to prevent networks from reaching saturation as well as it helps in the overall improvement of the throughput in NoC. Network performance is strongly impacted by congestion, which is a serious problem in networks. The primary switch arbiter is the Scheduler. Arbiters are the fundamental building blocks of systems with shared resources, and a tightly integrated architecture for its input requests is a centralized arbiter. It is suggested in [3] to employ a new centralized arbitrator for the arbitration of a crossbar switch in NoC routers. They create an Islip arbiter for NoC by combining a mesh router and the Islip scheduling method. As manufacturing technology advances, smaller feature sizes enable a greater integration of system components onto a single die. Communication between these components can become the performance bottleneck if the right scheduling strategy is not used. A simple machine learning method that gathers information about the traffic at each destination and labels it using a revolutionary time reversal method in order to predict network congestion. A low overhead, comprehensible decision tree model is created using the labeled data for runtime congestion control [2].

The most popular ways adopted for the indication of the existence of network congestion are Buffer and link status [6][7][8]. In this case, a congestion-aware routing algorithm that may be used specifically will help ensure that the traffic burden on the network is distributed fairly. Based on the knowledge of the buffer load, a favorable path for incoming packets is chosen when using a self-optimized routing technique [7].The proximity congestion awareness method, which helps people avoid congested areas, is also advised by the study [9]. This is carried out based on the stress values provided by surrounding switches. These techniques are based on the approach taken to try to direct packets away from network hotspots.

For the same goals, the contention-aware input selection algorithm developed by [10] prioritizes incoming packets from

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congested places to help relieve congestion in upstream areas. Based on making appropriate throttling decisions, the study by [11] is an application-aware congestion management method that can be employed in on-chip buffer less networks. Another study by [12] suggests a minimal NoC router architecture that is congested-aware. This method, which is based on dynamic port arbitration, aids in the alleviation of congestion. It also features adaptive output path selection, which makes it easier to distribute the traffic load uniformly and effectively. The aforementioned approaches might be viewed as a means of easing the NoC's congestion.

III. IMPLEMENTED ROUTER ARCHITECTURE

The router is the NoC system's most vital and significant component. In a network, traffic is routed from sources to destinations by the router. It coordinates the data flow in order to make that possible, which is regarded as a highly important stage in communication networks. As a result, it is appropriately regarded as the foundation of communication within a NoC system. Given the significance of a router, it should be built to have the highest efficiency and throughput possible. The following are the essential elements of a router's architecture:

1. One port for input
2. One port for output
3. A switching matrix: The input and output ports are connected by the usage of a switching matrix.
4. A local port that makes it easier for the router to connect to the right IP core

Since these routers gather incoming data packets, evaluate their destinations, and select the optimal path for the data to take from source to destination, they can be thought of as intelligent devices. The critical path delay is mostly determined by a router's architectural design, which also influences per hop delay and network latency. Because of the limited space and power requirements, the router's architectural design must be carefully developed to fit the required latency and throughput requirements. Consequently, the deterministic element in evaluating the network's total performance is the router design efficiency. The router architecture proposed in this technique will be built on the router function, input controller, switch, and switch Allocator phases.

Input ports, Output ports , Crossbar units and Arbitration units are only a few of the parts that make up the implemented router. The control logic employs routing logic to check whether the nearby router has any buffers available to store the packets before switching them.

The router routes the packets inside the network using Dynamic XY routing algorithm. The Rund-Robin arbitration technique is used to send packets from the output port, which is directly connected to the arbitrator.

Through a signaling method, each port informs an arbiter of the output queues it has access to. After that, each port creates a new input queue for every possible output queue that was mentioned in the earlier stage. When a frame needs to be transported across ports in a network, the input port puts it in a virtual output queue. The output port then requests that the input port send the frame over the crossbar. The arbiter receives the request from the input port, prepares the output queue, selects a buffer from among the available output queues, and sends the frame. The output port notifies the arbitrator that the outlet queue is now open after transferring the frame.

TABLE:1 IMPLEMENTED ROUTER ARCHITECTURE COMPONENTS

S.N	Components	Specification
1.	Used Topology	2D
2.	Finalized Algorithm	Dy XY
3.	Selected packet switching method	Wormhole
4.	Fixed Buffer size	32 bits
5.	Flit Length	32 bits
6.	Total Packet Length	16 flits

A detailed description of the router architecture is shown in Table 1. Five ports (Input & Output), an arbitration block, a routing block, and a signaling block make up the internal design, which is seen in Figure 1. The flits arriving from the ports are categorized by the arbitration block. The production of signaling packets is the signaling block's primary purpose. This flit information can be used to update the neighboring router's current status, which includes whether or not free space is available. Signaling flits, which inform the neighbors of the router's current state, are produced by the signaling block. This block also collects neighbor router states and saves them in an internal database that is refreshed each time a signaling flit occurs. The network's path construction procedure relies on these preserved states to handle header flits. Lastly, during the data flit routing, this block collaborates with the routing block. The primary structural element of the router is the routing block. This guarantees the routing methods.

Our approach makes use of the Virtual Output Queue (VOQ) wormhole switch architecture, which lowers average packet delay while using less power and space than the conventional Virtual Channel (VC) switch architecture. Every VOQ has a designated input port that it is paired to an output port. The FLITs from competing VOQs for the same output port are moved via a Round-Robin process to the following hop. The FLIT is already stored in VOQ (i,j) and ready to be broadcast to output channel j when it reaches input port i. When a VOQ with FLIT arrives and presents demands, the switch allocation unit (SA) assigns each output channel. If required, a FLIT will be sent to the output port.

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It is now possible to construct signaling blocks with this router design. To update the statuses of neighboring routers with the changed traffic load conditions, it generates and broadcasts signaling information from asynchronous flits. The primary responsibilities of this block are updating internal routing table data with neighboring router statuses and processing recently received signaling flits. Decisions about routing are made using the data in this routing database.

This block checks the status of virtual output queues to gather congestion data from nearby ports. There is no congestion if there is space in the buffer for sorting packets; otherwise, there is congestion. The Signaling block receives information about the current status of all neighbor blocks. As a result, this Signaling block contains information about every nearby router. This is necessary to control a head-flit while creating a path. Signaling block gathers information about available buffer space from all of its nearby routers and creates a signaling flit.

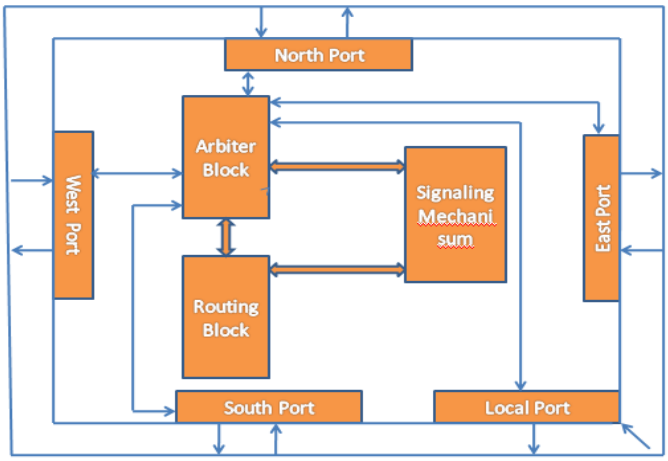

Figure 1. Signaling Block implementation inside Router architecture

This flit is nothing more than the router status of a neighbor. Every time a single block communicates with the routing block before data flit routing inside network. Arbiter and routing blocks were attached to this signaling block. This data is subsequently transmitted to Routing block. The routing block then chose a new path for the packets to travel. It always chooses the free path when there is no traffic.

IV. ROUTER ARBITER MECHANISM

The incoming packet must be sent by the Router arbitrator to the desired output port. There is a conflict when several requests are sent at once to the same device or channel. Arbitration is used to settle this dispute. This research work for arbitration has a round robin descending order clockwise direction mechanism. The arbiter can simultaneously gather requests for packets from the five nodes. This research's architecture, arbitration method, signaling block, and routing block all operate simultaneously. Arbiter block's input and output ports are all fully connected. When packets enter inside the buffer, the signaling block is informed of this information. Additionally, the signaling block physically routes this information to every neighboring router. Since the signaling path is bidirectional, the same path is also used to gather data on the status of nearby buffers. While setting up the routing path, the routing block always verifies the signaling block's state. After that, it gives the arbitration mechanism control.

The output port's 'READY' signal is constantly checked for status before packets are transferred to the next node. Only one packet is switched to another node if it is ready. Through this approach, the likelihood of network congestion is eliminated. The 'CONNECT' signal is generated and set to high when the arbiter actually sends packets from one node to another node. No other channel is attempting to make contact with the same node. Therefore, the arbitrator's job is done when they find the packet's TAIL flit. When the arbiter receives the last TAIL flit, the "CONNECT" signal is sent. Therefore, a request for the same port could come from another input port.

Different research projects have used different arbitration processes like priority-based, round-robin, first-come-first-served, and priority-based round-robin and many more. In general, Priority based and Priority based Round Robin is used for guaranteed traffic service, whereas First Come First Serve and Round Robin are used for best effort data flow services. In this research work priority-based round robin is used to ensure service. The architecture of the arbitration mechanism is based on a 5x5 multiplexer

V. ROUND ROBIN ARBITRATION WORKING MECHANISM

Each port is granted a priority in a round pattern, either clockwise or counterclockwise, under the round robin arbitration procedure. The request to the arbiter is generated by the required input. The arbitrator uses the algorithm when there are several requests. There is a conflict when several requests are sent at once to the same device or channel. This congestion problem will be resolved by arbitration. The Round Robin descending order clockwise direction arbitration mechanism for router was completed by this research study. Here all generated requests are prioritized from highest to lowest, with the greatest priority being granted first. The round robin system operates depending on time slot allotment. It will determine which ports require the service during a designated time slot. The token passing mechanism is used in this. This token is always moving around. Let's say there is a port with a high request priority, but the output port is not yet ready. This token is always moving around. The token is immediately forwarded to other higher priority nodes that are prepared to distribute the resources. Sharing of resources is assigned in this manner.

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This work by generating the three requests basis:

1. Request Signal: In the first stage, each input port requests the required output port from the arbitrator.

2. Grant Signal: Grant signal generated by arbiter to the requested input port by applying the priority based Round Robin algorithm

3. Accept Signal: Accept is final step through which requested port is obtained the sharing resource parameters.

Information about the allocation of input, output, and resource is kept by Arbiter in a table. 'History' table is the name of this table. When using the routing algorithm, the arbitrator refers to this table and simultaneously modifies the entry according to the allocation of the resources.

TABLE 2. HISTORY TABLE INFORMATION AT INITIAL STATE

Port	North	East	West	South
VC - 1 (LP)	1	1	1	1
VC- 2 (LP)	1	1	1	1
VC - 3 (LP)	1	1	1	1
VC-4 (LP)	1	1	1	1

VC: Virtual channel LP: Local port

The port request is displayed in rows of the history table and the virtual channel request generation is displayed in columns. Assume that all channels are open and accessible to all four ports in the initial state. Values are therefore '1', which denotes the status of the free VC buffer. The request for VC 1 is now generated simultaneously by the four ports. The same VC is required for all four channels. Arbitration uses the Round Robin procedure at this period. The arbiter provides VC to port "W" and changes the information in the history table as shown in Table 3 if port "W" has the highest priority, in accordance with the approach.

TABLE 3. CHANNEL ALLOTMENT RECORDS INSIDE HISTORY TABLE

Port No.	North	East	West	South
Virtual channel 1 (LP)	0	1	0	0
Virtual channel 2 (LP)	0	1	1	1
Virtual channel 3 (LP)	1	1	0	0
Virtual channel 4 (LP)	0	1	1	1

VI. CONCLUSION

Here, we looked into the specifics of an arbitration system based on round robin that prevents congestion while a packet is traveling through a network. Each node has the concept of open buffered space cleared up in advance. Congestion will therefore be automatically eliminated. Each router will receive early knowledge of the available buffer space. Each router has access to congestion information in advance, allowing the routing mechanism to determine the best route before routing packets. The quality of service management technique of the NoC, which is based on a signaling approach mechanism between neighbors' routers, is enhanced by this study. Information exchanges constitute the foundation of the technique being developed to quantify the router state to its neighbors. The road will be aided by this information. The path establishment between communicated processors can benefit from this knowledge. We test the created router architecture and planned protocols using various 2D mesh topology routing algorithms. We discovered stunning outcomes. We can infer from the results that the proposed router implemented arbitration mechanism protocols properly operate and deliver congestion information in advance. Positive outcomes will automatically improve NoC's performance. At a particular level, the QoS level will be updated. According to the findings, the DyXY router technique outperforms alternative topologies in terms of performance and latency. The maximum injection rate of packets (flits/node/cycle) is 1 flit per node each cycle, and the operating frequency is 500 MHz in this case.

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