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Design of Reversible Even and Odd Parity Generator and Checker Using Multifunctional Reversible Logic Gate (MRLG)

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***Abstract*—** Digital data transmission made more efficient of communication. For error free transmission in the digital communication at the source end used parity generator and at destination used parity checker. This paper proposed design of 3 bit reversible Even and Odd parity generator and checker using the multifunctional reversible logic gate (MRLG). The proposed design is designed and simulated using cadence software.

Keywords- *reversible logic, Parity generator, Parity checker, MRLG.*

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I. INTRODUCTION

Moore's law, that has only outperformed itself in the past, states that, the number of the transistor fabricated in an IC doubles in a period of a year and a half, so does the heat generation arising from the increasing chip density. Hence In the past years the incentives of Reversible logic have become increasingly motivating. During the operation conventional gates dissipate heat on losing a bit. In 1973 C.H Bennett [1], a physicist, demonstrated that when a circuit is designed with reversible logic no energy dissipation takes place. A circuit is reversible if one can recover input data from the output data which means the circuit information is lossless. The general considerations of bijectivity is imposed on the design of reversible logic, which means that the circuit design should have equal number of output and input and one to one mapping. This eliminates the loss of information that is main reason for power dissipation. The unused outputs of reversible gate are called Garbage output similarly Redundant Inputs to reversible gate are called Garbage inputs. Complexity and Performance of reversible circuits/ gate are defined by the following parameters

- Number of logic gates
- Number of garbage and constant inputs
- Number of Garbage outputs.
- Fan-out is restricted in reversible logic gate. The fan-out of each gate is equal to one. If more fan out are required then use a copying gate.

In the end of this paper we get a new reversible logic gate so as to produce minimum no. of garbage output, lower quantum cost and minimum delay. In Section II we have outlined the related work in terms of gate size, functionality, number of inputs and outputs and logic description. In Section III we have described the proposed New Multifunctional Reversible Logic Gate (MRLG) with CMOS logic structures. In Section IV and V give the basic idea of the reversible parity generator and checker. In Section VI we have design the circuits of proposed parity generator and checker. The proposed design and MRLG gate has been developed to operate in the voltage range of 1.5 V to 5V with length 180nM and width 2µM transistor with gpdk 180 process. Section VII presents the simulation result and Input output waveform. Conclusion is presented in section VIII.

II. RELATED WORK

Various similar implementation of logic gates have been addressed in [1-14], the classification is defined in terms of its size and functionality. The 1x1 reversible gate is NOT. The 2x2 reversible gate is Feynman. The 3x3 reversible gates are Fredkin, Toffoli, Peres, TR gate, new gate, PRT-1 and PRT-2 and the 4x4 gate includes MKG, TSG and DKG. In Table 1 we have described the logic functionality and a brief description of various gates.

Table 1: Existing Reversible Logic Gates

Reversible Gate (Existing)	Gate Size	Input and output	Logic Description
Feynman 1985 [5]	2x2	Input A, B Output P =A and Q = A ⊕ B	Output Q = A' , when input A=1 Q = Buffer, otherwise
Fredkin 1982 [6]	3x3	Input A, B, C Output P=A, Q=A'B⊕AC and R=A'C'⊕ AB)	Output Q = C and R = B when input A = 1. Otherwise Q = B and R = C'.
Toffoli 1980 [16]	3x3	Input A, B, C Output P=A, Q=B and R=AB⊕ C	R = C' , When A =1 and B = 1 R = Buffer, otherwise
Peres 1985[14]	3x3	Input A, B, C Output P=A, Q= A⊕ B and R=A⊕ BC	Q = B', When A=1 R= C', When A=1 and B=1.
TR 2011 [7]	3x3	Input A, B, C Output P=AQ= A⊕ B, R=AB'⊕ C	R = A NAND B, when B = inverted input
New 2002 [2]	3x3	Input A, B, C Output P=A, Q= AB⊕ C, R=A'C'⊕ B'	R= A' Ex-OR B', When C=0 Else Q= A AND B

PRT-I 2011[15]	3x3	Input A, B, C Output P=AB⊕B'C,Q= A⊕ B⊕ C and R=AB'⊕ BC	Q= B Ex- NOR C, and R= B OR C When A=1. and Q= A Ex-OR B, and R= A AND B, When C=0
PRT-II 2011 [15]	3x3	Input A, B, C Output P=BC⊕AC', Q=A'(B⊕C)+A B and R=C	P= B OR C, When A=1, and Q= A Ex-NOR C, When C= 1
TSG 2005 [8]	4X4	Input A, B, C, D Output P = A, Q = A' C'⊕ B', R = (A'C'⊕ B') ⊕ A and S=(A'C'⊕B') D⊕ (AB⊕ C)	S= A AND B, When C=0 & D= 0
MKG 2007 [11]	4X4	Input A, B, C, D Output P = A, Q= C, R = (A'D'⊕ B') ⊕ C and S = (A'D'⊕ B')C ⊕ (AB⊕D))	R= B Ex-OR C, and S= B AND C When A=0 & D=0 R= B Ex-NOR C, When A=1 & D= 0
DKG 2011 [10]	4X4	Input A, B, C, D Output P = B, Q = A'C + AD', R=(A⊕B)(C⊕D) ⊕ CD and S = B⊕C⊕ D)	Ex-OR when A=0

III. PROPOSED MULTIFUNCTIONAL REVERSIBLE LOGIC GATE (MRLG)

The basic proposed of this Multifunctional Reversible Logic Gate is a reversible logic gate. MRLG have a low power and small delay in design. Fig.1 was the basic approach of this proposed 4X4 reversible MRLG gate. Table 2 shows the MRLG gate truth table. In the truth table of the MRLG input pattern corresponding to a specific output pattern is determined uniquely and to maintain the one-to-one correspondence mapping between the input vector and the output vector.

The MRLG input vector is I_v = (A, B, C, D) and there output vector is O_v = (P = A, Q = AB ⊕ A'C, R = B⊕ AC, S = B⊕ AC ⊕D). Its CMOS realization is shown in fig. 1.

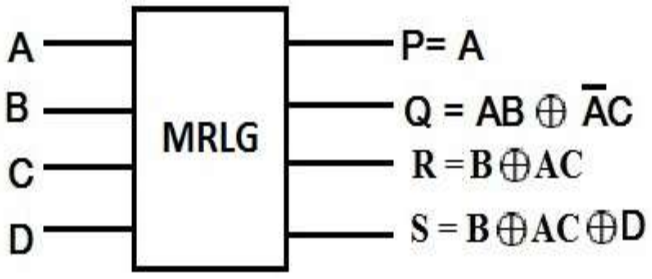

Fig. 1. Proposed MRLG reversible gate.

Table 2: Proposed MRLG gate truth table

Inputs				Outputs			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	1	0	0
0	0	1	1	0	1	0	1
0	1	0	0	0	0	1	1
0	1	0	1	0	0	1	0
0	1	1	0	0	1	1	1
0	1	1	1	0	1	1	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	1
1	0	1	1	1	0	1	0
1	1	0	0	1	1	1	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	0	0
1	1	1	1	1	1	0	1

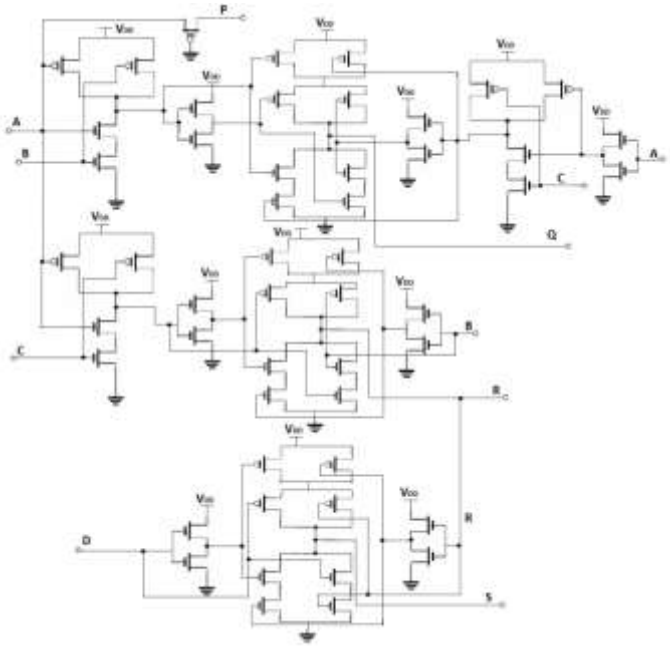

Fig. 2. CMOS realization of MRLG gate

IV. PARITY GENERATOR

Parity bit is an extra bit included with the binary information to detect errors during the transmission of binary information. In digital communication, an extra bit is added in binary message such that the total number of 1s in the message can be either odd or even according to the type of parity used. The parity generator is a combinational logic circuit that generates the parity bit(s). There are two types of parity generators.

1. Even parity generator
2. Odd parity generator

1. **Even parity generator:** The even parity generator is a combinational logic circuit that generates the parity bit such that the number of 1s in the message becomes even. The parity generator checks the

input's binary information and generators the parity bit 0/1 such that after the addition of parity bit, the total number of 1s in the message become even. Table 3 shows the 3-bit information with even parity.

Table 3. 3-bit information with even parity

A	B	C	Output (P)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

2. **Odd parity generator:** The odd parity generator is a combinational logic circuit that generates the parity bit such that the number of 1s in the message becomes odd. The parity generator checks the input's binary information and generators the parity bit o/1 such that after the addition of parity bit, the total number of 1s in the message become odd. Table 4 shows the 3-bit information with odd parity.

Table 4. 3-bit information with odd parity

A	B	C	Output (P)
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

V. PARITY CHECKER

At the receiving end, a combinational logical circuit is used to check the parity of the received information. It determines whether the error is included in the message or not. The combinational logic circuit used at the receiver to check the parity of received information is known as the parity checker. There are two types of parity checkers:

1. Even parity checker
2. Odd parity checker

1. **Even parity checker:** The even parity checker is a combinational logical circuit. It has n-bit inputs message and a parity error as the output. The circuit checks the parity of inputs and provides the output 0/1. For an even parity checker, if the parity of input massage is even, then the output is zero. Otherwise the output is 1. When the output is 1, it shows there is error in the message. The truth table of a 4-bit even parity checker is given in Table 5.

Table.5 even parity checker

A	B	C	Pin	Output (P)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

2. **Odd parity checker:** The odd parity checker is a combinational logical circuit. It has n-bit inputs message and a parity error as the output. The circuit checks the parity of inputs and provides the output 0/1. For an odd parity checker, if the parity of input massage is odd, then the output is zero. Otherwise the output is 1. When the output is 1, it shows there is error in the message. The truth table of a 4-bit odd parity checker is given in Table 6.

Table 6. even parity checker

A	B	C	Pin	Output (P)
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

VI. PROPOSED DESIGN

In Fig.3 shows the Design of Even and odd Parity Generator/Checker/ Parity Generator and Checker using MFRG Gate.

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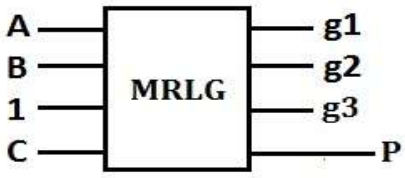
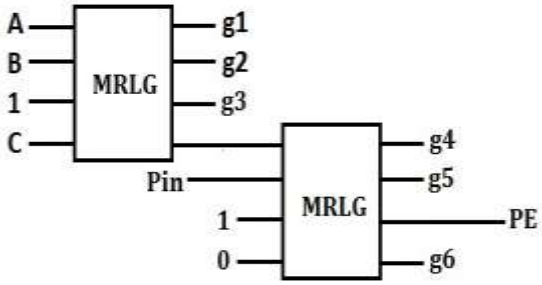
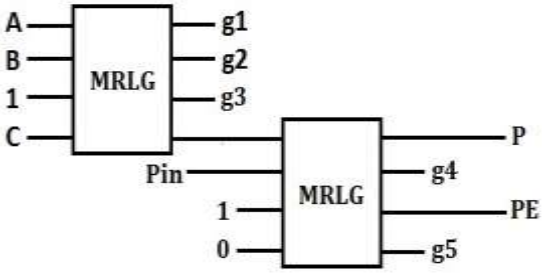
85 - 91



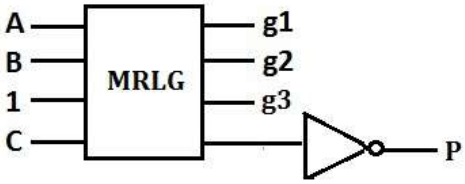
3.A) Even Parity Generator



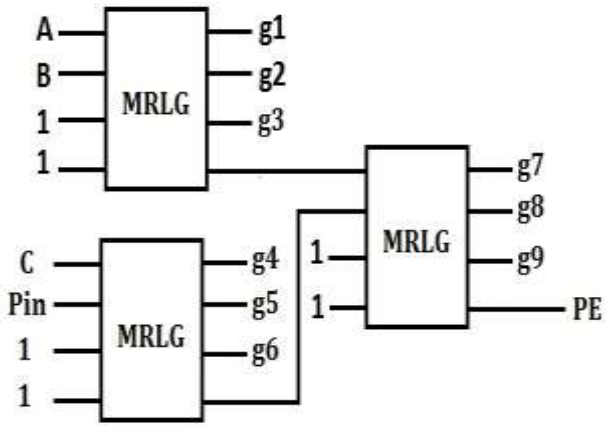
3.B) Even Parity checker



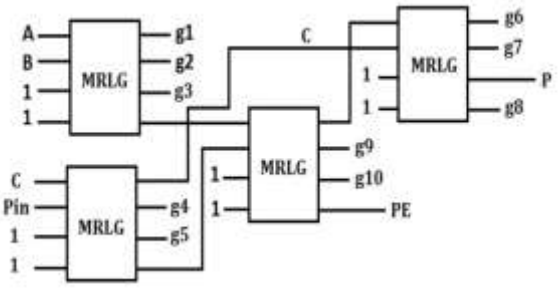
3.C) Even Parity generator and checker



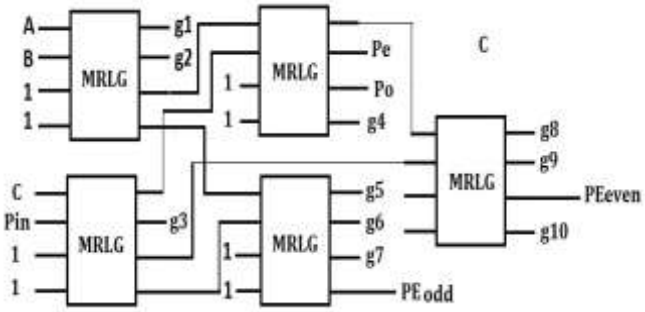
3.D) Odd Parity Generator



3.E) Odd Parity checker



3. F) Odd Parity checker and Generator

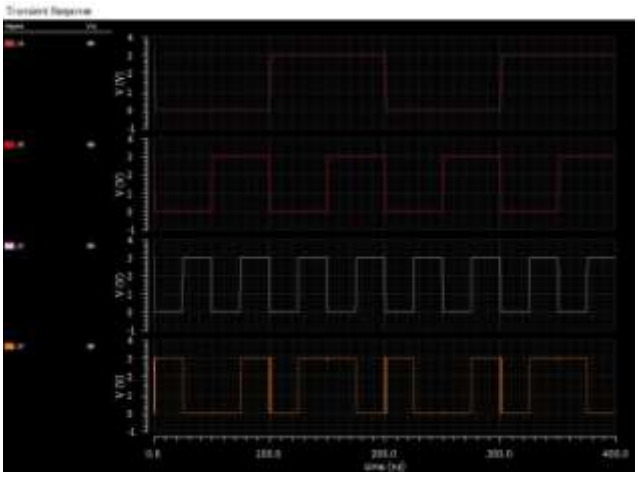


3.G) Even and Odd Parity checker and Generator

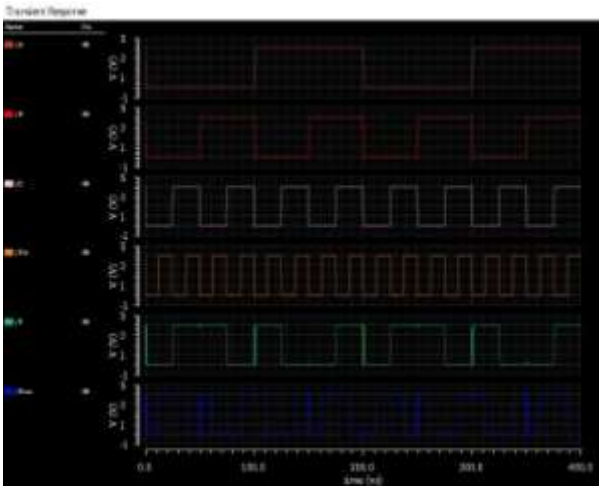
Fig.3 Design of Even and odd Parity Generator/Checker/ Parity Generator and Checker using MFRG Gate

VII. RESULTS AND DISCUSSION

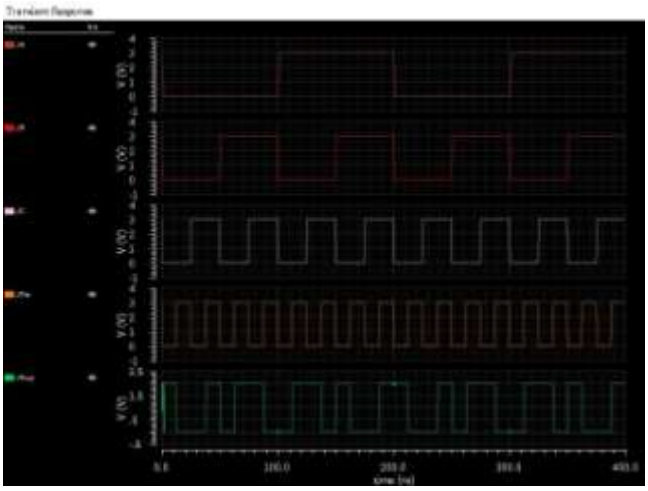
The proposed design is simulated using Cadence software. Input and Output waveform of Even and odd Parity Generator/Checker/ Parity Generator and Checker shown in fig.4. In Table 4. Shows the average power dissipation calculated for the entire input bit pattern. In comparison of different techniques, the advantage of this design is not only depends on transistor count, delay, and power but also on delay product) and PDP (power and delay product) values. The comparisons of transistors count, Power dissipation, Delay, and PDP are shown in Table 4.



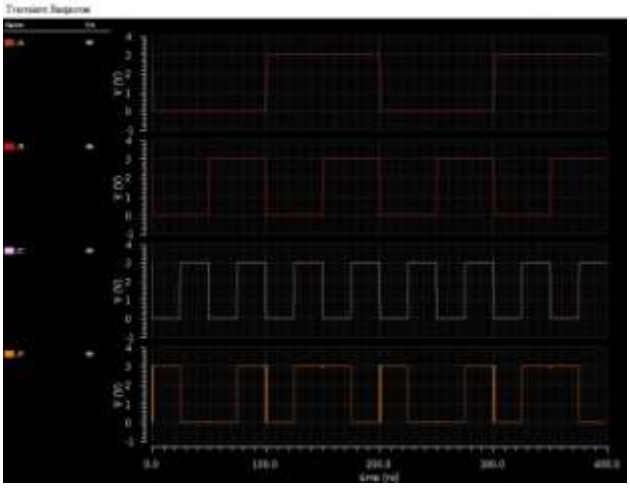
4.A) Even parity generator



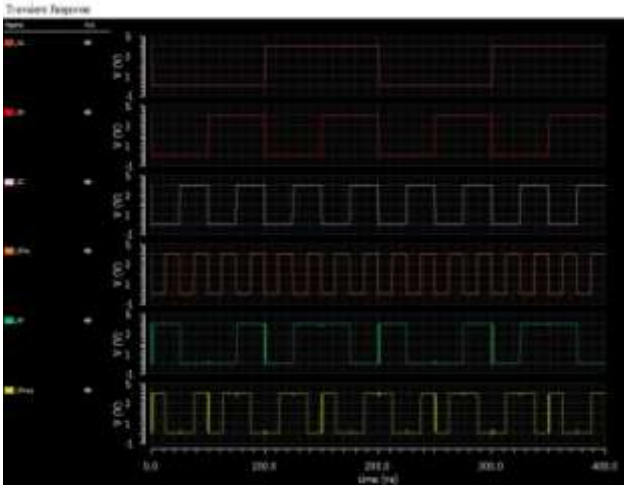
4.B) Even parity checker



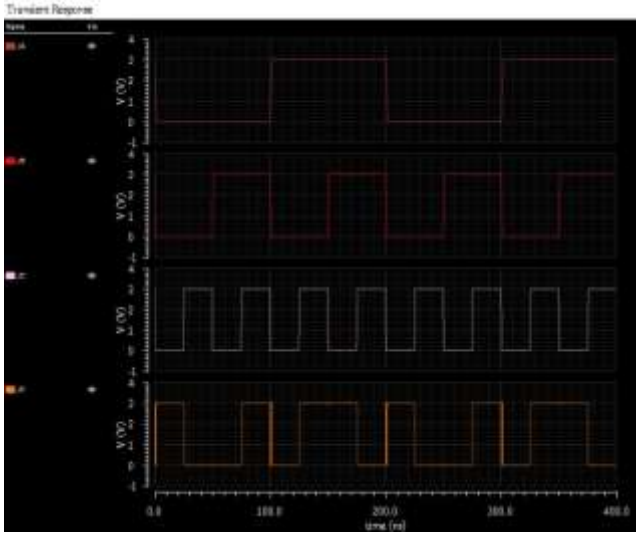
4.E) Odd parity checker



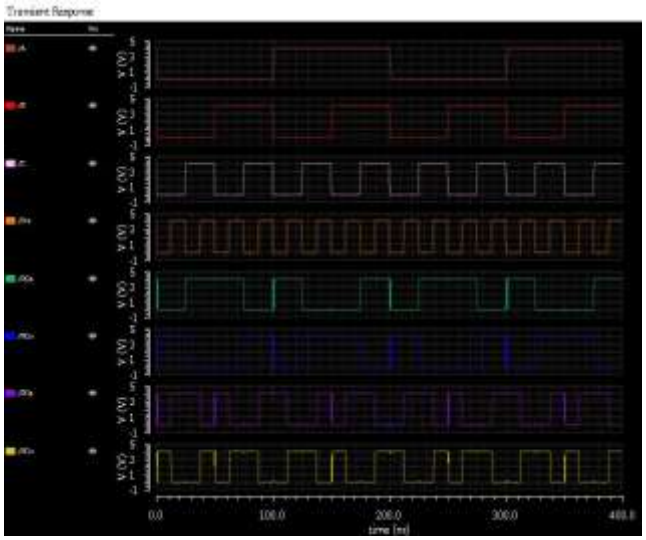
4.C) Even parity generator and checker



4.F) Odd parity generator and checker



4. D) Odd parity generator



4. G) Even and odd parity generator and checker

Fig.4. Input and Output waveform of Even and odd Parity Generator/Checker/ Parity Generator and Checker.

Table4. Synthesis results of Even and odd Parity Generator/Checker/ Parity Generator and Checker

	MRLG gate count	Garbage output	Applied voltage	Average power dissipation (µW)	Delay (ns) (average)	Power delay product
Even Parity Generator	1	3	1.5 V	12.74	0.1757	2.2384
			2 V	33.67	0.2753	9.2693
			3 V	144.1	0.4641	66.876
			4 V	395.1	0.4368	172.57
Even Parity Checker	2	6	1.5 V	6.6	0.1250	8.325
			2 V	136.8	0.4166	56.990
			3 V	438.5	0.5392	236.43
			4 V	1046	0.6122	640.36
Even Parity Generator and Checker	2	5	1.5 V	66.64	0.1239	8.256
			2 V	139.8	0.3048	42.611
			3 V	438.5	0.3924	172.06
			4 V	1046	0.4578	478.06
Odd Parity Generator	2	3	1.5 V	13.95	0.2924	4.0789
			2 V	36.02	0.3792	13.658
			3 V	150.8	0.5011	75.565
			4 V	411.9	0.6526	268.80
Odd Parity Checker	3	9	1.5 V	86.68	1.0711	92.842
			2 V	195.3	0.6732	131.47
			3 V	611.7	0.4313	263.82
			4 V	1449	0.2387	345.87
Odd Parity Generator and Checker	4	10	1.5 V	111.9	0.7373	82.503
			2 V	250.5	0.5472	137.07
			3 V	792.7	0.4612	365.59
			4 V	1885	0.4161	784.34
Even and Odd Parity Generator and Checker	5	10	1.5 V	143.2	0.7744	110.80
			2 V	333.9	0.4876	162.80
			3 V	1100	0.5951	654.61
			4 V	2601	0.4922	1280.2

VIII. CONCLUSION

For error free transmission in the digital communication at the source end used parity generator and at destination used parity checker. The Even and Odd Parity Generator and Checker designed using reversible logic with CMOS and pass transistor switch enables the circuit in providing better performance with low power consumption and minimum delay time with supply voltage 1.5 V to 4 V. The use of MFRL gate for parity generator and the parity checker with reduced power dissipation. The retival of the input data from the output therefore generated is created highly possible by the use of the garbage values. Hence efficient data transmission, reversible logic gates are effective than the conventional methods. The data transmission in the digital form using the reversible logic gates the loss of information is zero. The simulation is done on cadence software with transistor length 180nM and width 2µM transistor with gpdk 180 process.

REFERENCES

[1] Bennett, C.H., "Logical Reversibility of Computation", IBM Journal Research and Development, 525-532. 1973.

[2] Azad Khan, M.H, "Design of Full-Adder with Reversible Gates", International Conference on Computer and Information Technology, Dhaka, Bangladesh, pp: 515-519. 2002.

[3] Bisdounis, L., D. Gouvetas and O. Koufopavlou, "A comparative study of CMOS circuit design styles for low-power high-speed VLSI circuits". International Journal of Electronics, 599-613. 1998.

[4] Chatzigeorgiou, A. and S. Nikolaidis, "Modeling the operation of pass transistor and CPL gates", International Journal Electronics, 977-1000, 2001.

[5] Feynman, R., "Quantum Mechanical Computers", Optic News, 11-20, 1985.

[6] Fredkin, E. and T. Toffoli, "Conservative Logic", International Journal of Theoretical Physics. 219-253. 1982.

[7] Himanshu Thapliyal and Nagarajan Ranganathan, "A New Design of the Reversible Subtractor circuit", 11th IEEE international Conference Nanotechnology, 2011.

[8] Himanshu Thapliyal and M.B. Srinvas, "Novel Reversible TSG gate and Its Application for Designing Components of Primitive Reversible/ Quantum ALU", ICICS 2005.

[9] Krishnaveni, D. and M. Geetha Priya, "Design of Reversible Serial and Parallel Novel Adder/Subtractor", International Journal of Engineering Science and Technology; (IJEST) march. 2011.

[10] Landauer, R., "Irreversibility and Heat Generation in the Computing Process", IBM Journal Research and Development, 183-191, 1961.

[11] Majid haghparast and Keivan Navi, "A Novel Reversible Full Adder Circuit for Nanotechnology Based Systems", Journal of Applied Sciences, 3995-4000, 2007.

[12] Maslov, D., D.M. Miller and. G.W. Dueck, "Techniques for the Synthesis of Reversible Toffoli Networks", ACM Transaction Design Automated Electronic System, 2007.

[13] Morgenshtein, A, A. Fish and I.A. Wagner, "Gate-diffusion input (GDI): A power-efficient method for digital combinatorial circuits", IEEE Transaction on VLSI, 566-581, 2002.
[14] Peres, A., "Reversible Logic and Quantum Computers", Physical Review, 3266-3276. 1985.
[15] R. Landauer, ―Irreversibility and heat generation in the computing process, IBM J. Res. Develop., vol. 3, pp. 183–191, 1961.
[16] V. V. Zhirnov, R. K. Cavin, J. A. Hutchby, and G. I. Bourianoff, ―Limits to binary logic switch scaling—A Gedanken model, Proc.IEEE, vol. 91, no, 11, pp. 1934–1939, Nov. 2003.
[17] C. Bennett, ―Logical reversibility of computations, IBM J. Res.Develop., vol. 17, no. 6, pp. 525–532, 1973.
[18] T. Ogriro, A. Alhazov, T. Tanizawa, and K. Morita, ―Universality of 2-state 3-symbol reversible logic elements—A direct simulation method of a rotary element, in Int. Workshop Natural Comput. (IWNC2009), Proc. Inform. Commun. Technol. (PICT), 2010, vol. 2, pp. 252–250.
[19] T. Sasao and K. Nimoshita, ―Conservative logic elements and their universality, IEEE Trans. Comput., vol. C-28, no. 9, pp. 682–685, Sep.1979.
[20] M. A. Karim and A. A. S. Awal, Optical Computing: An Introduction. New York: Wiley, 1992, chs. 7 and 9.
[21] J. E. Rice, ―Project in reversible logic, Dept. Math. Comput. Sci., Univ.Lethbridge, Lethbridge, AB, Canada, Tech. Rep. TR-CSJR1-2005, Jul.2005.
[22] H. M. H. Babu and A. R. Chowdhury, ―Design of a compact reversible binary coded decimal adder circuit, J. Syst. Archit., vol. 52, pp. 272–282,2006.
[23] H. R. Bhagyalakshmi and M. K. Venkatesha, ―Optimized reversible BCD adder using new reversible logic gates, J. Comput., vol. 2, no. 2, pp. 28–32, 2010.
[24] D. P. Vasudevan, P. K. Lala, J. Di, and J. P. Parkerson, ―Reversable-logic design with online testability, IEEE Trans. Instrum.Meas., vol. 55, no. 2, pp. 406–414, Apr. 2006.
[25] Vinay Kumar, Divya Dhawan "An approach To Design of Reversible Synchronous Counters Using Pseudo Reed – Muller Expression", IRJETERM, vol.1 issue 8, pp. 37-48, 2015.
[26] S.S.Gayathri, A.V.Ananthalakshmi, "Design And Implementation Of Efficient Reversible Even Parity Checker And Generator", International Conference on Science, Engineering and Management Research (ICSEMR), 2014.
[27] Vinay Kumar, Divya Dhawan, "An Approach to Design a New Multifunctional Reversible Logic Gate (MRLG)", International Journal of Innovative Research in Computer and Communication Engineering, vol.4 issue 5 pp. 9249-9256, 2016.