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Power Droop Reduction In Logic BIST By Scan Chain Reordering

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Abstract—Significant peak power (PP), thus power droop (PD), during test is a serious concern for modern, complex ICs. In fact, the PD originated during the application of test vectors may produce a delay effect on the circuit under test signal transitions. This event may be erroneously recognized as presence of a delay fault, with consequent generation of an erroneous test fail, thus increasing yield loss. Several solutions have been proposed in the literature to reduce the PD during test of combinational ICs, while fewer approaches exist for sequential ICs. In this paper, we propose a novel approach to reduce peak power/power droop during test of sequential circuits with scan-based Logic BIST. In particular, our approach reduces the switching activity of the scan chains between following capture cycles. This is achieved by an original generation and arrangement of test vectors. The proposed approach presents a very low impact on fault coverage and test time.

Keywords-*Significant peak power, power droop, Logic BIST.*

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I. INTRODUCTION

The system-on-chip (SoC) revolution in parallel with the rising complexity of VLSI circuits has made the issue of automated testing inevitable. Power dissipation in the testing phase is a major challenge for the testing engineers. The power droop occurs in both shift phase & capture phase but majorly in capture phase. So we have come up with our project " POWER DROOP REDUCTION IN SCAN-BASED LOGIC BIST USING SCANCHAIN REORDERING ".Essentially, introduction of scan cells in the circuit, is one of the most widely used and accepted way of testing.Re-ordering of these scan cells significantly reduces the power consumption during the testing. In our project, we strive to minimize the power droop by reordering of scan cells.

The main objective of this project is to reorder the scan chain in such a way that the power droop(reduction) will be significantly reduced. Weachieved this by reducing the switching activity which is the major reason for the power droopis reduced to a certain extent comparing to the existing method that we had considered as our base paper. By our approach the area is also reduced by reducing the number of gates.

II. LITERATURE SURVEY

We consider the widely adopted scan-based LBIST architecture represented in fig2.1.The state flip-flops of the CUT are converted into scan flip-flops, and arranged into many short scan chains. Additional scan flip - flops are included in such scan chains to drive and sample the primary inputs (PI) and primary outputs (PO), respectively.The Pseudo-Random Pattern Generator (PRPG) is implemented by an LFSR [4, 12, 15]. The Phase Shifter (PS), allowing reducing the correlation among the test vectors applied to adjacent scan-chains [15], is composed by an XOR network expanding the number of outputs of the LFSR in order to match the number of scan chains s. In fact, the number of LFSR outputs is usually considerably smaller than the number of scan chains. At the same clock cycle, the PS provides as outputs, the current LFSR sequence together with many future/past sequences. As described later on, this feature will be exploited by our proposed solution in order to derive the new test vectors allowing reducing PD during capture cycles.

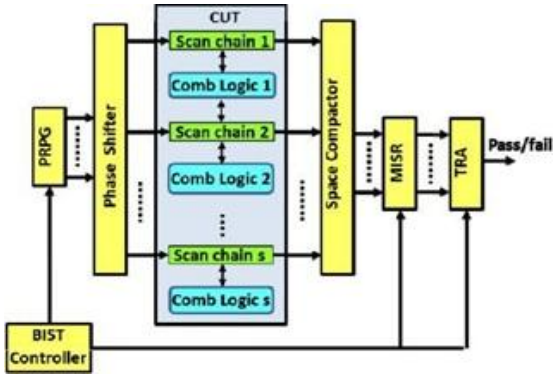

Figure 1: Considered Scan-Based LBIST Architecture

Proposed Approach For Power Droop Reduction During Scan-Based LBIST:

In this section, we introduce our approach for PD reduction during the capture phase in scan-based LBIST. As

previously introduced, our approach exploits the phase shifter (PS) to determine the substitute test vector replacing the original test vector to be applied to the scan chain m(m=1..s) at the i-th capture cycle. Our approach allows a reduction of approximately 50% in the SA of the CUT with respect to conventional LBIST, while featuring the same fault coverage and test length. In turn, this leads to a significant reduction of the PD and, consequently, of the probability to generate false test fails. Since our approach reduces the number of switching bits in the new test sequence compared to conventional LBIST, the power consumption associated to glitches due to unbalanced paths within the CUT is expected to be reduced as well. It is worth noticing that, if a higher SA reduction is required, our solution can be properly scaled by introducing two or more proper substitute test vectors (depending on the target SA reduction) between two original test vectors.

Possible Implementation:

Our solution exploits the fact that, for each scan chain m and capture cycle i, at every scan CK cycle j (j=1..n), the PS provides at its outputs the values (m = 1.. s), together with many of its past/future values. In fact, if the number of outputs m of the PS is considerably larger than the depth n of the longest scan chain (i.e., if m >> n) , as it is usually the case in actual designs , then it is very likely that the value of at n past and future CK cycles are provided by other outputs of the PS. Nevertheless, the PS can be designed in order to provide all necessary values for the application of the proposed approach. Therefore, given the PS design, at each scan CK cycle j, we can determine the past/future logic value at n past and future CK cycles are provided by other outputs of the PS.Nevertheless, the PS can be designed inorder to provide all necessary values for the application of the proposed approach. Denoting by Om (m = 1.. s) the PS output feeding the scan chain m, the logic value in the j- th position of the i-th test vector of the scan chain m, that is ξ is the current shift clock cycle, represented as the number of the total shift clock cycles applied by the LBIST architecture from the beginning of the test. Therefore, considering that each capture cycle i requires n shift cycles, the logic values in the position j of the vector applied at the previous and to be applied at the next capture cycles to the scan chain m are the values assumed by at n cycles before and after, respectively, the current shift clock cycle ξ. As per the characteristic of the PS to provide at its outputs many past/future values of each output Om, we can determine the values of ξ and ξ from the current value present at proper two PS outputs. Therefore, there exist two values k and p, with k, p = 1..s, k p and both different fromorder to provide all necessary values for the application of the proposed approach. Denoting by Om (m = 1.. s) the PS output feeding the scan chain m, the logic value in the j- th position of the i-th test vector of the scan chain m, that is ξ is the current shift clock cycle, represented as the number of the total shift clock cycles applied by the LBIST architecture from the beginning of the test. Therefore, considering that each capture cycle i requires n shift cycles, the logic values in the position j of the vector applied at the previous and to be applied at the next capture cycles to the scan chain m are the values assumed by at n cycles before and after, respectively, the current shift clock cycle ξ. As per the characteristic of the PS to provide at its outputs many past/future values of each output Om, we can determine the values of ξ and ξ from the current value present at proper two PS outputs. Therefore, there exist two values k and p, with k, p = 1..s, k p and both different from

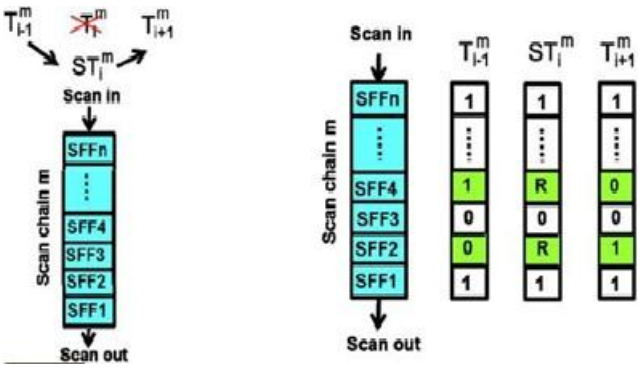

Figure 2:Schematic Representation (a) Sequence Of Test Vectors (b) Substitute Test Vector

III. PROPOSED SYSTEM

For the test of ICs two reference approaches are available: external testing and built-in self-test (BIST), out of which a variety of hybrid test strategies are obtained by test resource partitioning (TRP) . The final goal is to provide advantageous trade off of the test evaluation indicators like: test development and application cost, hardware overhead, fault coverage, etc.

The design for low power has become one of the greatest challenges in high-performance very large scale integration (VLSI) design. As a consequence, many techniques have been introduced to minimize the power consumption of new VLSI systems. However, most of these methods focus on the power consumption during normal mode operation, while test mode operation has not normally been a predominant concern.

Built In Self-Test (BIST):

BIST offers support for in-field, on-line, burn-in and at-speed test that is indispensable for delay fault testing. Moreover, tradeoffs between fault coverage, hardware overhead and test length are possible. External testing coverage for a given test length. The sustained improvement of deep-submicron technologies has led to an explosion in the number of transistors that may be integrated on a chip and further to

possibility of putting a whole system on a chip (SOC).circuit-based design is one paradigm of the new trends used to reduce complexity and costs of ship development. Nevertheless, test-related costs are problems still far away from having a unitary and satisfactory solution. The external testing of integrated circuits (ICs) is a traditional approach in which automated test equipment (ATE) provides all the necessary test data. This may set high requirements on the storage capacity and speed of the ATE. Furthermore, the ever increasing transistor count per I/O pin and the low accessibility of internal blocks are affecting the tradeoff between the final fault coverage and the test application time. All of these, combined with the necessity of specially tuned testers for different types of cores and the growing need for periodic in- field maintenance and on-line testing capabilities make the external testing difficult , costly and insufficient. All the above mentioned problems demand built-in self-test (BIST) solution.

BASIC CONCEPT:

Built-in-self-test (BIST) is a technique in which additional circuitry is added to core under test (CUT) in order to make it able to test itself with minimum external help. General structure of a self-testable circuit composed of test pattern generator (TPG) , a test response evaluator (TRE) and a BIST control unit (BCU) .This technique is especially preferable when it is difficult to access the CUT externally. It also helps to protect intellectual property (IP)and to reduce cost of theexternal test equipment (ATE) by minimizing the amount of test data that has to be stored off-chip. it implementation can result in an improvement in the test quality due to its better support for at-speed testing, which is essential for detecting delay faults. BIST supports in-field and on-line testing, which helps to reduce the cost of system maintenance. It also offers the opportunity to improve reliability by means of burn-in testing.

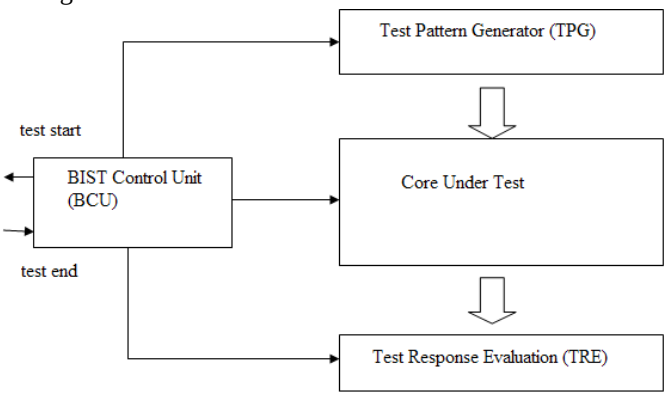

Figure 3:built in self-test

Test per Scan Schemes:

Test-per-scan BIST schemes require scan-based design. In the case of sequential circuits, this means that all the storage cells can be configured as one or several scan paths (chains), which are used as serial shift registers in test mode .In this way, each storage device of the CUT becomes easily controllable and observable. The test stimuli/responses are shifted into/out of the scan paths. Scan-based design helps to reduce the problem of testing sequential circuits to the simpler problem of testing combinational circuits. The shift counter controls the bit stream which is generated and shifted into the scan path by a TPG.

Test per Clock Schemes:

In a test-per-clock scheme a test pattern is applied to the CUT every clock cycle. This scheme is best suited for register-based design. This kind of scheme employs a specific BIST architecture using the built-in logic block observer (BILBO), which is a more sophisticated register that can function as a normal state register, scan register, PRPG or MISR All functionality of the BILBO depends on the mode input signals.

Test Pattern Generation:

Test pattern generation for both test-per-scan and test-per-clock BIST schemes can be classified into the following groups: pseudo-random, weighted, exhaustive, pseudo exhaustive, deterministic and mixed-mode schemes.

Pseudo Random Pattern Generation:

Pseudo-random pattern testing is an attractive approach for BIST. Possible choices for pseudo-random pattern generators (PRPGs) are one-dimensional linear hybrid cellular automata (LHCAs), linear feedback shift registers (LFSRs) or different accumulator based structures As processor kernels or programmable units are integrated into SOCs, they can also be used for pattern generation .

Weighted Random Pattern Testing:

Although LFSRs, LHCAs or other linear TPGs can generate a large set of pseudorandom test patterns with very simple hardware, this seldom provides sufficient fault coverage for a CUT. A way to address this problem is to use weighted-random pattern testing techniques. The TPG used in weighted-random pattern testing is composed of an LFSR and additional combinational logic to modify the probability of ones and zeros in the output sequence. This weighting circuitry is used to bias the pseudo-random patterns towards those that detect random pattern resistant faults, such that the fault coverage is increased and the test length can be reduced.

Exhaustive and Pseudo-Exhaustive Testing:

Exhaustive testing applies all possible 2n test patterns to an n-input combinational circuit, so that a high quality test can be obtained and no particular fault model is used. The test pattern generator can be a binary counter or an LFSR with a primitive feedback polynomial, in which the all-zero pattern may be

generated by a reset signal. As the number of test patterns increases exponentially with the number of the circuit inputs, this approach is usually not feasible for circuits with a large number of inputs (n>30). Pseudo-exhaustive testing relies on the partition of the CUT into output cones which are tested exhaustively .As compared to exhaustive testing, far fewer test patterns are required. Evertheless, the feasibility of pseudo-exhaustive testing depends on the size of the largest output cone.

Deterministic Testing:

Deterministic testing applies a pre-computed set of test cubes (test patterns with unspecified bits) to the CUT. Thus, any coverage of the testable faults can be achieved. The patterns may be stored on-chip, e.g. using a ROM, or off-chip in which case they have to be loaded from an ATE. In both approaches the data volume to be stored tends to be extremely large. In the case of the ATE-based approach this may also have a strong impact on the required bandwidth. In order to reduce the storage and bandwidth requirements, special algorithms for generating compact test. Similar approaches can also be used with (ROM based) BIST schemes to reduce the storage requirements. Such methods are often called store and generate.

Mixed Mode Testing:

Mixed-mode approaches can achieve more efficient test data compression and hardware implementation than pure deterministic test schemes. Mixed-mode testing combines pseudo-random testing with various deterministic testing schemes so that the test storage requirements can be significantlyreduced and high levels of fault coverage can be obtained within a reasonable test application time.

Test Response Evaluation:

Besides test pattern generation, BIST architectures should also be able to compress/evaluate test responses. As the number of test patterns applied to the CUT is usually very large, it is infeasible to store all the expected values on-chip and compare them with the response values. It is much cheaper in terms of storage requirement and compacting circuitry to compress the test responses to short sequences, called signatures, which are delivered foranalysis at the end of the test session. A signature is obtained as the final state of a finite state machine whose inputs are fed with test responses. This type of compression which addresses the length of the test response sequence is also known as time compression. Examples of time compressors are accumulator, LFSR- and counter-based compactors.

Proposed LFSR:

Proposed LFSR is a combination of LFSR and 2*1 multiplexer. Swapped output is obtained from the final value of BS LFSR .we see how the swapped output is obtained is explained bellow In this we choose one of the cells and swap its value with its adjacent cell , if the current value of 3rd cell in the LFSR is 0 and leave the cells and swapped if the 3rd cell has a value I 1.the value of third cell is described as selection line value The selection line is linked to one of the swapped cells through an xor gate in this configuration a single cell can save 50% transition that where originally produced by an LFSR cell.

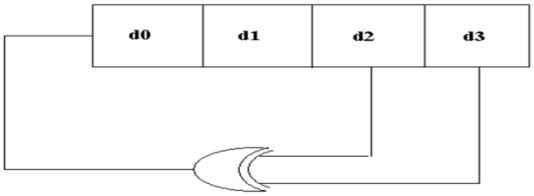

Figure 4: conventional LFSR

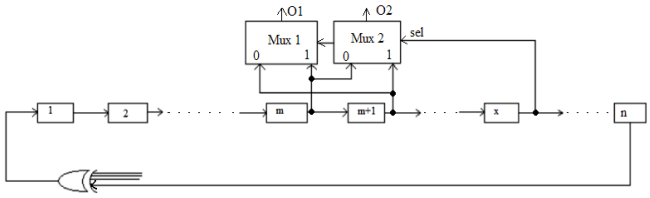

Figure 5:swapping arrangement of LFSR

IV . SOFTWARE DESCRIPTION

Xilinx:

Xilinx ISE[1] (Integrated Software Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer. The Web Edition is a free version of Xilinx ISE that can be downloaded at no charge. It provides synthesis and programming for a limited number of Xilinx devices. In particular, devices with a large number of I/O pins and large gate matrices are disabled.

The low-cost Spartan family of FPGAs is fully supported by this edition, as well as the family of CPLDs, meaning small developers and educational institutions have no overheads from the cost of development software.The Spartan-3 platform was the industry's first 90nm FPGA, delivering more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry.

Xilinx designs, develops and markets programmable logic products, including integrated circuits (ICs), software design

tools, predefined system functions delivered as intellectual property (IP) cores, design services, customer training, field engineering and technical support. Xilinx sells both FPGAs and CPLDs for electronic equipment manufacturers in end markets such as communications, industrial, consumer, automotive and data processing. Xilinx's FPGAs have been used for the ALICE (A Large Ion Collider Experiment) at the CERN European laboratory on the French-Swiss border to map and disentangle the trajectories of thousands of subatomic particles. Xilinx has also engaged in a partnership with the United States Air Force Research Laboratory's Space Vehicles Directorate to develop FPGAs to withstand the damaging effects of radiation in space, which are 1,000 times less sensitive to space radiation than the commercial equivalent, for deployment in new satellites.

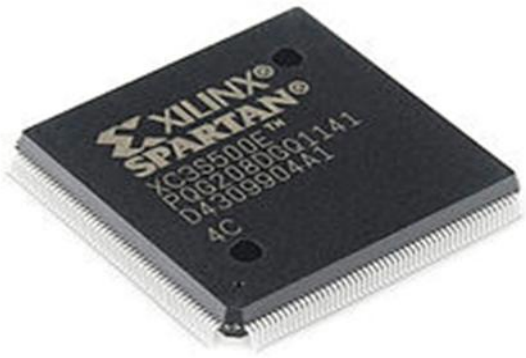

Figure 6: output of GSM initialization

MODELSIM:

ModelSim® PE, our entry-level simulator, offers VHDL, Verilog, or mixed-language simulation. Coupled with the most popular HDL debugging capabilities in the industry, ModelSim PE is known for delivering high performance, ease of use, and outstanding product support.

Model Technology's award-winning Single Kernel Simulation (SKS) technology enables transparent mixing of VHDL and Verilog in one design. Modalism's architecture allows platform independent compile with the outstanding performance of native compiled code.

An easy-to-use graphical user interface enables you to quickly identify and debug problems, aided by dynamically updated windows. For example, selecting a design region in the Structure window automatically updates the Source, Signals, Process, and Variables windows. These cross linked ModelSim windows create a powerful easy-to-use debug environment. Once a problem is found, you can edit, recompile, and re-simulate without leaving the simulator.ModelSim PE fully supports the VHDL and Verilog language standards. You can simulate behavioral, RTL, and gate-level code separately or simultaneously. ModelSim PE also supports all ASIC and FPGA libraries, ensuring accurate timing simulations. ModelSim PE provides partial support for VHDL 2008.

VHDL:

Integrated circuits were made possible by experimental discoveries which showed that semiconductor devices could perform the functions of vacuum tubes, and by mid-20th-century technology advancements in semiconductor device fabrication. The integration of large numbers of tiny transistors into asmall chip was an enormous improvement over the manual assembly of circuits using discrete electronic components. The integrated circuit's mass production capability, reliability, and building-block approach to circuit design ensured the rapid adoption of standardized ICs in place of designs using discrete transistors. There are two main advantages of ICs over discrete circuits - cost and performance. Cost is low because the chips, with all their components, are printed as a unit by photolithography and not constructed a transistor at a time. Performance is high since the components switch quickly and consume little power, because the components are small and close together. As of 2006, chip areas range from a few square mm to around 250 mm2, with up to 1 million transistors per mm2.

RTL CODING SIMULATION AND SYNTHESIS:

In RTL coding, Micro design is converted into Verilog/VHDL code, using synthesizable constructs of the language. Normally we like to lint the code, before starting verification or synthesis .Simulation is the process of verifying the functional characteristics of models at any level of abstraction. We use simulators to simulate the Hardware models. To test if the RTL code meets the functional requirements of the specification, we must see if all the RTL blocks are functionally correct. To achieve this we need to write a test bench, which generates clk, reset and the required test vectors. We use the waveform output from the simulator to see if the DUT (Device under Test) is functionally correct. Synthesis is the process in which synthesis tools like design compiler or Simplify take RTL in Verilog or VHDL, target technology, and constrains as input and maps the RTL to target technology primitives. Synthesis tool, after mapping the RTL to gates, also do the minimal amount of timing analysis to see if the mapped design is meeting the timing requirements.

IV. RESULTS AND DISCUSSIONS

In the results ,we are reduced the area ,delay and power consumption lower than the existing system .The comparison between the existing and proposed system for the area ,time and power is explained below in a clear view.

Comparison of Area:

Here in our project the area has been reduced when comparing to the existing system .In the below comparison of area in existing system is (277) reduced to (224) in proposed system respectively.

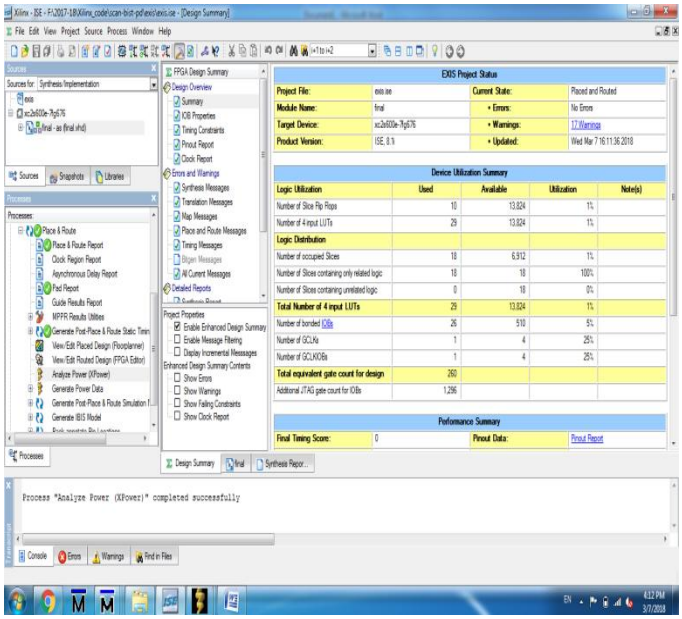

Figure 7: Area Obtained In Existing Method

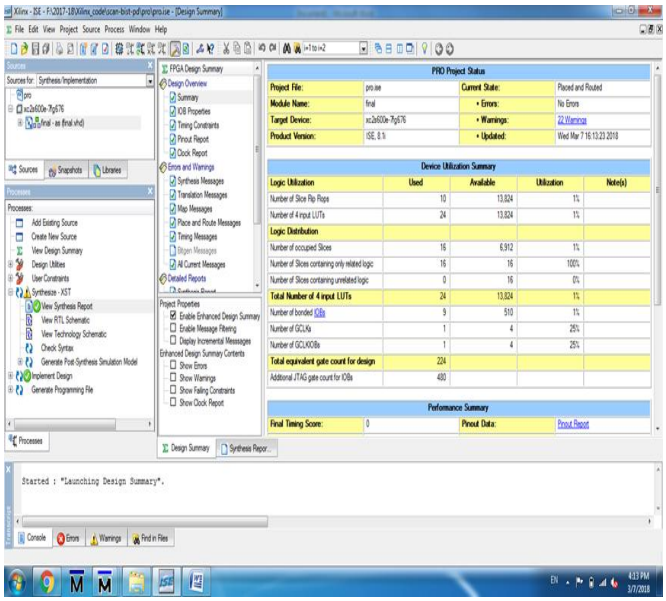

Figure 8:Area Obtained In proposed Approach

Comparison of Delay:

Here in our project the delay has been reduced when comparing to the existing system .In the below comparison of delay in existing system is (5.31ns) reduced to (5.07ns) in proposed system respectively. The comparison in figure (5.3&5.4) shows the comparison of delay by our approach.

Comparison of Power Consumption:

Here in our project the power has been reduced when comparing to the existing system .In the below comparison of power in existing system is (371W) reduced to (344W) in proposed system respectively. The below comparison in figure (5.5&5.6) shows the comparison of delay in our approach.

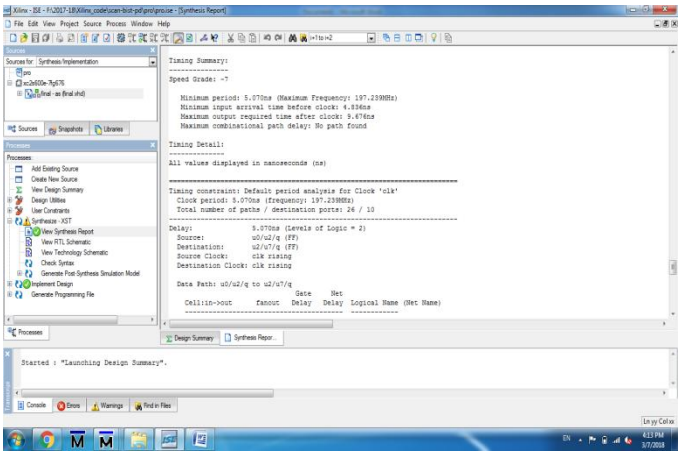

Figure 9: Delay in Proposed Method

PARAMETERS	EXISTING SYSTEM	PROPOSED APPROACH
Area	277	224
Delay	5.31ns	5.07ns
Total power consumed	371W	344W

Table1:Comparison ofArea, PowerAnd Delay

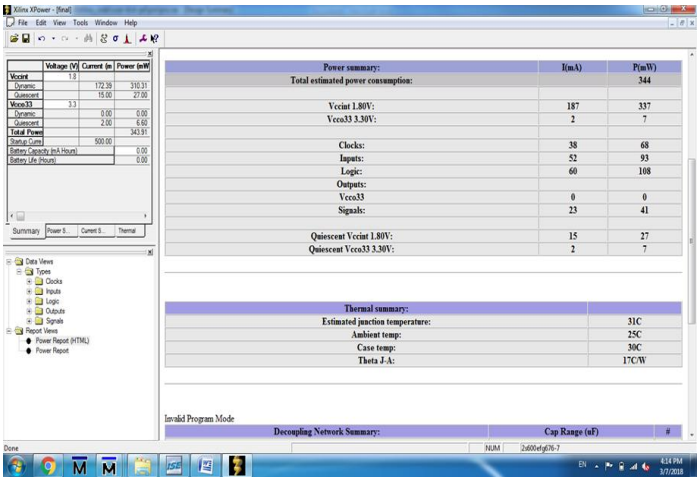

Figure 10: Power Consumption in Proposed Approach

V. CONCLUSION

We have presented a novel approach to reduce peak power and power droop during the capture cycles in scan-based Logic BIST, thus reducing the probability that the induced delay effect is erroneously recognized as presence of a delay fault,

with consequent erroneous generation of a test fail. We showed that our approach allows reducing by approximately the power consumption using algorithm in the scan chains on design itself with respect to standard scan-based LBIST. This is achieved by exploiting the operation of the phase shifter, usually inserted in LBIST structures in order to reduce the correlation among the test patterns applied to adjacent scan- chains. We also showed that our approach reduces area and time delay inside the process .The proposed approach exhibits no impact on increasing power, delay and area respectively. Moreover, it is fully compatible with standard scan-based LBIST architectures.In future work, it will be good to apply this algorithm everywhere it is useful to create more number of products on this study side easily. In our thesis we have used scenario, it will be good to apply the algorithm by using this inside the scan chain will reduce surely the area, delay and powerrespectively. Moreover, we have compared both the existing and proposed with the comparison charts for a clear view. It will be interesting to see how these algorithm works in a real environment and how these algorithm reacts across study when it is implemented in a real environment

VI. ACKNOWLEDGMENT

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