National Conference on Innovative Trends in Science and Engineering (NC-ITSE'16)
Volume: 4 Issue: 7
ISSN: 2321-8169
239 - 243

Optimization of Mac Unit with Block Enabling Technique

[1] Mr. Tejrao P. Marode
ME Student,Department of Electronics And Telecommunication Engineering,
Shri SantGajananMaharaj College Of Engineering,
Amravati University,
SHEGAON-444203, Maharashtra, India.
e-mail :tejrao7777@gmail.com

[2]Dr. G. S. Gawande
HEAD,Department of Electronics And Telecommunication Engineering,
Shri SantGajananMaharaj College Of Engineering,
Amravati University,
SHEGAON-444203, Maharashtra, India.
e-mail : gopalgawande@rediffmail.com

Abstract : Multipliers are the key components of Digital filters. The filter designer has to proposed a low power multiplier and accumulator(MAC) unit as most of the Multiplication involves multiplication of multiplier and multiplicand and addition of the partial product generated. In Wallace tree multiplier the number of partial products are reduced. In this paper 8 x 8 bit Wallace tree multiplier is constructed and implemented. Wallace tree multiplier uses full adders and half adders, 4:2 compressor, 3:2 compressor in their reduction phase of the partial products. Considering this design, minimizing the number of half adders used will reduced the complexity of design. This Wallace tree multiplier is used in the Multiplier accumulator unit(MAC) and block enabling technique is applied to the MAC unit to optimized the power of MAC unit.

Key Words :*CSA, Compressor, Wallace,MAC.*

*****

1.INTRODUCTION

In digital signal processing (DSP) applications the critical operations usually involve many multiplications and/or accumulations. The multiplication and accumulation is an important operation in digital filter structures. The main goal of this work is to design and implement an efficient architecture for computing MAC.High throughput Multipliers-Accumulator (MAC) are always a key to achieve a high performance digital signal processing system. The main consideration of MAC design is to enhance its speeds. A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the time and power consuming element in the system. Furthermore, it is generally the most time and power consuming. Hence, optimizing the speed and power of the multiplier is a major design issue.

A detail study is done on Wallace tree multiplier which uses carry save adders to reduce an N-row bit product matrix to an equivalent two row matrix that is then summed with a carry propagating adder to give the product. Now the MAC unit is designed using the Wallace tree multiplier. This MAC unit is implemented and realized. Block enabling technique is applied to the same MAC unit and it is implemented and realized.After implementation of the MAC unit with and without block enabling technique, its performance is analyzed. The power analysis shows that the power is minimized for MAC with block enabling technique. So ultimately we have minimized the MAC unit and optimized the digital filter structures using block enabling technique.

1.1Wallace Tree Construction

There exist a handful ofways to implement the Wallace Tree. One method is to consider all the bits in each column at a time and compresses them into two bits. (a sum and a carry). A second method, which is used in this paper, considers all the bits in each fours rows at a time and compresses (see Figure 1). [11]

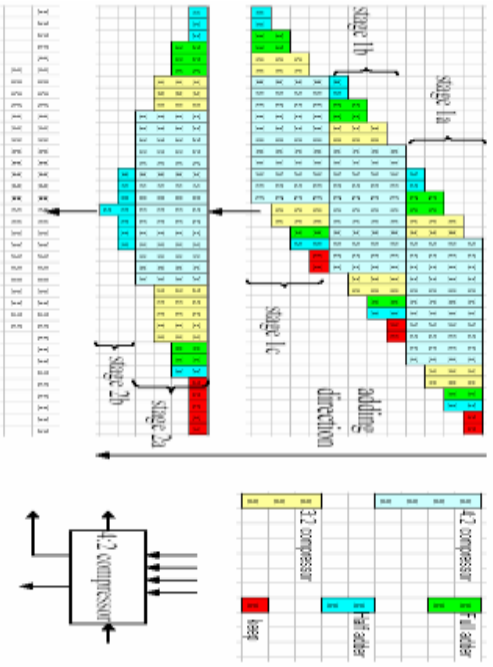

Fig 1. Traditional Wallace Tree construction

In Figure 1, the Wallace tree uses 4:2 compressor, 3:2 compressors, full adders and half adders to compress a 12 partial products tree. Each 4:2 compressor takes in four bits from the same position "j", one bit fromthe previous position "j-1" (which is the carry our of the compressor in the previous position) and outputs one sum bit in the position "j" and two

 ISSN: 2321-8169
239 - 243

carry outs into the next position "j+1".[11]

2. BACKGROUND

Any multiplier can be divided into three stages: Partial products generation stage, partial products addition stage, and the final addition stage. In the first stage, the multiplicand and the multiplier are multiplied bit by bit to generate the partial products product The second stage is the most important, as it is the most complicated and determines the speed of the overall multiplier. This project will be focused on the optimization of this stage, which consists of the addition of all the partial products. If speed is not an issue, the partial products can be added serially, reducing the design complexity. However, in high- speed design, the Wallace tree construction method is usually used to add the partial products in a tree-like fashion in order to produce two rows of partial products that can be added in the last stage. Although fast, since its critical path delay is proportional to the logarithm of the number of bits in the multiplier, the Wallace tree introduces other problems such as wasted layout area and increased complexity. In the last stage, the two-row outputs of the tree are added using any high-speed adder such as carry save adder to generate the output result.

3. WALLACE TREE MULTIPLIER DESIGN

The critical path of the Wallace tree is simulated to be less than 1ns. The Wallace tree multiplier block diagram is shown in Figure 2.It takes a 8 bits multiplicand and a 8 bits multiplier and generates result. The partial products are then added in a Wallace tree fashion as shown in Fig.1. It consists of Following numbers of components:[11]

14 – Full Adder
14 – 4:2 compressor
6 – 3:2 compressor
2 – Half Adder

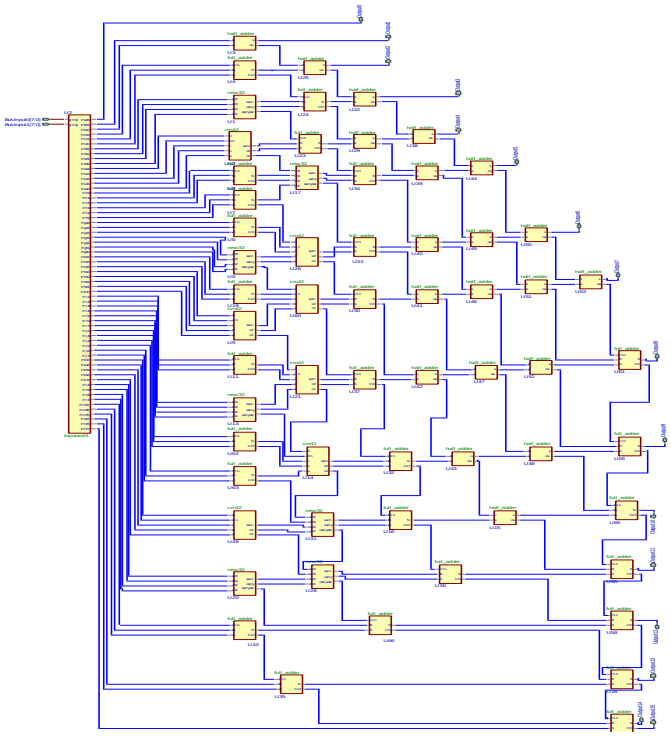

Fig.2 Block Dia. Of Wallace Tree Multiplier

4:2 compressor takes five inputs and produces two outputs with carry given to a next stage. 3:2 compressor takes four inputs and produces two outputs with carry given to a next stage. Full adders takes three inputs to produce two outputs which contains sum and carry while half adders takes two inputs and produces two outputs containing sum and carry. As half adder does not contribute much more in reduction phase , it is necessary to reduce the number of half adders. The modified Wallace tree construction reduces the number of half adders and hence complexity reduces. 8*8 bit multiplication provides 64 partial which are reduced using Wallace tree by using above components.[5]

4. MAC UNIT DESGN

The main consideration of MAC design is to enhance its speed. This is because; speed and throughput rate are always the concern of digital signal processing system. But for the epoch of personal communication, low power design also becomes another main design consideration. This is because; battery energy available for these portable products limits the power consumption of the system.[5]

In any MAC unit, data flows from the input register to the output register through multiple stages such as, multiplier stage, adder stage and the accumulator stage as shown in Fig.3. Within the multiplier stage, further we find that there are multiple stages of addition. During each operation of multiplication and addition, the blocks in the pipeline may not be required to be on or enabled until the actual data gets in from the previous stage. In block enabling technique, we find the delay of each stage. Every block gets enabled only after the expected delay. For the entire duration until the inputs are available, the successive blocks are disabled, thus saving power. [4]

 ISSN: 2321-8169
239 - 243

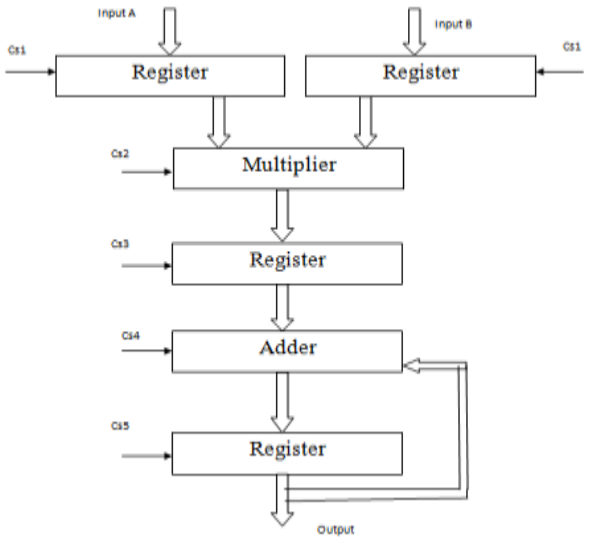

Fig. 3 Block Diagram of pipeline MAC unit

4.1 ARCHITECTURE DETAILS OF MAC

This architecture comprises following components:

1) Latches -3
2) Wallace tree multiplier -1
3) Adder -1

Fig 4 shows Architecture of MAC .This architecture is simple and can be is easily implemented inVLSI

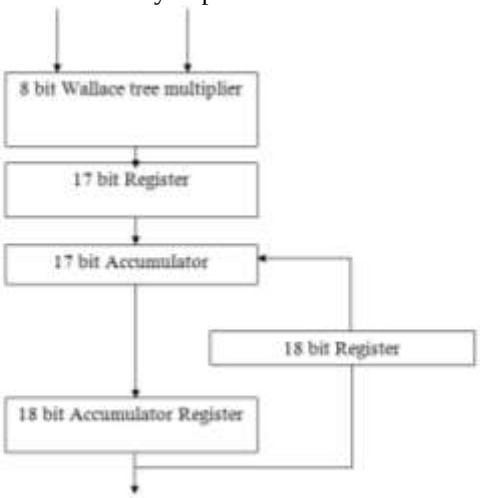

Fig 4. Architecture of MAC

4. BLOCK ENABLING TECHNIQUE

In MAC unit the data flows from the input register to the output register through multiple stages such as, multiplier stage, adder stage and the accumulator stage as shown in Fig.3.the data flows block wise and at each time the block need not to be active as the actual data is not at each block at a given time. The data flows from block to block for a particular time period. So during each operation of multiplication and addition, the blocks in the pipeline may not be required to be on or enabled until the actual data gets in from the previous stage. In block enabling technique, we calculate the delay of each stage. Every block gets enabled only after the expected delay. thus for the particular duration the blocks are enable only when the inputs are available and the successive blocks are disabled at that time. Here the power is minimized or saved.[4,11]

5. IMPLEMENTATION AND RESULTS

5.1 WALLACE TREE MULTIPLIER

The complete circuit of 8*8 bit Wallace tree multiplier is described in VHDL and implemented in Xilinx ISE 13.4 tool. The hierarchical structure is created and the complete simulation can be observed.

Fig.5 shows the simulation result for the Wallace tree multiplier.

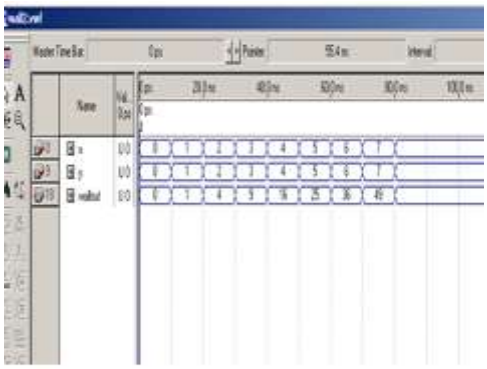

Fig.5 Simulated results of Wallace tree multiplier

5.2 MAC UNIT

The MAC unit with wallace tree is designed block wise in Active-HDL tool and VHDL code is generated form it. Simulated waveform for MAC unit with wallace tree Is shown in Fig.6. The complete circuit of MAC is described in VHDL and implemented and synthesized in Xilinx ISE 13.4 tool . The hierarchical structure is created and the complete simulation can be observed.

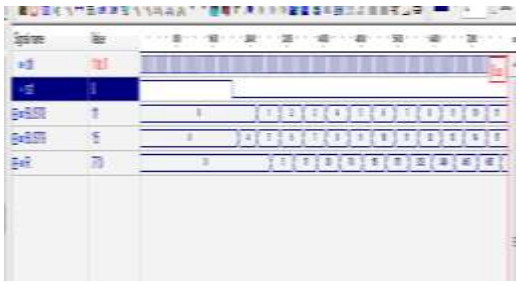

Fig.6Simulated result for MAC with Wallace tree multiplier

The RTL view of the MAC with Wallace tree multiplier is shown in Fig.7. The MAC is designed and implemented using QuartusII tool.

 ISSN: 2321-8169
239 - 243

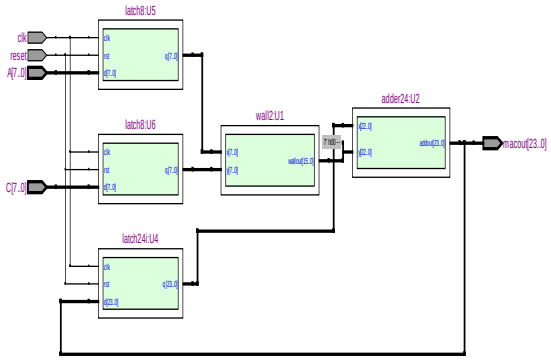

Fig. 7 RTL view of MAC with Wallace tree

5.3 MAC WITH BLOCK ENABLING TECHNIQUE

Fig.8 shows the RTL view of MAC with Wallace tree multiplier and with block enabling technique. Latches are used to unable the blocks in the MAC unit.

The control unit controls the signal flow to all the blocks as well as Wallace tree multiplier.

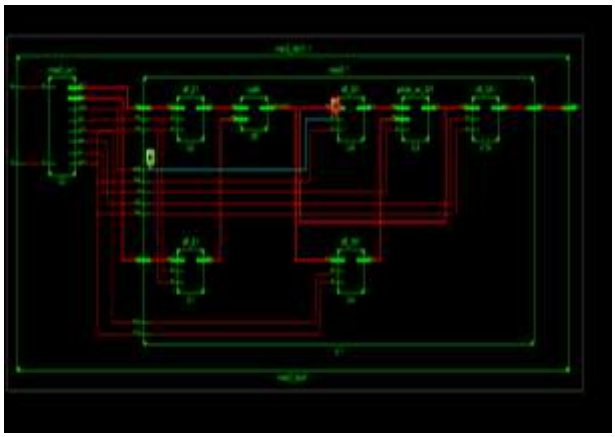

Fig.8 RTL view of MAC with Wallace tree multiplier and with Block enabling technique

5.4 MAC WITH AND WITHOUT BLOCK ENABLING TECHNIQUE

5.4.1 Timing Summary

Table 1 shows the timing analysis for MAC with and without block enabling technique. The timing analysis is performed by synthesizing VHDL code in Xilinx ISE 13.4 tool.

Table 1 Time Analysis for device XC3S1000FG320-4

Parameters	MAC Without block enabling	MAC With Block Enabling
Minimum Period(ns)	5.667	5.794
Maximum frequency(MHz)	176.460	172.592

Table 2 shows the power analysis for MAC with and without block enabling technique. From the table 2 we can say that MAC with block enabling technique is power efficient.

Table 2 Power Analysis for device XC3S1000FG320-4

Parameters	MAC Without block enabling	MAC With Block Enabling
Total Thermal Power Dissipation	71.23mW	70.84mW
Dynamic Thermal power Dissipation	0.06mW	0.05mW
Static Thermal Power Dissipation	47.36mW	47.36mW
Input/output Thermal Power Dissipation	23.81mW	23.43mW

Percentage decrease in Dynamic Thermal power Dissipation = (((0.06-.05)/0.06)*100)

= 16.66%

From the above analysis MAC with block enabling technique consumes less power by 16.66% as compare to MAC without block enabling for the device mentioned.

6. CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

As compare to MAC with conventional multiplier, MAC with Wallace tree multiplier is efficient architecture due to less delay and low power. Also when we use the block enabling technique, we find that the MAC consumes less power as compared to the MAC without block enabling technique. The main aim of our work is to achieve low power and less area. For this our proposed architecture of MAC with block enabling technique is the best option. Here we have achieved 16.66% improvement in power. The MAC designed hence optimized the digital filter structures.

The modified 8x8 bits Wallace tree has a slightly smaller critical path, a slightly larger wiring overhead but requires low power.

6.2 FUTURE SCOPE

The proposed MAC architecture is to demonstrate that, a Wallace tree multiplier can be executed efficiently with low power consumption.

Future work may consist of extending the MAC architecture to a 16-bit architecture. The change required, is simple and consists of extended number latches and 16*16 bit Wallace tree multiplier. This change is also easy to implement due to a very modular and extendible multiplier design. Another possibility for future work consists of 32-bit and 52-bit Wallace tree multiplier.

7. REFERENCES

[1] S. J. Jou, C.Y. Chen, E.C. Yang, and C.C. Su, "A pipelined Multiplier-accumulator using a high speed, low power static and dynamic full adder design", IEEE Custom Integrated circuit conference,1995,

[2] Anantha. P. Chandrakasan, Samuel Sheng, Robert W. Brodersen, "Low-Power CMOS digital design," IEEE Journal of Solid-State Circuits, Vol 27, No.-4,April, 1992

[3] Neil H.E. Weste, and David Harris, CMOS VLSI Design : a circuits and systems perspective Addison –Wesley Publishing Company, 3rd ed.

[4] Shanthala S, S. Y. Kulkarni, "VLSI Design and Implementation of Low Power MAC Unit with Block Enabling Technique", EuroJournal ISSN 1450-216X Vol.30 No.4 (2009),

[5] AkondiNarayanaKiran, G.VeeraPandu, " Hardware Efficient Vlsi Architecture Of Parallel Mac For High Speed Signal Processing Applications", International Journal of Engineering Research & Technology, Vol.1 - Issue 6 (August- 2012).

[6] TajulHamimiHarun, "High Speed 8-bits x 8-bits Wallace Tree Multiplier", Chapter 3,dspace .unimap. edu. my/bitsstream/Methodology.pdf, May 2007

[7] NiichiItoh, Yuka Naemura, Hiroshi Makino, YasunobuNakase, Tsutomu Yoshihara, and Yasutaka Horiba, "A 600-MHz 54 x 54-bit Multiplier with Rectangular-Styled Wallace Tree", JSSC,vol.36, no. 2, February 2001.

[8] K. S. Ganesh Kumar, J. Deva Prasannam, M. Anitha Christy, "Analysis of Low Power, Area and High SpeedMultipliers for DSP Applications", IJETAE, Volume 4, Issue 3,March 2014.

[9] Naveen Kr. Gahlan, Prabhat Shukla, Jasbir Kaur " Implementation of Wallace Tree Multiplier Using Compressor",IJCTA, Vol 3(3),1194-1199, June 2012.

[10] Shruti Dixit, Praveen Kumar Pandey "FPGA Implementation of Wallace Tree Multiplier using CSLA / CLA",IJSR, Volume 2 Issue 12, December 2013.

[11] Ms. V.N. Chaudhary, Prof. Dr. P.R. Deshmukh "Analysis and implementation of low power Wallace tree multiplier", ISSN: 0975 – 6779**,**VOLUME – 01, ISSUE – 02,NOV 10 TO OCT 11.

[12] StianMathiassen "Power optimized multipliers", Norwegian University of Science and Technology Department of Electronics and Telecommunications, Nov 2009.