

Phase noise Analysis of Charge Pump Phase Locked Loop (PLL) using Simulink and Design Nonlinearities

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Abstract - Designing of an analog circuit satisfying the design constraints for desired application is a challenging job. Phase Lock Loop (PLL) is an important analog circuit used in various communication applications such as frequency synthesizer, radio, computer, clock generation, clock recovery, global positioning system, etc. Since all these applications are operating at different frequency with different specified phase noise. In this paper, 'phase noise' important parameter which reflect stability of PLL system is describes and phase noise analysis for third order charge done by adding noise at different stages in loop. This paper also review of design issues and effect of nonlinearities, so how the constraints based PLL design is so challenging job is explained here and provides the design idea of PLL to designer before implementation on chip. It is suggested by using MATLAB, Simulink as a simulation tool.

Index Terms - PLL, Charge Pump PLL, phase noise, Loop Bandwidth ,offset frequency, Simulink, CAD, EDA tool.

I. INTRODUCTION

Noise is a random signal inherent in all physical components. It directly limits the detection and processing of all information results in poor performance of the system. The common form of noise is

white Gaussian due to the many random processes that make serious problems to system .For the designer it necessary to know the cause of noise and how to limit that because electronic noise is ubiquitous, present in all passive and active components, it is critical for engineers to characterize and understand how to limit noise[1][2][4].

As PLL performance is decides by its various parameter such as lock range, lock time capture range, bandwidth, phase noise etc each parameters has its important depends upon applications but the most important parameter in many higher frequency operation is 'Phase Noise' because it decides the stability of system [3][9] here this section serves an in-depth discussion on what is exactly means by phase noise, and which block in PLL creates maximum phase noise in system. The design of PLL for minimum phase noise is very difficult because phase noise of PLL has various tradeoffs between other parameters [2][4][8][9]

The section I discusses the concept of phase noise and its sources, section II what is reference spurs , section III gives measure of phase noise in Simulink and section IV and V discuss setup used for analysis of phase noise and design nonlinearities respectively.

A. Phase Noise

A perfect sinusoidal oscillator would produce an ideal sine wave

$$s(t) = A \sin(\omega t) \dots\dots\dots(1)$$

But in practice the signal always contains some noise. This can be represented by fluctuations in the amplitude of the signal(variations

in A) and by fluctuations in the signal phase (so phase becomes $\omega t + \text{phase noise}$).

In general we can represent the noisy oscillator signal as

$$s(t) = (A + a(t)) \sin(\omega t + f(t)) \dots\dots\dots(2)$$

Where: $a(t)$ represents the amplitude fluctuations in the signal $f(t)$ represents the phase fluctuations or the phase noise.

Well-designed signal sources have small amplitude noise. Amplitude noise can also be removed using automatic level control (ALC) systems, or by passing the signal through a limiting amplifier. Amplitude noise is also rejected to some degree by many of the mixers used in radio systems. Phase noise is another matter. Once present on a signal it is very difficult to remove, and as will be explained later its measurement, it can have a major impact on system performance.

Assuming that the signal contains only phase noise and so is of the form

$$s(t) = A \sin(\omega t + f(t)) \dots\dots\dots(3)$$

In the time domain, if the signal $s(t)$ was viewed on an ideal oscilloscope, the effect of $f(t)$ would be to cause timing jitter

(time domain phase error) on the zero crossings of the waveform.

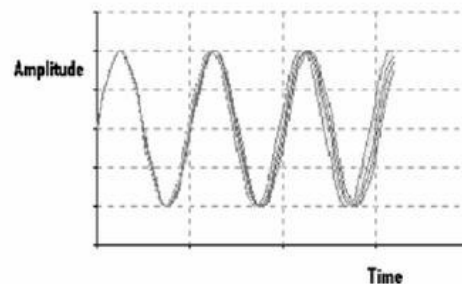


Figure:1 Signal with very bad phase noise

This timing jitter can be significant in many applications, for example if $s(t)$ is used as a data clock in a digital transmission systems, the timing jitter could cause erroneous data sampling [11]. This is not the major concern to radio engineers, the phase noise usually has to be severe (as in Figure:1) to cause significant timing errors. Levels of phase noise that are far too small to detect on an oscilloscope can cause changes to the spectrum of a signal that can be very important in radio applications. Such minute amounts of phase noise on a transmitter signal can result in the transmitter causing significant interference to other services, whereas minute amounts of phase noise on a receiver local oscillator can severely reduce the receiver selectivity or cause other undesirable effects. These effects are of major concern to radio or wireless applications.

Basically, Phase noise is random variation of phase of the signal. It is the frequency domain representation of rapid, short term fluctuations in the phase of the wave, caused by time domain instabilities (“jitter”). Generally the phase noise and jitter are closely related. Or more specifically, it is call as phase noise, but in digital system, it is call as jitter of the clock. [2][3][9]

As phase noise can also be characterized in the frequency domain. An ideal sine wave in the time domain corresponds to an ideal impulse in the (single sided) frequency domain, as shown in Figure.2 (a)

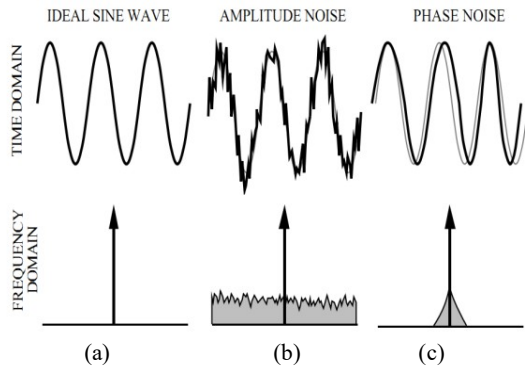


Figure:2 Clock jitter in time and frequency domains.

Consider the spectrum of an ideal sine wave with additive white noise, shown in Figure2 (b),(c).The noise adds uncertainty to the measurement of the zero crossings of the waveform.

Phase noise is very much concern in PLL, since it directly affects the entire performance of the system so Phase noise is the major problem in PLLs, especially when the system operating frequency increases rapidly in recent years. The major noise sources of phase noise in the charge-pump PLL include an external reference input noise, VCO internal noise, phase detection noise, and VCO control voltage noise [3] etc. The external reference signal always on trains noise generated from a number of sources such as the thermal noise, crosstalk, short noise, and so forth. When noise is present in the signal waveform, the timing information is severely obscured. Additive White Gaussian Noise (AWGN) is a term to refer to the fact that noise eventually combines with the desired signal and is a major limiting factor in the transmission of information.

Following are the common sources of phase noise in PLL. [9][18] [19][22]

- 1) **Oscillator noise:** Practically, there are two oscillators that contribute to the phase noise of the PLL. One is the reference oscillator and other is the VCO. Although both oscillators can be modeled similarly, their effects on the output noise are distinct just due to their position in the loop.
- 2) **Phase detector noise:** Usually phase detectors are not major sources of noise in PLLs. As the work of PD is to detect the phase difference, any random variation in the phase of input signal makes the phase detector to produce wrong output, which is get transferred through filter and tunes the VCO wrongly.
- 3) **Frequency Divider noise:** In a PLL, this noise directly appears at the input of phase detector and experiences the same transfer function as the noise on the input terminal.

II REFERENCE SPUR

Reference spurs are spurious emissions that occur from the operating frequency (f_0) at an offset frequency. Reference spurs are a serious issue in RF systems because it can degrade the signal-to-noise-ratio in reception and transmission. This spur is caused by

non-idealities in the PFD and charge pump circuits. These non-idealities are usually caused by leakage and mismatch in charge pump of PLL. Though there is no phase difference between reference and feedback signal, in the locked state, the phase detector (or phase frequency detector) produces very narrow pulse width error voltage which drives the charge pump. Although these pulses have a very narrow width, the fact that they exist means that the dc voltage driving the VCO is modulated by a signal of frequency equal to input reference frequency. This produces reference spurs in the output occurring at offset frequencies that are integer multiples of input reference frequency. In Simulink a FFT spectrum analyzer used can be used to detect reference spurs easily [6]. The frequency spectrum of distorted VCO output with spurs is shown in figure:3

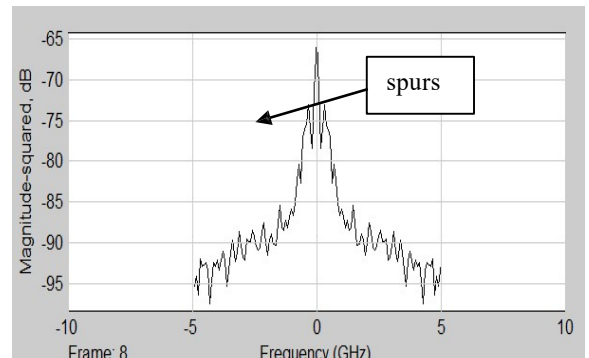


Figure:3 Spectrum output with reference spurs

III. PHASE NOISE MEASUREMENT

Some oscillators have phase noise levels that are mention in their specifications. Any high quality signal generator will have the level of phase noise specified, as do many high performance crystal oscillators used as standards. Their performance is generally specified in dBc/Hz and at a given offset. The term dBc simply refers to the level of noise relative to the operating point i.e. -10 dBc means that the level is 10 lower than the operating frequency [3][8][9]

The bandwidth in which the noise is measured also has to be specified. The reason for this is that noise spreads over the frequency spectrum. Obviously the wider bandwidth that is used, the greater the level of noise that will pass through the filter and be measured. It will rise for a wider bandwidth and fall when a narrow bandwidth is used. Technically the most convenient bandwidth to use a 1 Hz bandwidth and so this is used. When measuring this wider bandwidth is usually used because it is difficult to obtain 1 Hz bandwidth filters. Finally the level of noise varies at different offsets frequency from the operating frequency. The level of phase noise decreases as the offset from the operating frequency increases.

To measure phase noise the equation (4) [3][9][8] is used and obtained by measuring operating frequency power level in decibel and spur's /SSB power levels,

$$Sc(f) = P_s - P_{SSB} \dots\dots\dots(4)$$

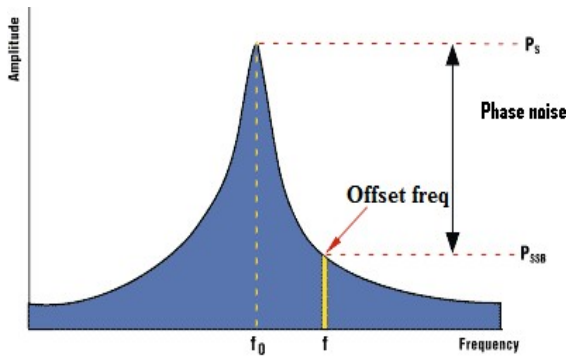


Figure:4 Phase noise measurement

Above spectrum is double sided so it is denoted by $S_c(f)$ but if it is single sided then denoted by $L(f)$ both are express in dBc/Hz [9].

IV SETUP FOR PLL PHASE NOISE ANALYSIS

The setup made in Simulink for phase noise analysis of charge pump PLL is shown in figure 5 by considering one of widely used application such as frequency synthesizer with input or reference frequency equal to 450MHz, frequency divider $N=10$ and second order filter components $R_1=24\text{KHz}$, $C_1=2\text{Pf}$ and $C_2=0.002\text{Pf}$ As shown figure 5, PFD block followed by charge pump assembly and loop filter consist of R_1 , C_1 and C_2 combine in one clock with input supply 3.3 Volts. The analog VCO was used to get low phase noise and VCO block parameters are VCO gain (K_{vco}) as 165.15 MHz/volts, quiescent frequency is 450MHz keeping amplitude and phase are 1 and $\pi/2$ respectively and charge pump current is $100\mu\text{A}$.

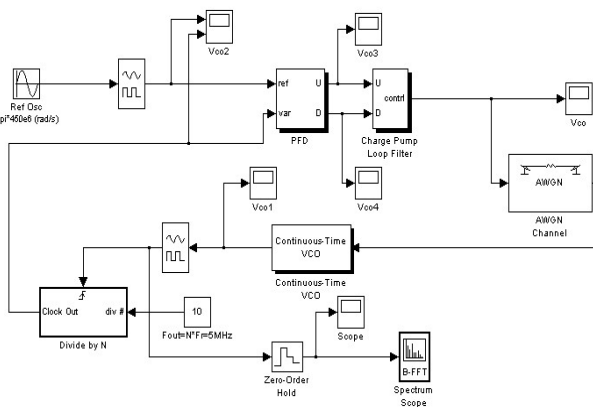


Figure: 5 Simulink model of third order PLL with noise

To measure phase noise of PLL system FFT spectrum scope is used and connected at VCO output through zero-order hold with sample time $0.1e-9$, from the output scope the power levels of operating signal and SSB are measure to give phase noise of PLL in dBc/Hz . Its can gives two sided spectrum or one sided spectrum. The effect on phase noise and spurs levels are studied by adding AWGN noise at different stages in loop that is at reference stage called ref noise, before VCO block and phase detector noise is introduced by transport delay of $10e-12$ ps in signal path.

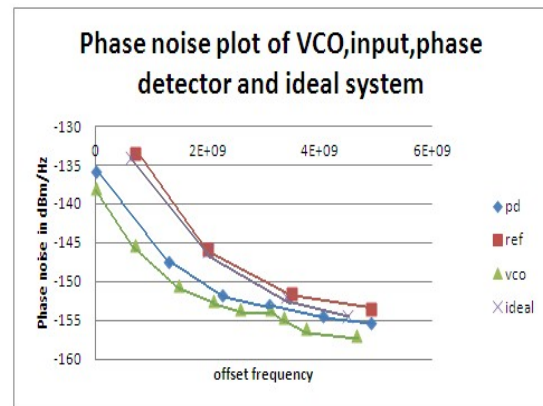


Figure:6 Phase noise plot considering all

Figure:6 shows the phase noise plot for considering all noise effect so from graph it is clear that the VCO noise more dominant than other noise and table 1 provides phase noise calculated values for different stages at specific offset frequency

Table:1 The Phase noises at different stages at offset frequency

VCO	PD	Ref	Ideal
-138@ 300MHz	-135.9@ 400MHz	-133.5@ 700MHz	-134.8@ 620MHz
-145.37@ 700MHz	-147.4@ 1.3GHz	-145.8@ 2GHz	-146@ 2.63GHz
-150.5@ 1.485GHz	-151.8@ 2.25GHz	-151.5@ 3.5GHz	-151.9@ 3.4GHz
-152.5@ 2.1GHz	-153.1@ 3.1GHz	-153.5@ 4.9GHz	-154.9@ 4.5GHz
-153.5@ 2.58GHz	-154.4@ 4.06GHz	.	.
-153.6@ 3.125GHz	-155.4@ 4.9GHz	.	.
-154.6@ 3.35GHz	.	.	.
-156@ 3.37GHz	.	.	.
-157@ 4.65GHz	.	.	.

From the table: 1 it is clear that VCO noise is greater than other noise effect and it also has more spurs levels and FFT spectrum output for VCO noise shown in figure 9. In order to have low phase noise then loop bandwidth is important parameters of PLL system [3][22] which to be increases because loop bandwidth will act as threshold for VCO noise. Basically loop BW is measured on scope as frequency from operating frequency to the first spurs level from onward VCO noise is begins as shown in figure 7. The loop BW will get affected by the noise at different stages shown in table 2. So the noise added at different stages in loop will significant effect on loop bandwidth. The VCO noise has less loop bandwidth therefore more are spurs created.

Table:2 The effect on loop bandwidth

Noise at different stages	Loop Bandwidth
VCO noise	300 MHz
PD noise	400 MHz
Ref noise	700 MHz
Ideal system	720 MHz

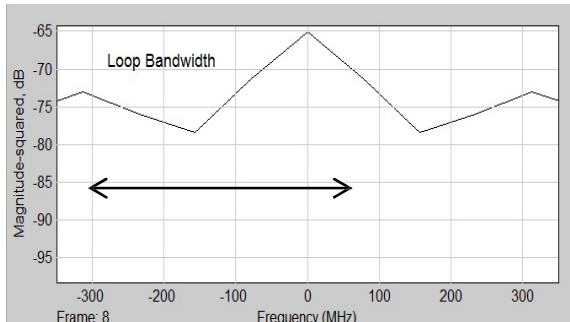


Figure:7 Loop bandwidth measurement of PLL

The figures 8-11 shows the output of FFT spectrum for the different phase noise for considering noise at different stages in loop and corresponding calculation for their phase noise by measuring power levels of operating frequency and spurs levels.

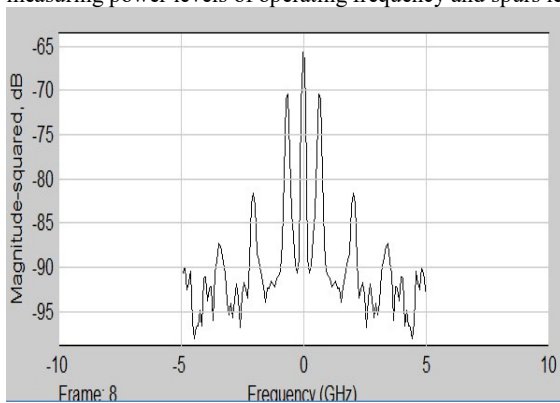


Figure:8 spectrum scope output for system without noise

From figure 8. The phase noise obtained for ideal system is -70.4(power level of signal power)-64.4(power level of spurs)=-134.8 dBc/Hz@620MHz offset frequency.

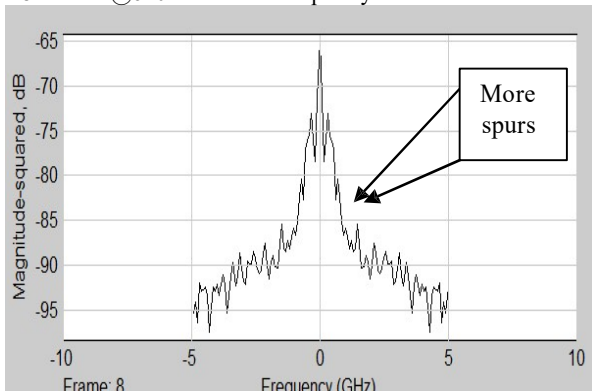


Figure:9 Spectrum scope output for system with VCO noise

From figure 9 the phase noise obtained for VCO noise is -65(power level of signal power)-73(power level of spurs)=-138 dBc/Hz @300MHz offset frequency for this case the number of spurs are more at different offsets frequency and first spur is more below the reference peak which indicates more phase noise.

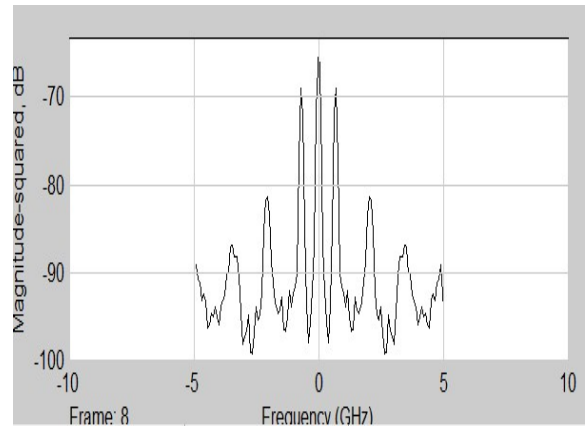


Figure:10 spectrum scope output for system with reference noise

From figure 10 the phase noise obtained for reference output is -69(power level of signal power)-64.5(power level of spurs)=-133.5 dBc/Hz @700MHz offset frequency.

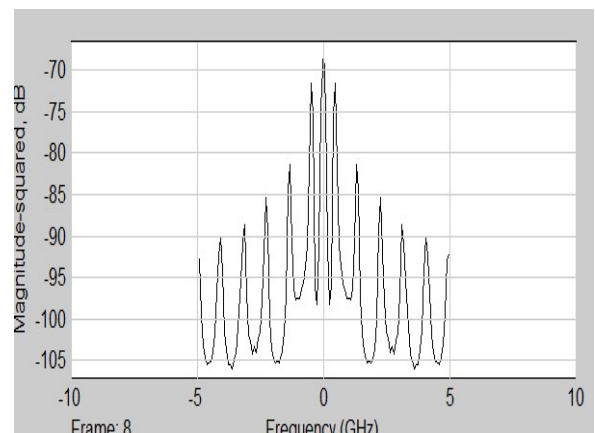


Figure:11 spectrum scope output for system with PFD noise

The figure 11 shows the phase noise obtained for PFD noise is -71.4(power level of signal power)-64.5(power level of spurs)=-135.9 dBc/Hz .This case also shows more spurs but at specific offset frequency whereas in VCO noise spectrum spurs available at all possible offset frequencies. Now considering application where PLL use for in microprocessor to provide reference clock on chip[20][21] then the effect on phase noise due to jitter at input providing by transport delay block between reference oscillator and PFD. The spectrum scope are shown figure 12 and figure 13 with delay and without input delay and corresponds to input jitter provide respectively and phase noise plot for this cases given in figure 14.

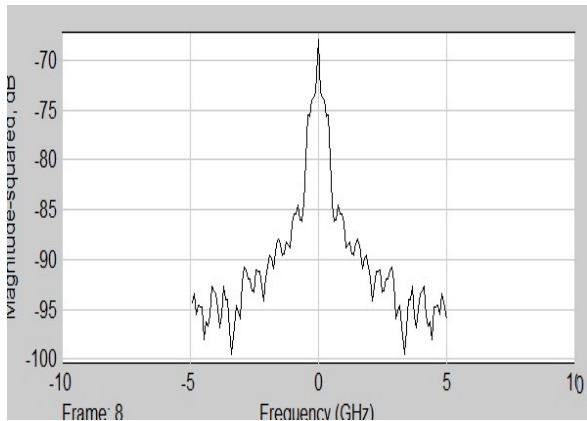


Figure:12 Spectrum scope output for system with input Delay 10e-12

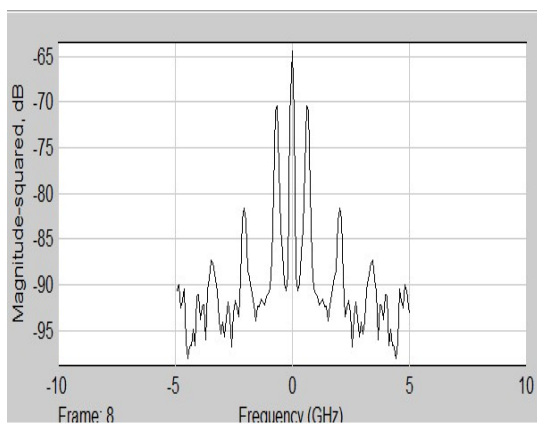


Figure:13 spectrum scope output for system without input Delay

The table3 shows the phase noise measurement for with and without delay input clock jitter

Table:3 Effect on Phase noise for with and without delay

Offset freq	without i/p delay	with i/p delay
200MHz	-134.8	-138
700MHz	-146.2	-150.06
3.4GHz	-151.9	-153.6
4.85GHz	-154.4	-157.37

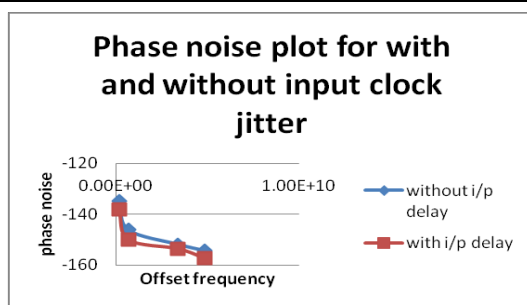


Figure:14 Phase noise plot for with and without clock jitter

Phase noise plot shown in figure 14 implies that the phase noise will get affected due to input jitter.

V DESIGN NONLINEARITIES

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The tradeoff involved in the design of PLL for specified application can be summarized in the “RF design hexagon” shown in figure 15 where almost any two of the six parameters trade with each other to some extent.[18]

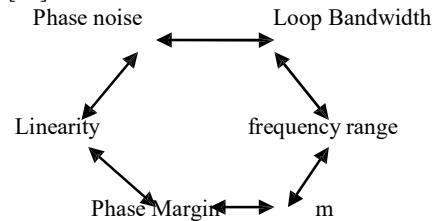


Figure: 15 PLL design hexagon

The key point here is that, while digital circuits directly benefits from advances in IC technologies but RF circuits do not as much. In particular figure of merit used for individual devices fail to predict the performance of circuits

Most wireless communication applications have tight jitter specifications on the transmitted and received sides. These specifications make it possible to design the transmitter independent of the receiver. These jitter specifications must be considered carefully in choosing the best PLL for the application.

When selecting PLLs for ASIC applications [5] it is important to understand the tradeoffs between different PLL features. Many of these features tradeoff directly with the PLL’s jitter performance. The PLL loop bandwidth and the type of VCO are the biggest factors impacting output jitter. The most flexible designed PLLs for a given application is the requirements in today’s market scenarios [10][13][14]. Designing constraint based PLLs is very challenging since a number of performance metrics have to be taken into account simultaneously such as stability and reference spurs. The design is complicated because these metrics are not independent of each other; an improvement in one effect results in degradation in the other so designer should have to take care of all aspects because of these tradeoff between PLL parameters the best PLL design cannot be possible.

This paper explain the design aspect of monolithic PLL for the constraint as low phase noise ,as there are various tradeoff involved such as by increasing loop BW the phase noise [3][7][can be limited that can be achieved by three levels. These levels are level 1 is transfer function ie in terms of damping factor or natural frequency .The level 2 is PLL parameters like frequency range, settling time and level 3 is stability issue in terms of phase margin as shown in figure 16

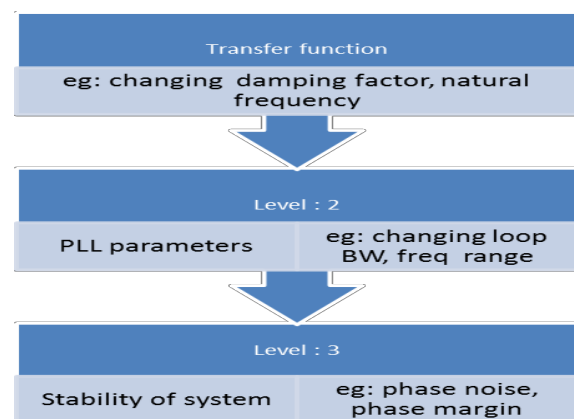


Figure: 16 PLL design Levels

the figure 17 shows the combine effect on phase noise by increasing any one PLL parameters like settling time, loop BW, Phase margin .This result implies phase noise effect is random.

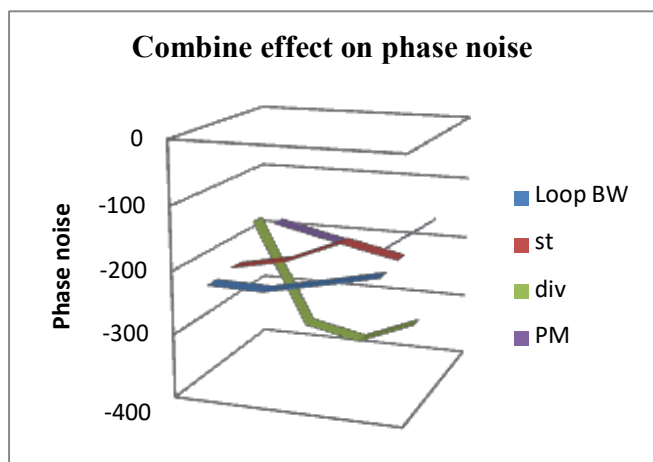


Figure 17 The combine effect on phase noise

Similarly if the effect on phase noise and loop BW for keeping any two parameters constants as shown in figure 18 and 19. Where the frequency range of PLL is changing and two parameters such as phase margin and m constant. The graphs are obtained for series of Phase margin of 80,70,50,30 and corresponding m are 0.0019,0.0321,0.1527 and 0.5 respectively.

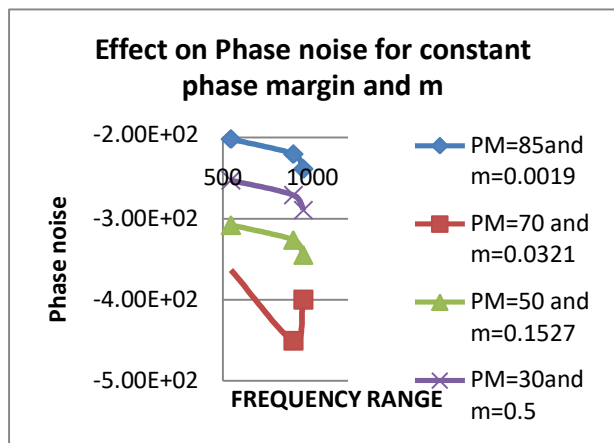


Figure 18 The effect on phase noise for constant m and phase noise

This random effect on phase noise shows that so many nonlinearities are coming on the way of design low phase noise[17] PLL. This gives the idea about real design challenges. So the designer should have take care of all the dependent aspects to make best design. The Simulink tool effectively helps to provide design idea[12]

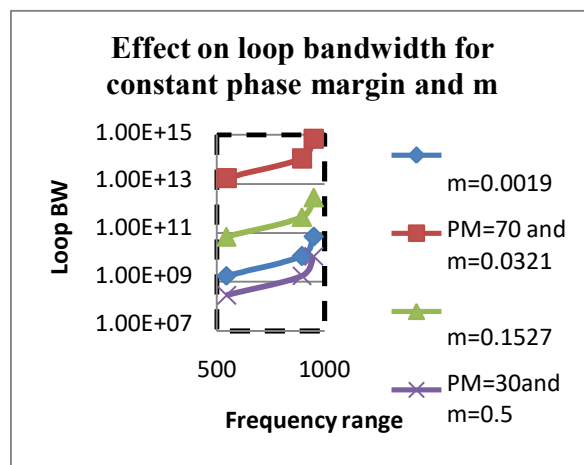


Figure 19 The effect on loop BW for constant m and phase noise

VI. RESULT AND CONCLUSION

Simulated output gives VCO phase noise $-64.4\text{dB}-70\text{dB}=-138\text{dBc/Hz}@300\text{MHz}$ offset frequency which is higher than other phase noise effect also affect the loop bandwidth this shows there is tradeoff between low phase noise and loop bandwidth. From the phase noise plot it is concludes that the phase noise effect is different for different PLL applications. For the design so many nonlinearities are becomes obstacles to make flexible PLL design.

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