National Conference on Science, Engineering and Technology (NCSET – 2016)
Volume: 4 Issue: 6
ISSN: 2321-8169
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Performance Analysis of PWM Control of Three-Phase Boost-Derived Hybrid Converter

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Abstract—This paper proposes a power converter architec-ture which can provide a step-up dc and a three-phase ac output simultaneously from a single dc input in a single-stage conversion. This architecture, named three-phase boost-derived hybrid converter (3- BDHC), is derived from a conventional boost converter by replacing the control switch with a three-phase bridge network. Compared to conventional voltage source inverters, the 3- BDHC topology has inherent shoot-through protection capability and continuous input current. Since the boost and the inverter functions are integrated within a single architecture, the power processing density of the overall system is higher and the coordination of power flow into two different outputs becomes easier. Both the step-up dc and the three-phase ac outputs can be independently regulated. In addition to a conventional 3- BDHC, this paper also describes the 3- BDHC topology where the neutral of the three-phase filter is connected to the split-dc output capacitor. This split-dc capacitor arrangement allows for independent control of each of the three-phase voltages at unbalanced load conditions. A suitable pulse-width-modulation (PWM) control strategy for the purpose of regulation of each of the outputs (dc and ac) has been described. Experimental results have been shown to validate the converter operation, when a single dc input provides a step-up dc and a three-phase ac using a 150 W experimental prototype; the ac output is generated at fundamental frequencies of 50 Hz and 400 Hz.

Key words:*3-BDHC,SPWM,CFST-SPWM*

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I. INTRODUCTION

More-electric power distribution architectures are charac-terized by ac and dc loads connected to the same system. Typical examples include aircraft power distribution [1], hy-brid electric vehicle [2], dc Nanogrid [3], hybrid fuel-cell and inverter system [4], etc. In most of these systems, in addition to the primary power conversion, auxiliary systems need to be powered up for effective operation of the overall system [4]. Multi-output converter topologies are often used in most of these cases. When both dc and ac loads are present, conventionally many dc-dc power converters or a multi-output dc-dc converter is used; voltage source inverter (VSI) stages are cascaded to dc-dc converters to provide ac output. Fig. 1 shows a representative schematic of a multi-output architecture. Here, a single dc input is interfaced to dc and ac outputs using a multi-output dc-dc stage (Stage 1) and a VSI (dc-ac) stage . The same system can be realized using a hybrid-converter topology, which provides dc and ac outputs simultaneously using an integrated architecture. Hence, the hybrid converter (Stage 2), shown in Fig. 1, reduces the overall

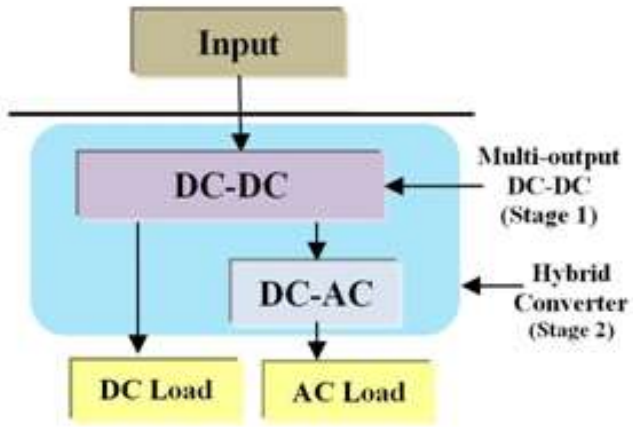

Fig. 1. Concept of hybrid-converter topology.

number of power conversion stages and results in increased power processing density. Also, since power conversion stages are integrated in a single architecture, the coordination control system for power flow management becomes centralized.

The contributions of this work are as follows: A hybrid-output converter topology has been presented which can simultaneously provide a dc and a three-phase ac output from a single dc input. This topology has been derived from a conventional boost converter, and is denoted as three-phase boost-derived hybrid converter (3- BDHC) in this paper. Unlike conventional VSIs, the 3- BDHC topology uses the shoot-through state of the inverter legs to generate boost-action for generation of the step-up output. Both the outputs (dc and ac) of the proposed 3- BDHC can be regulated independently. A single-phase BDHC, based on the same circuit modification principle, has been reported in [5]. This paper extends the concept to a three-phase system. The major focus areas of this paper are:

1) to study two different 3- BDHC architectures: (a) a conventional 3- BDHC, and (b) a 3- BDHC topology where the neutral of the ac filter is connected to the mid-point of a split-dc output capacitor. The second configuration enables independent control of each of the three ac output voltages at unbalanced load conditions.

2) As the operations of boost and 3- inverter are inte-grated, conventional 3- sine PWM (SPWM) strategy

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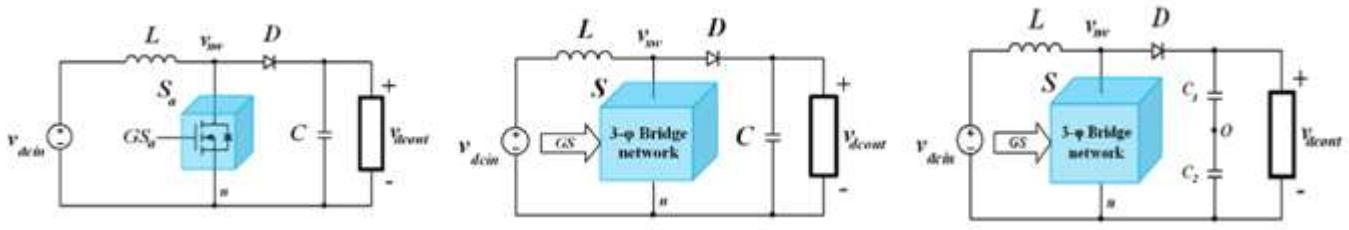

(a) (b) (c)

Fig. 2. Derivation of 3- BDHC topology from a conventional boost converter. The switch S_a of boost converter in Fig. 2 (a) is replaced by the 3- bridge network in Fig. 2 (b). Fig. 2 (c) shows the circuit modification with split-dc output capacitor.

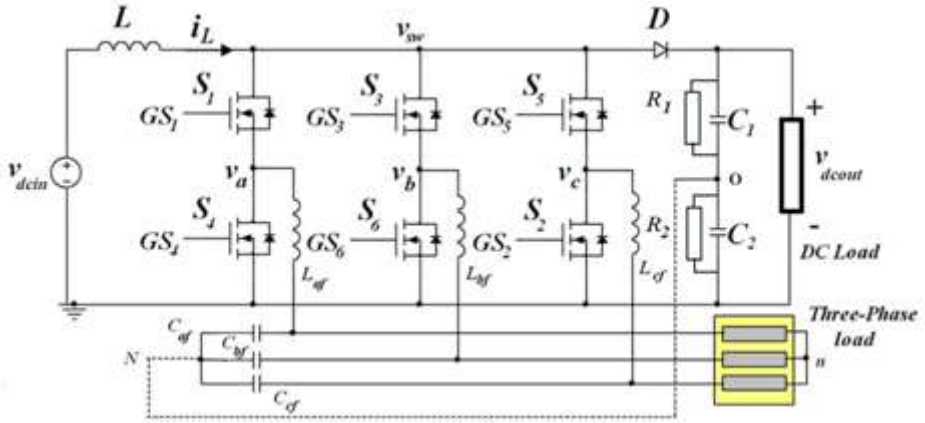

Fig. 3. Three-phase boost-derived hybrid converter (3- BDHC) topology.

cannot be used to modulate the proposed topology. This paper describes a modified SPWM control scheme hav-ing a constant frequency shoot-through interval (called CFST-SPWM in the paper). The implementation of the modified CFST-SPWM scheme has been shown in this paper.

3) Simulation verifications and experimental results are given in this paper to validate the behavior of the 3-BDHC. The proposed converter, operated at 10 kHz switching frequency, can provide a dc and 3- sine ac outputs at 50 Hz and 400 Hz.

The paper is organized as follows: The following section describes the derivation of the 3- BDHC topology from a conventional boost converter. Section III shows character-ization of the topology. A control methodology has been described in Section IV. Section V shows a comparison of the topology with conventional converters. Experimental results in Section VI validate the operation of the converter behavior. Section VII concludes the paper.

II. DERIVATION OF THREE-PHASE BOOST-DERIVED HYBRID CONVERTER

Fig. 2 (a) shows a conventional boost converter with the control switch S_a. The three-phase hybrid converter can be derived from the boost converter by replacing the switch S_a by a three-phase bridge network as shown in Fig. 2 (b). The resulting topology can be used to provide dc and 3- ac outputs. The generalized schematic of the 3- BDHC topology has been shown in Fig. 3. The switches (S_1 S_6) replace the control switch of the conventional boost converter, and are used to control both the dc and the ac outputs. The ac filter capacitors C_{af} , C_{bf} , and C_{cf} are connected to the star-point 'N', while the load neutral is 'n'. C_1 and C_2 are used for dc output capacitors, with the mid-point denoted by 'O'. In this paper, two different BDHC architectures have been considered: (a) conventional three-phase BDHC, where the loads are star-connected and the load and the filter star points are connected (i.e. points 'N' and 'n' are connected), and (b) Split-dc output capacitor-based BDHC, where 'N' is connected to 'O'. The split-capacitors have bleeder resistors in order to ensure equal voltage sharing. The magnitude of these resistors R_1 and R_2 are high (in the order of k), and for analysis their effects on the overall circuit operation have been neglected. The following section describes the steady state behavior of the conventional BDHC.

III. STEADY STATE OPERATION

A. Operating Principle of conventional 3 BDHC

The six switches of 3 BDHC regulate both the ac and the dc outputs. Depending upon the states of the switches, the converter operates through three distinct intervals, during each switching cycle. The equivalent circuits for each of the three distinct intervals of a conventional 3 BDHC have

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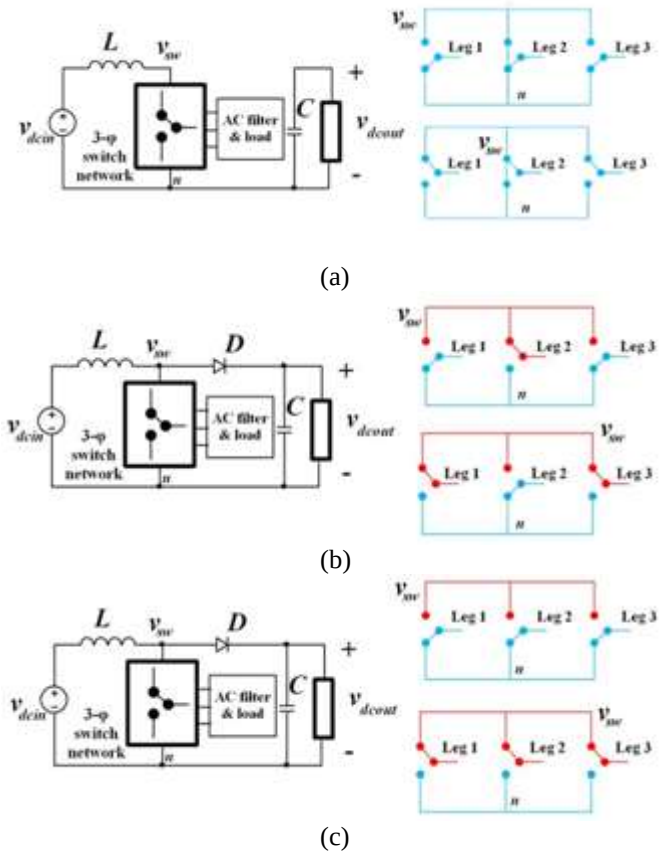

Fig. 4. Operating intervals of the 3 BDHC, (a) Shoot-through Interval,

(b) Power Interval, and (c) Zero Interval. Legs 1, 2 and 3, shown in the right of each figure, can be any one of phase legs 'a', 'b' or 'c'.

been shown in Fig. 4. The switching signals for the converter have been shown in Fig. 7. For the entire analysis, continuous conduction mode of operation is assumed. The operating intervals of the proposed converter are described below:

1) Interval I: Shoot-through (ST) [(t_9 t_0) and (t_4 t_5)] [Fig. 4 (a) and Fig. 7]

Depending upon the magnitude of the phase voltage, both the switches of a particular leg are 'on'. The duration of this interval, defined as 'D_{st}', regulates the step-up dc output. This interval is analogous to the control switch of a boost converter being 'on' and the diode D is reverse biased. For a conventional VSI, this switching state is forbidden. It should be mentioned here that the shoot-through interval can be achieved by having both switches of either any one or two or all the legs turned 'on'. In this work, we are turning 'on' a single leg to achieve shoot- through.

2) Interval II: Power (P) [(t_1 t_3) and (t_6 t_8)] [Fig. 4 (b) and Fig. 7]

During this interval, the 3 ac output receives power from the source. Any two top or bottom switches and the opposite switch of the remaining leg is on. The diode D conducts during this interval, and a part of the current flows to the ac side. The switch node voltage v_{sw} gets clamped to the output dc voltage during this interval and acts as the input to the VSI (assuming continuous conduction mode operation). This operation interval is different from a conventional boost converter, because the current through the diode D is a function of the inductor current i_L and the current drawn by the bridge network.

3) Interval III: Zero (Z) [(t_0 t_1); (t_3 t_4); (t_5 t_6) and (t_8 t_9)] [Fig. 4 (c) and Fig. 7]

During this interval, either all top or the bottom switches are on. The current in the inductor L is discharged through the diode D during the interval.

From the above switching states we see that shoot-through interval is inserted within the Zero interval of a conventional three-phase uni-polar SPWM switching scheme. This modification does not alter the output ac voltage expression for the ac output when compared to a conventional three-phase VSI. The main reason for this is that, during the zero intervals, the DC voltage of input to the inverter is not applied to the bridge, and the input current is zero. Compared to a conventional VSI, the input to the inverter is a square wave, with the non-zero value applied during the power interval. Thus, the dc-ac conversion of the 3 BDHC is same as a conventional 3 VSI, and operations of the VSI and the boost converter can be integrated in the same architecture. Also, unlike a conventional VSI where the input current is discontinuous, the input current to the 3 BDHC is continuous and the discontinuous input current to the bridge is sourced from the inductor current i_L.

B. Steady-State Analysis

The analysis of the conventional three-phase BDHC topology in steady state assumes continuous conduction mode of operation. This means that the diode current never becomes zero during 'Power' and 'Zero' intervals. For a duty of D_{st}, the step-up dc voltage is related to the input dc by relation

(1).

$$\frac{V_{dcout}}{V_{dcin}} = \frac{1}{1 \; D_{st}} \qquad (1)$$

Considering the modulation index to be M_a, the rms value of the line-to-line output ac voltage can be expressed as shown in relation (2).

$$\frac{V_{acout}}{V_{dcin}} = 0{:}612 \quad \frac{M_a}{1 \; D_{st}} \qquad (2)$$

From relations (1) and (2), we can conclude that the dc output is dependent only upon the duty cycle D_{st}, while the output ac voltage is dependent upon both D_{st} and M_a. For the purpose of regulation, if the variation of duty is assumed to be small compared to the modulation index, then we can have independent control of both the outputs. Since, the BDHC has an additional three-phase ac output; the magnitude of the input current is greater than that of a conventional boost converter as given by (3).

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$$^{I}dcin = {}^{I}L = \frac{^{V}dcout\,^{I}dcout + {}^{3V}ph\,^{I}ph\,^{cos}}{^{V}dcin} \quad (3)$$

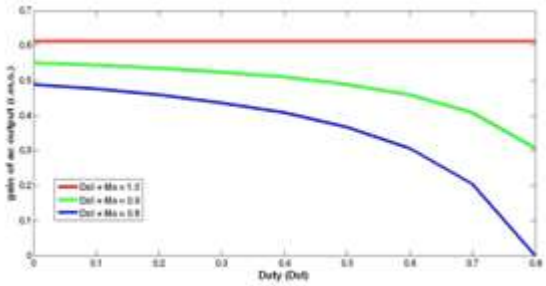

Fig. 5. Output ac voltage gain (r.m.s.) of the 3 BDHC topology with varying duty cycle.

where, V_{dcout}, I_{dcout} are the dc output terminal voltage and current, V_{ph}, I_{ph} and are the ac output terminal phase voltages, phase currents and load power factor angle, respectively.

Relations (4) and (5) show the expressions for dc and ac output power for the converter. Here, the loads at the dc and ac outputs are considered purely resistive, and equal to R_{dc} and R_{ac}.

$$^{P}dc = \frac{V^{2}_{dcin}}{R_{dc}\ (1\ D_{st})^{2}} \quad (4)$$

$$^{P}ac = \frac{3m^{2}\ V^{2}_{a\ dcin}}{4R_{ac}\ (1\ D_{st})^{2}} \quad (5)$$

It has to be noted that both the dc and ac outputs are reg-ulated using two control variables within the same switching period. Hence, for independent control of each output, relation
(6) must be satisfied.

$$m_a + D_{st} \quad 1 \quad (6)$$

For the condition of equality of relation (6), the rms value of the output ac voltage is equal to 0:612 V_{dcin}. This is equal to that achieved using a single 3-phase VSI topology. Fig. 5 shows the variation of ac output gain for different equality relations of (6). The 3 BDHC operates in continuous conduction mode of operation so long as the diode current i_D remains non-zero during Power interval. This can be achieved if relation (7) holds true.

$$^{bi}l_{xf}\ jx=a;b;c\ \ ^{i}L \quad (7)$$

where $^{b}i_{lxf}$ is the peak value of the current through any of the ac filter inductors. The proposed converter is derived from a uni-directional boost converter and hence, the load at the output cannot be zero. Also, the operation of the 3 BDHC requires that the switch-node (v_{sw}) be clamped to the output dc voltage (v_{dcout}) during power interval. This is possible when the converter operates in CCM operation, satisfying relation

(7). The converter can however be operated with no ac loads; the switches can only be used to perform the step-up operation (m_a = 0).

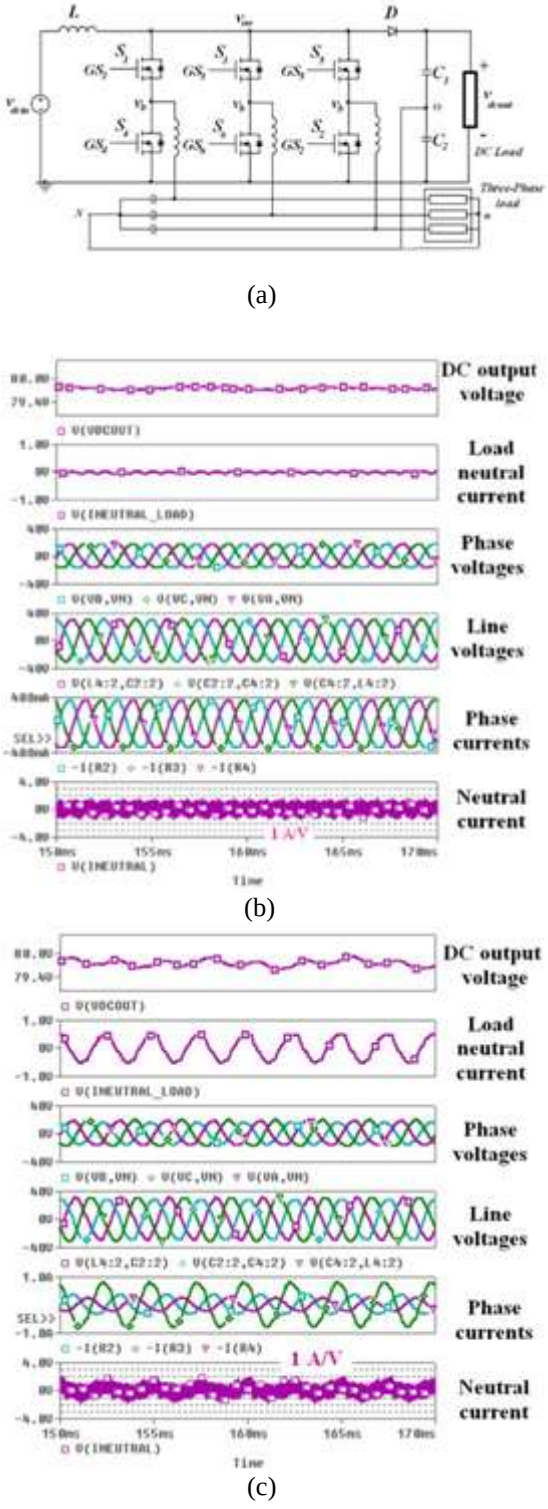

Fig. 6. (a) Schematic of split-dc capacitor-based 3 BDHC. Simulation of its steady-state operation when subjected to (b) balanced loads of $R_a = R_b = R_c = 50$ each, (c) unbalanced loads of $R_a = 50$, $R_b =$
20 , and $R_c = 80$. The dc-output voltage (v_{dcout}), line and phase output voltages, phase currents, and neutral current have also been shown.

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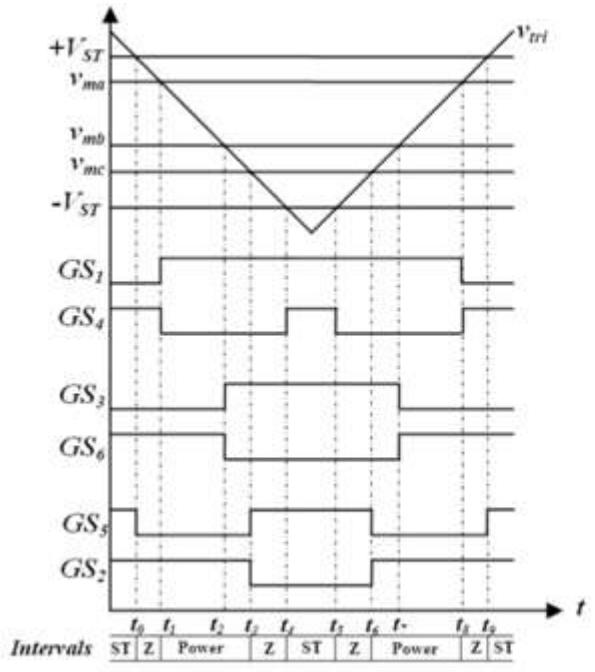

Fig. 7. CFST-SPWM based gate switching waveforms for the 3 BDHC circuit for the 3 BDHC topology.

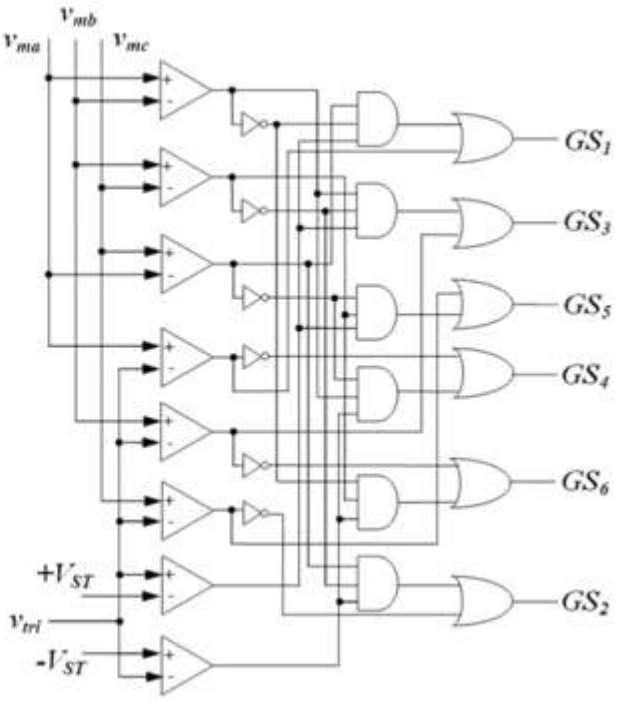

Fig. 8. CFST-SPWM Generation

C. Split-dc output capacitor-based BDHC

For a split-dc output capacitor-based BDHC, shown in Fig. 6 (a), the neutral of the load is connected to the mid-point of the output dc capacitor. The principle of operation of this converter is similar to a conventional split-capacitor four-wire three-phase inverter, whenever relation (7) is satisfied. In this configuration, all the three phases can be independently regu-lated even in the presence of unbalanced loads (even when the load neutral is not connected to the ac-filter star point) since the circuit configuration is equivalent to three separate half-bridge inverters. The neutral wire connects the load neutral 'N' to the mid-point of the output dc capacitor 'O'. When the ac loads are balanced, the neutral wire carries currents at the switching frequency of the converter.At unbalanced loads, the neutral carries the zero sequence component of the load currents in addition to switching frequency components. This has been verified using simulation results shown in Fig. 6 (b) and Fig. 6 (c). From simulation, it is clear that with higher degree of unbalance in the ac-loads, the ripple in the output dc voltage increases.

IV. CONTROL SYSTEM ARCHITECTURE

This section describes a suitable control scheme for the purpose of regulation of ac and dc outputs of the 3 BDHC. This switching scheme can be applied to both the topologies studied in this paper. The CFST-SPWM control strategy is based upon the control scheme proposed in [6]. In this scheme, depending upon the relative magnitudes of the phase voltages, the shoot-through interval is executed by any particular leg. Fig. 7 illustrates the behavior of this scheme for the condition when the reference for the phase voltages are related as
$v_{ma} > v_{mb} > v_{mc}$. In this condition switches (GS_1; GS_4) and (GS_5; GS_2) perform the shoot-through operation. Fig. 8 shows the schematic for realization of the PWM control signals for the proposed converter. The PWM control circuit requires five references: v_{ma}; v_{mb}; v_{mc} which regulate the ac output, and $+V_{ST}$, and V_{ST} , which regulate the dc output voltage. The PWM control has been implemented using ePWM modules [7] of TMS320F28335 digital signal processor.

V. ADVANTAGES OF THE TOPOLOGY

The advantages of the 3 BDHC can be listed below:

1) The converter topology has an inherent shoot-through protection because of the fact that having both the switches of any particular leg 'on' is a valid switch-ing state. Hence, converter is immune to EMI-induced misgating 'on' of any of the switches.

2) For a conventional VSI, dead time is required and this causes distortion of the output ac voltage. Dead-time compensation circuits have been used for this purpose

   [8]. For the proposed converter, dead time need not be implemented.

3) Since, both the boost and VSI topologies have been integrated in a single architecture, the power processing density increases. Due to the integrated nature, control of power flow becomes easier. Also, the topology reduces the total number of switches and gate drivers.

4) The topology can provide dc as well as a three-phase ac simultaneously. The ranges of output for ac as well as dc outputs are same as that of a boost converter as well as a VSI.

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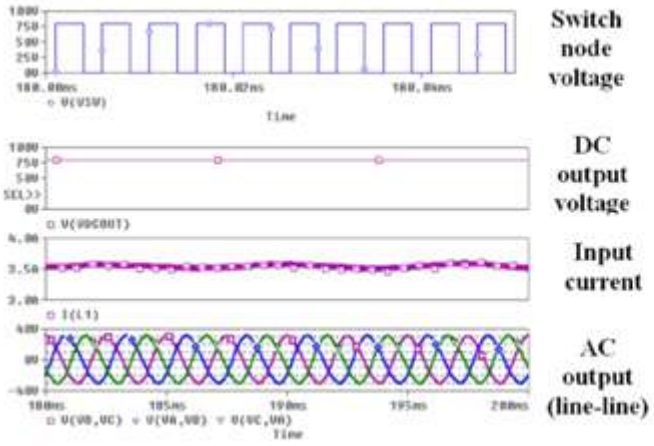
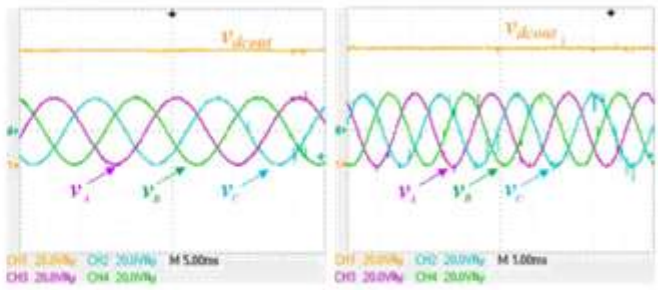


Fig. 9. Simulation of the steady state behavior of the three-phase BDHC.



(a) (b)

Fig. 10. Steady state operation of the 3 BDHC. Step-up output dc and three-phase ac output voltages at (a) 50 Hz, (b) 400 Hz.

5) Compared to a conventional VSI, the input current of the 3 BDHC is continuous. Hence, the input filter requirements are reduced, and the converter can be effectively interfaced to renewable sources, e.g., solar panel with lesser input power distortion.

VI. VERIFICATION

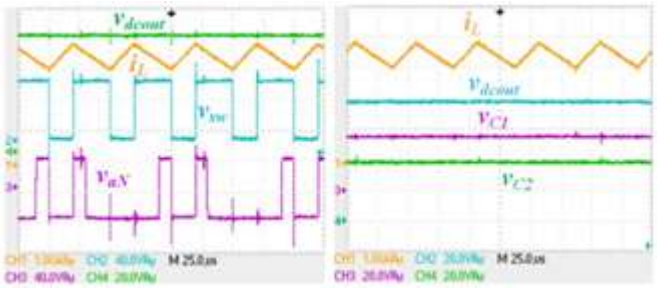
A. Steady state operation

The behavior of the converter has been verified using a 150 W experimental prototype. The switching frequency of operation is 10 kHz. The specifications of the prototype has been shown in Table I. From a 48 V input DC, the converter can generate a 80 V dc output as well as a three-phase 15 V rms ac output (phase) for a duty cycle (D_{st}) of 0.4 and modulation index (M_a) of 0.55, respectively. The steady state behavior of the converter has been simulated using Pspice and has been shown in Fig. 9. The simulation results validates that the input current of the converter is continuous. The simulation shows that the switch node voltage (v_{sw}) has two distinct levels, equal to zero and (v_{dcout}), neglecting the drop in the diode D. This shows that the converter is operating at continuous conduction mode at these conditions.

Fig. 10 shows experimental results which validate the operation of the proposed three-phase BDHC topology. The parameters used for the experiment are: R_{ac} = 50 ; R_{dc} = 40 ; L = 1 mH; $C_1 = C_2$ = 1 mF; L_f = 1 mH; C_f = 10 F; $R_1 = R_2$ = 10 k : The output dc (v_{dcout}) as well as 3-phase ac output voltages (v_A; v_B; v_C) at frequencies of 50

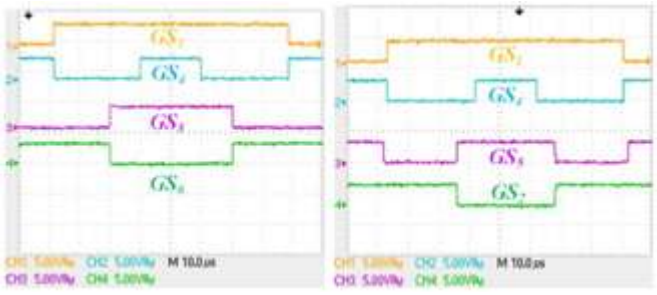
TABLE I
EXPERIMENTAL SPECIFICATIONS

Parameter	Attribute
Input	48 V dc
DC output	80 V dc
AC output	20 V ac (peak)
Switching frequency	10 kHz
DC load	40
AC load	50 (balanced)



(a) (b)

Fig. 11. Steady state operation of the split-dc output capacitor-based 3 BDHC. (a) The switch node voltages v_{sw} and v_{aN} , input current and output dc voltage v_{dcout}, (b) voltage across the split-dc output capacitors v_{C1} and v_{C2}



(a) (b)

Fig. 12. Steady state operation of the BDHC. (a),(b) Gate control signals for the condition $v_{ma} > v_{mb} > v_{mc}$.

Hz and 400 Hz have been shown in Fig. 10 (a) and Fig. 10 (b), respectively.

Fig. 11 (a) and Fig 11 (b) validate that the input inductor current (i_L) waveform of the proposed converter is continuous. The relation between the switch node voltage (v_{sw}) and the phase leg output (v_{aN}) for the split-dc output capacitor based 3 BDHC is shown in Fig 11 (a). From the results, we can show that the phase output voltage is bipolar, and assumes a negative pole voltage during the shoot-through interval. Also, the power interval occurs only when the diode D conducts. The voltage across the split capacitors have been shown in Fig 11 (b).

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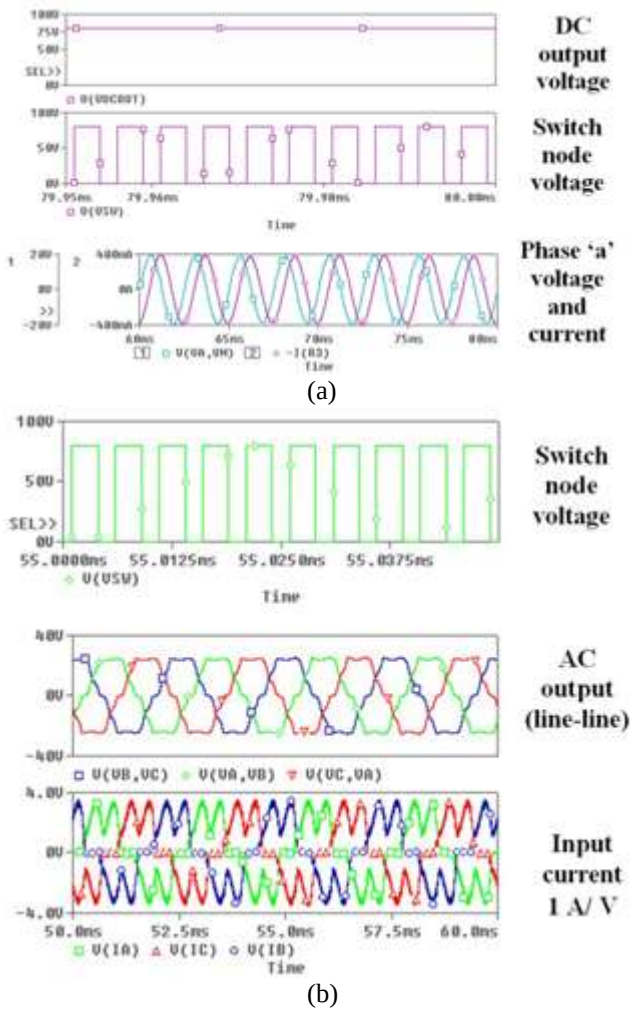

Fig. 13. Simulation of the behavior of the 3 BDHC to (a) highly-inductive loads (R = 10 , L = 19.49 mH), (b) non-linear load (diode bridge rectifier with 50 resistor and 10 F output capacitor).

B. Gate control signals

Fig. 12 (a) and Fig. 12 (b) show the gate control signals for the 3 BDHC topology. The gate control signals are for the condition when the reference control signals are related as $v_{ma} > v_{mb} > v_{mc}$. The schematic shown in Fig. 8 has been implemented digitally using TMS320F28335 digital signal processor to generate the gate control signals.

C. Behavior of the 3 BDHC to inductive and non-linear loads

The behavior of the 3 BDHC has been studied when subjected to inductive and non-linear loads. Fig. 13 (a) shows the behavior of the converter to highly inductive balanced three-phase loads. The parameters of the balanced 3 load are: R = 10 and L = 19.49 mH. Fig. 13 (b) shows the behavior of the converter when interfaced to a diode-bridge rectifier with an output capacitor of 10 F and output of 50 load.

VII. CONCLUSION

In this paper, a three-phase hybrid converter topology with simultaneous dc and a 3- ac outputs that can be independently regulated has been proposed. Furthermore, the topology has been shown to exhibit shoot-through protection, continuous input current and reduced number of switches. Suitable circuit modification has been shown to realize a conventional BDHC and a split-dc capacitor-based BDHC. A PWM control scheme for regulation of both outputs has been described. Preliminary experimental results have been shown which validate operation of the proposed converter topology.

ACKNOWLEDGMENT

The authors would like to thank the Department of Science and Technology, Government of India, for providing funding to this research under the grant no. SR/S3/EECE/0187/2012.

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