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Frequencey to digital conversion based sampled PLL

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***Abstract*—** Conversion of analog signal frequency in digital output is presented. Phase-Locked loops (PLL) serving as a frequency synthesizer locks the output frequency and generates the square pulse output which is sampled and processed digitally. Simulation results presents that errors due to various factors are minimized and provide wide range of linearity and insensitivity to non-linear error. A lower phase noise, low power consuming, wide range frequency generating and increased tuning range Voltage-Controlled Oscillator (VCO) design is used. An improved current mismatch adjusting circuit controls mismatches in UP and DOWN currents which does not allow disturbing the control voltage so that disturbances to PLL can be reduced and it works on smoothly. For a particular range of frequency bands voltage controlled delay lines acts as a replacement for PLL. They are easier to stabilize and have low jitters and avoid false locking problems.

Keywords*—frequency to digital converters, efficient charge pump, high frequency synthesizer, digital PLL*

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I. INTRODUCTION

Analog circuits are facing performance degradation day by day in aspects of power consumption and delay as compared to nanometre technology used in modern digital circuits. Due to less gain, different device sizes in analog circuits, and low supply voltages limits the use of analog circuits[1] in high performance. A trade-off exists [3]between gain. Band-width, delay, power, and supply voltages which limits either one of the aspect in order to achieve another aspect. Thus in design of Analog-to-digital converters maximum concern is to replace analog circuitry by digital as much as possible. In design of a F2D converter design of efficient PLL is prime concern[4]. A sampler samples the PLL[2] output and followed by digital differentiator which together performs the time encoding of signal information. A sampling is a time axis quantization techniques, that's what usually Sigma-Delay-Modulator do for quantization in voltage axis. A digital differentiator eliminates +the sampling noise by time domain quantization.

In high demand of bandwidth, synchronous interfaces use PLL as a reference clocks. To remove timing errors like clock skew PLL should be designed with less settling time, maximum frequency range and improved phase margin. There is dead phase zone in CP of PLL which causes non idealistic nature of PLL. Those characteristics are: (1) charge injected due to parasitic capacitors (2) current mismatches between UP and DOWN currents (3) ripples (4) variations in voltages along source and drain voltages in transistors. A Frequency-to-Digital (F2D) converter is proposed with PLL and DLL. In addition to the previous works the presented circuit focuses to reduce mismatch in charge pump circuit and eliminates the phase errors. Besides this the charge sharing in CP is minimized. The VCO output is sampled and converted in digital levels and fed back to the input of phase detector. A Zero Crossing detector round offs the errors as quantization noise are shaped in sigma delta modulators, So that the phase noise is eliminated. The architecture is implemented in CMOS 180nm technology. Here two charge pump designs are proposed and a current starved high frequency ring oscillator type VCO is implemented.in section 2 we will discuss about the basic architecture of F2D converter and charge pump, phase noise introduced due to charge pump, followed by new charge pump is designed to reduce charge sharing and with reduced mismatching of UP and DOWN currents than in section 3 a detailed circuit description of current mismatch adjustment circuit is given. In section 4 design issues of F2D converter is shown.

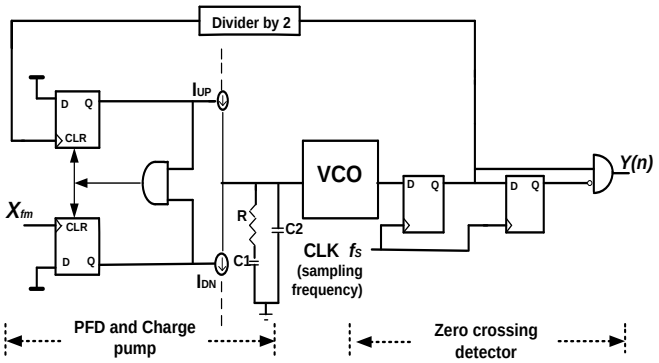

Fig 1: Proposed F2D converter

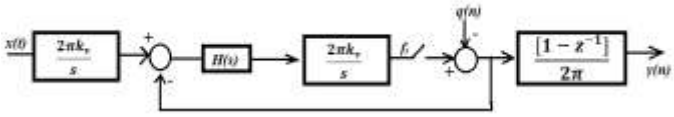

Fig 2 :linear model

Voltage controlled oscillators and charge pump is discussed at end.

I .BASIC ARCHITECTURE OF F2D CONVERTER

Description of architecture

A type II PLL performs the frequency locking operations. The sampled VCO output is fed back and acts as the one of the input of phase frequency detector[5]. $X_{FM}(t)$ is the Square wave is the input. If f_c considered to be the carrier signal frequency, *f(t)* is the instantaneous frequency if k_v (Hz/v) is the modulator system sensitivity in Fig 1.

$$f(t) = f_c + K_v x(t) \quad \ldots\ldots\ldots (1)$$

In traditional receivers output of VCO considered to be the output as demodulated desired signal, and output is converted into

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digital signals by conventional (Analog to Digital converters) ADC, but here approach is to convert VCO analog output into digital samples by a sampler[6]. Sampling is done by clocked D-flip-flops, which samples its output at the clock frequency of D-flip-flops. The signal reconstruction is carried out by a Frequency Discriminator (FD). Assuming input signal frequency sufficiently more than sampling frequency so that the input signal x(t) as some constant value X. Now for a duration of time T_{SA}, Zero Crossing Detector (ZCD) generates a output signal as a rectangular pulse of duration T_{SA} for VCO output. The averaged output of the system[5] is proportional to the ratio of sampling period to the input signal time period shown in Fig (2).

II PHASE DETECTOR

The "Phase frequency Detector" (PFD) is one of the main parts in PLL circuits. It has two D-flip-flops compares the Inputs of phase and frequency[4] difference between the reference clock and the feedback clock. 0Depending upon the deviation phase and frequency, it generates two output signals "UP" and "DOWN". The "Charge Pump" (CP) circuit is used in the PLL to combine both the outputs of the PFD and give a single output. The output of the CP circuit is fed to a "Low Pass Filter"(LPF) to generate a DC control voltage. The phase and frequency of the "Voltage Controlled Oscillator" (VCO) output depends on the generated DC control voltage. If the PFD generates[2] an "UP" signal, the error voltage at the output of LPF increases which in turn increase the VCO output signal frequency. On the antipodal, if a "DOWN" signal is created, the VCO output signal frequency decreases. The output of the VCO is then fed back to the PFD in order to recalculate the phase difference, and then we can create closed loop frequency control system shown in Fig (3).

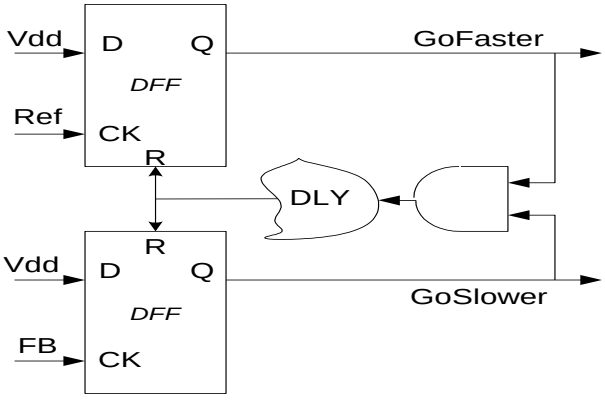

Figure 3: Phase detector

III CHARGE PUMP AND LOOP FILTER

Charge pump circuit is an important block of the whole PLL system.Current in charge pump decides the frequency of oscillation.It proselyte the phase or frequency difference error into a voltage, used to tune the VCO[6]. Charge pump circuit is used to join both the outputs of the PFD and give a single output which is federal to the input of the filter. Charge pump circuit gives a constant current of value IPDI which should be insensitive to the supply voltage[5] variation. The amplitude of the current always stick around same but the polarity variation which depend on the value of the "UP" and "DOWN" signal. The schematic diagram of the charge pump circuit with loop filter is shown in Fig (4).

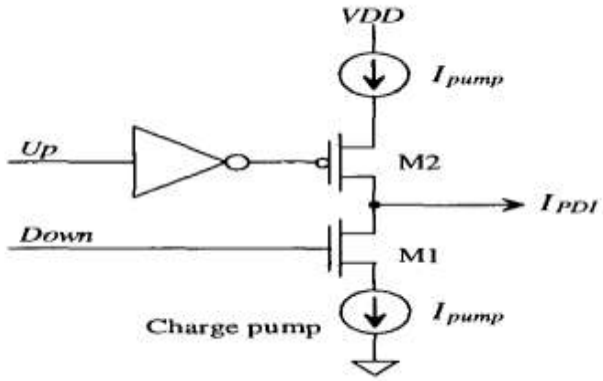

Fig 4 : charge pump

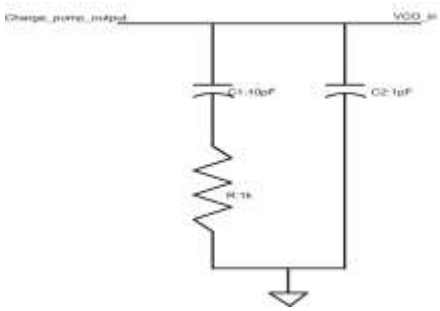

Fig 5 : Low pass filter

Whenever the UP signal is lead with respect to down signal high M2 transistor turns ON while M1 is OFF and the output current is IPDI with a positive polarity[6]. When the down signal becomes high M1 transistor turns ON while M2 is OFF and the output current is IPDI with a negative polarity.

IV DESIGN OF VCO

Design of VCO plays a critical role in dynamics of PLL. Desired characteristics of VCO are low power consumption, low operating voltage, low [5]phase noise, wide tuning range. Consumption of power and area required by PLL strongly depends upon VCO. The clock frequency of VCO can have a variation in frequency up to +/- 50% of its central frequency

Output frequency of VCO is the function of input voltage and the relation between the input voltage and output frequency should be linear[1]. Oscillators have their limited range up to which they shows linearity and that is the only suitable range for operation. Here a current starved VCO is used is a ring oscillator. Here the generation of oscillation purely depends upon concept of Schmitt trigger[2]. Characteristics difference between inverter and Schmitt trigger is that hysteresis present in the transfer curves. A Schmitt trigger circuit is shown in **fig 4(a).** Assume that output if is high, than transistors M3 if in saturation[8] and transistor M6 is in cutoff thus M4 and M5 provides a dc path to V_{DD}. If the output of Schmitt is high, input is below V_{SH}. Similarly if output is low M6 is in saturation and M3 is in cutoff, and

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output of Schmitt trigger will low if input exceeds V_{SH}. Schmitt trigger[7] will not change its state until input is between V_{SH} and V_{SL} which is the hysteresis of Schmitt trigger. Here current flowing through transistors M1 and M3 are same.

If input voltage is less than the threshold of transistor M1, and V_X maintains at $V_{DD} - V_{th3}$ .The point at which M1 is getting on and potential V_X gets start to fall down to zero. Thus switch potential is given as:

$$V_{in} = V_{SH} = V_{th2} + V_x$$

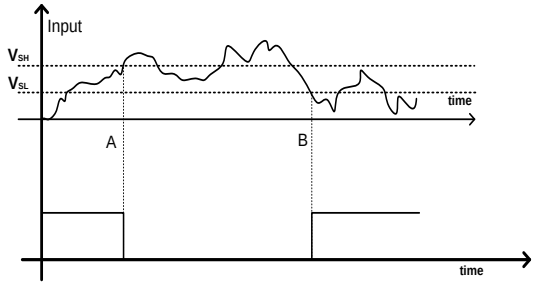

Fig 6 : Schmitt trigger

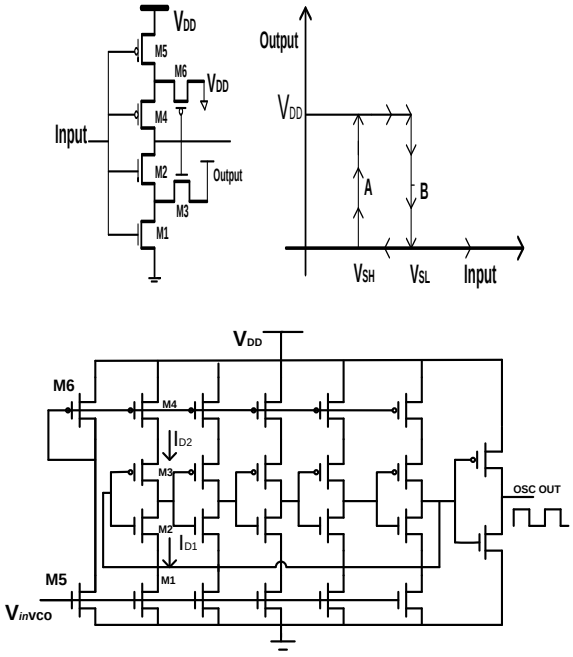

Fig 7 :A Schmitt trigger application, current starved VCO.

Here the current an equation valid which is given as:

$$\frac{k_1}{2}(V_{SH} - V_{SL}) = \frac{k_2}{2}(V_{DD} - V_X - V_{th3})^2 \quad \text{.....(2)}$$

If source terminal of transistors M2 and M3 are connected on common potential, threshold voltage due to body effect will be same. Using above equation new equation can be formulated. The following equation defines high switching voltage.

$$\frac{k_1}{K_2} = \frac{W_1}{L_1}\frac{L_3}{W_3} = \kappa\left[\frac{V_{DD} - V_{SH}}{V_{SH} - V_{TH}}\right]^2 \quad \text{.....(3)}$$

Similarly lower switching voltage is defined as:

$$\frac{k_5}{K_6} = \frac{W_5}{L_5}\frac{L_6}{W_6} = \kappa\left[\frac{V_{SL}}{V_{DD} - V_{SL} - V_{th}}\right]^2 \quad \text{.....(4)}$$

Solving these equations we determine voltages V_{SH} and V_{SL}.
This Schmitt trigger generates the oscillations in current starved VCO. Voltage at one stage Schmitt crosses V_{SH}, the output swings low, so that the oscillator output reaches high and allows a constant current from lower transistor to discharge down to V_{SL} [8], and the Schmitt trigger switches its state. If this event continues, a square output wave is generated. Here M1and M4 acts as current limiter, which control current flowing through M2 and M3 the inverter stage. Always middle inverter is starved for current so this oscillator is known as current starved VCO.[9] This VCO has infinite input resistance and input capacitor is small as compared to that capacitance of loop filter. Total capacitance on drain terminal of transistor is M2 and M3 is given as the sum of input and output capacitance.

$$C_{eff} = C_O + C_I = C_{ox}(W_p L_p + W_n W_n) + \frac{3}{2}(W_p L_p + W_n W_n) \quad \text{.....(5)}$$

$$C_{eff} = \frac{5}{2} C_{ox}(W_p L_p + W_n W_n) \quad \text{.....(6)}$$

Thus rise and fall time off oscillator are defined as:

$$t_r = C_{eff} \cdot \frac{V_{SH}}{I_{D2}} \qquad t_f = C_{eff} \cdot \frac{V_{DD} - V_{SH}}{I_{D1}} \quad \text{.....(7)}$$

Obviously it is desired for clean oscillation I_{D1} and I_{D2} to be equal to I_D and if input voltage of VCO is V_{DD}/2, than sum of rise and fall time are given as:

$$t_f + t_f = C_{eff}\frac{V_{DD}}{I_D} \quad \text{.....(8)}$$

Frequency of oscillation is given by the equation:

$$f_{osc} = \frac{1}{N(t_r + t_f)} = \frac{I_D}{NC_{eff}V_{DD}} \quad \text{.....(9)}$$

V SIMULATION RESULTS

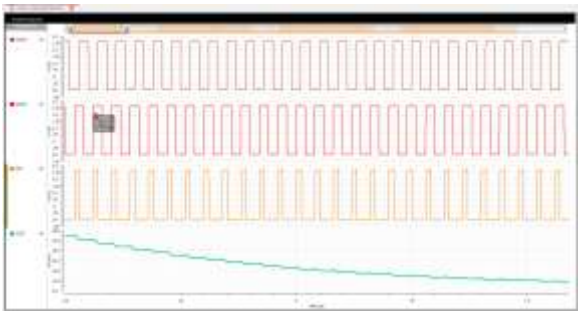

Fig.8 : charge pump during dis- charging

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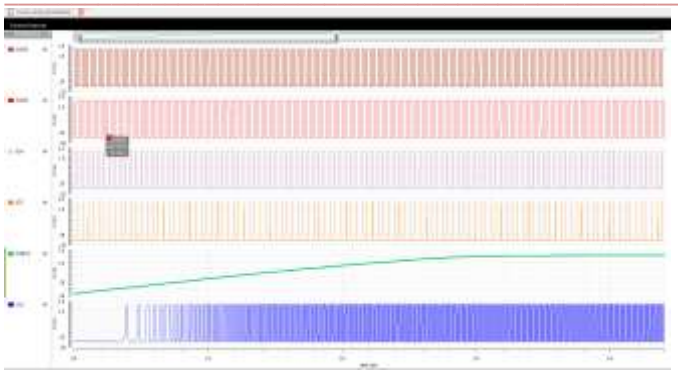

Fig 9: charge pump during charging & VCO during charging

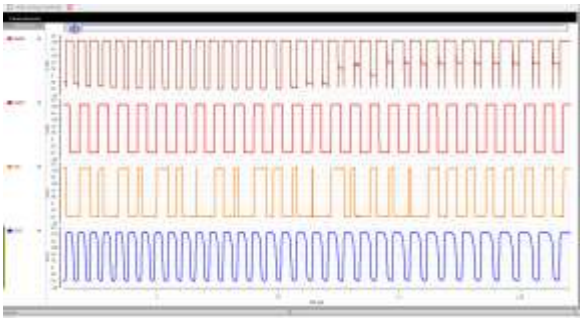

Fig 10 :PLL synthesizer

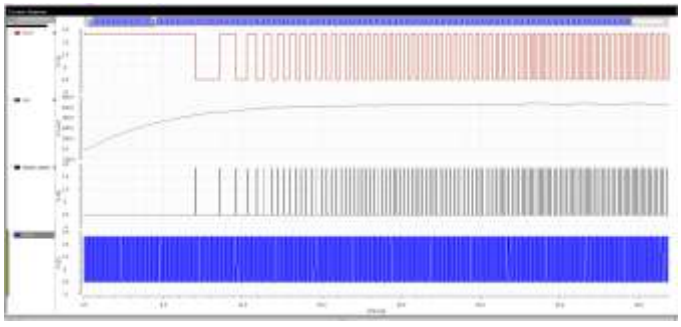

Fig 11 :F2D converter

Parameter	Value
Reference Clock frequency (F_{ref})	500 MHZ
V_{inVCO}	0 to 1.2V
Supply voltage	1V
Divided by n	2
C0	10pF
C1	1pF
R	1K ohm

Table I. Design parameters of the proposed frequency synthesizer

VIII. CONCLUSION

Proposed architecture is a low power consuming F2D converter. Traditional ADC are quite complex and consumes more power. Digitally controllable self-calibrating charge pump circuit which over comes the dis-advantages of conventional charge pumps PLL. A current starved VCO is low power consuming and provides wide range of linearity.a MOSFET based frequency synthesizer circuit capable of synthesizing a reference clock frequency into twice the frequency was designed. The functionality of the designed circuit is verified by synthesizing a 1GHz frequency from a reference frequency of 50MHz. The lock-in time observed is 234 ns.

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