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Optimizing Power in FinFET Based Domino Logic Circuit

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***Abstract*—**FinFETs are non planar transistors widely used in place of planar CMOS. In this paper, design of domino logic circuit using FinFET is discussed. By using the property of quantizing the width of FinFET, the design of domino logic is optimized. For a circuit with domino logic having pull down network (PDN) is designed, the leakage current of that PDN gets affected by the strength of the keeper. Sub-32nm technology is used to optimize FinFET based domino circuit's performance by reducing power consumption. This can be achieved via a different methodology for the design of keeper based on FinFET, by exploiting the 4 terminal (4T) FinFET devices that have a capacitive coupling among the gates. The method helps in reducing the contention current occurred due to keeper transistor and PDN transistors. A comparative study between the circuits for both standard domino AND gate and XOR gate with their new circuit design is done.

Keywords*—FinFET, Domino Logic, Keeper design, Threshold voltage*

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I. INTRODUCTION

FinFET is a non-planar or 3D transistor, which is set up on silicon on insulator (SOI) substrate. FinFET contains a body of silicon which is very thin and its width is wrapped by gate electrodes. It has source, drain and gate terminals. Multiple gate terminals are used to control the current flow. The source to drain diffusion surrounded by the gate is separated by the gate oxide. There is a three dimensional bar above the silicon substrate which acts as the channel between the source and drain. This thin bar is known as 'fin'. Thickness of fin determines the effective channel length of the device. For multifin devices, width can be calculated as twice the product of number of fins and the height of the fin. FinFETs can have multiple small units of fins based on the height constraints. This represents the width quantization property of FinFETs. With the increase in number of fins, it is possible to increase the width of the device. Even though smaller fin heights are favorable, it leads to multiple fins that result in more silicon area.

FinFETs are preferred over conventional CMOS in order to overcome the short channel effects. Short channel effects arise in CMOS due to scaling i.e. the channel length is reduced to increase both the operation speed as well as the number of components per chip [1]. Multiple gates of FinFET result in reduction of short channel effects. There are two main types of FinFET: Shorted gate (SG) and Independent gate (IG) [2]. Shorted gate FinFETs are also known as 3 Terminal (3T) FinFET and independent gate FinFETs are known as 4 Terminal (4T) FinFETs [3]. 3T FinFETs have higher ON current and higher OFF current compared to those of 4T FinFETs. 4T FinFETs enable the use of back gate bias that helps in varying the threshold voltage of front gate linearly by applying different voltages to both the gates [4].

In this paper, 3T as well as 4T FinFET standard cells are used. A domino logic circuit for AND gate and exclusive OR (XOR) gate is designed using FinFET. The design of keeper transistor is modified for various circuits. A standard domino is designed with two different 3T transistors each for precharge and keeper. A novel method is designed to optimize power. This design modulates the gate to source voltage instead of threshold voltage. The paper is organized in following manner. Section II gives an explanation on the working of different circuits. Section III details the results and discussion followed by conclusion in section IV.

II. CIRCUIT DETAILS

The major advantage of considering dynamic logic includes increased speed and reduced implementation area. Less number of devices to implement a given logic function implies that the overall capacitance is much smaller [5]. Power dissipation for a dynamic gate is much lower than for a static gate. This is because dynamic circuits use fewer transistors for realization. Also, for each fanout the load is one transistor instead of two. There is no glitching in dynamic logic design, i.e. one transition per clock cycle is done. Dynamic circuits do not have short circuit power since only pull down path is analyzed when the gate is evaluating. Some of the major issues in dynamic design are charge leakage and charge sharing. Charge leakage occurs when the output node has high impedance state in the evaluation mode given the PDN is OFF. Charge sharing occurs when the charge stored at the output node is shared among the junction capacitance of the transistors in evaluation phase [6]. A keeper transistor is placed to deal with the charge leakage and charge sharing issues. This leads to high contention current due to the keeper transistor and the pull down transistor [7]. There arises one major problem for dynamic circuits during cascading. Hence, we go for domino logic design.

A. Standard domino logic

A standard domino logic using FinFET for an AND gate is shown in Figure 1. It comprises of two PMOS transistors, one act as a precharge device and other as a keeper. It also includes one NMOS transistor as a footer device, a pull down network (PDN) and an inverter. The working of domino logic has two stages: Precharge and Evaluation. In the prechage stage, the clock (CLK) signal is kept low, during this the precharge transistor gets activated and the dynamic node gets charged to V_{DD}. This discharges output node to ground and turns ON the keeper transistor. The circuit enters the evaluation phase, when

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there is a transition from 0 to 1 in the clock. During this stage, the footer transistor gets activated and the signal at dynamic node is decided by the inputs of PDN discharges to ground or is kept at V_{DD}, depending on the inputs of the PDN.

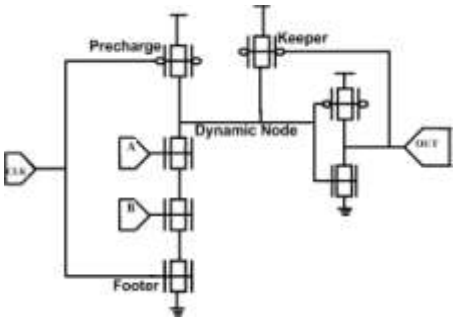

Figure 1. Schematic representation of standard domino logic for AND gate using FinFET

In this paper we go through the analysis of XOR gate along with the AND gate. Several VLSI applications use XOR gate as the arithmetic unit in adders, microprocessors etc. To design XOR gate using the domino logic provides several as the domino circuits have only pull down network. This reduces the unwanted capacitance at the dynamic and output which in turn enhances the speed of domino XOR gate. A standard domino XOR gate inputs require two signals i.e. original and its inverted one for PDN [8]. The circuit consists of precharge and evaluation transistors that depend on the clock signal. The circuit enters the precharge phase when CLK is low, at this time dynamic node is charged to V_{DD} via pull up network i.e precharge transistor. Footer transistor is switched OFF to avoid the short circuit current. When CLK turns high the circuit enters evaluation phase and the precharge transistor is turned OFF whereas footer transistor turns ON. Discharging of dynamic node starts depending on the inputs of PDN.

B. Dual purpose 4T FinFET

New Keeper design is implemented in order to improve the power consumption and to enhance the behavior of domino logic. Two circuits are explained here for keeper design. The first one has a single 4T FinFET device working both as precharge transistor and keeper transistor. This is shown in Figure 2. Having a single transistor working as both precharge and keeper has several advantages. The gate of the precharge transistor decreases and the output load capacitance decreases. These result in lower power consumption and have shorter delay. The second circuit for the modified keeper design for AND gate is shown in Figure 3. It consists of a non-inverting delay, a NAND gate to provide sufficient delay, an independent gate FinFET as keeper transistor [9].

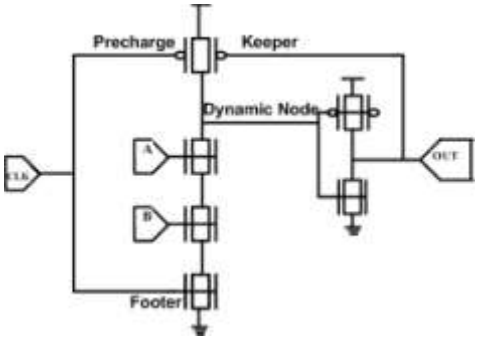

Figure 2. Circuit for 4T FinFET as precharge and keeper block

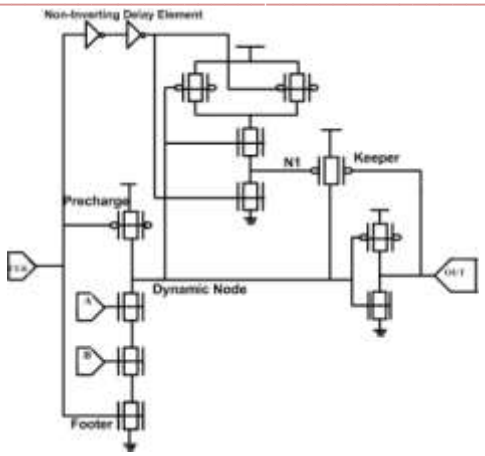

Figure 3. FinFET domino AND logic with keeper having varying threshold voltage

The XOR gate design with keeper having varying threshold voltage is shown in Figure 4. During precharge cycle, the CLK is set low, if PDN is OFF, the dynamic node starts charging to V_{DD} and output node starts discharging. The node N_1 is set to V_{DD} that is given to one of the gates of keeper transistor and a logic 0 from the output to other gate. This makes keeper transistor to work with only one gate. During this mode it has high threshold voltage. The evaluation cycle begins when the CLK is high. If the PDN is in ON state, the dynamic node starts discharging.

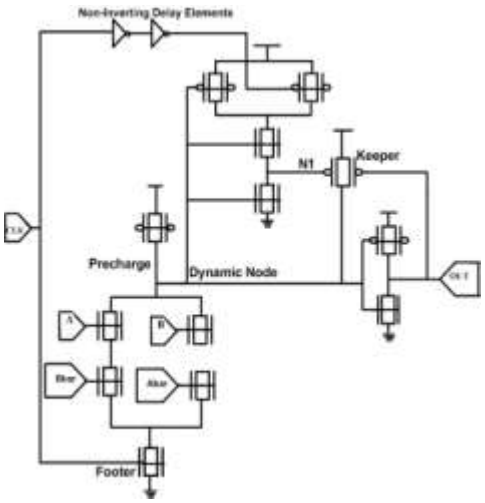

Figure 4. FinFET domino XOR logic with keeper having varying threshold voltage

C. FinFET Domino with gate-source modulation

An alternative method to design the keeper transistor is achieved by controlling gate-source voltage instead of varying threshold voltage. The circuit design of domino XOR logic by this method is shown in Figure 5. This design has T1 transistor working as both keeper and precharge. The performance of precharge is done by the front gate and that of keeper by the back gate of T1 transistor. By modulating the gate-source voltage we can adjust the strength of the keeper. This can be achieved by applying a differential waveform to the gate [10]. Differential waveform can be obtained by placing the transistor T1 and T2 as shown in Figure 5. The transistor T1 and T2 can work as an RC circuit. Using this RC circuit and the CLK we can obtain a modulating gate to source voltage.

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In a subthreshold region, the transistor T2 acts as a resistor. The capacitor can be obtained by the 4T transistor T1 using the combined capacitance that exist between the front gate and back gate of transistor T1 [10]. This RC circuit results in a differential waveform K_b when there is a transition in CLK. To vary the strength of keeper, this differential waveform is used.

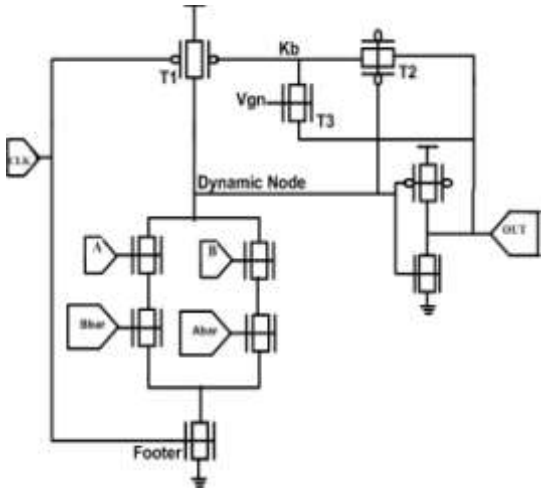

Figure 5. FinFET domino for XOR logic with gate bias

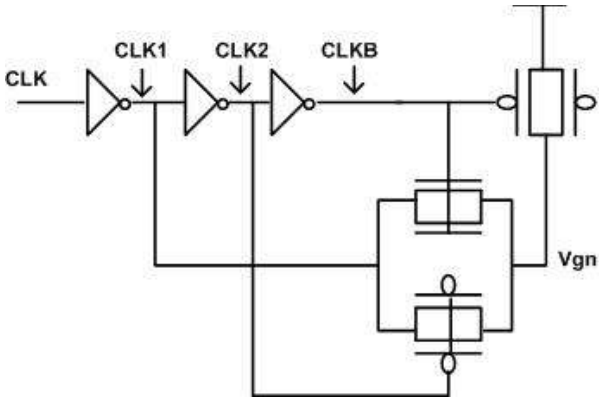

Figure 6. Circuit for generating gate bias of T3 [10]

During the start of the evaluation stage, K_b provides small gate to source voltage that decreases the strength of the keeper transistor. Gradually it increases the keeper strength by providing large gate to source voltage. K_b connects the output through the transistor T3. The gate bias Vgn, for transistor T3 is attained by the circuit shown in Figure 6. It consists of three inverters with CLK, CLK1 and CLK2 as inputs respectively. There is a pass transistor that outputs V_{gn}. V_{gn} is always in logic 1 state with some delay.

III. Results and Discussion

A. Standard Domino logic

The result for standard domino logic for AND gate is shown in Figure 7. Firstly, the circuit is in precharge phase, where CLK signal is set to logic 0. The PDN is in OFF state with A = 0 and B = 1. At this time, only the precharge transistor is activated. The dynamic node gives logic 1 as output and logic 0 is assigned to output node. As the CLK signal transitions to 1, the circuit switches to evaluation stage and PDN is ON i.e. A = 1 and B = 1, the dynamic node discharges to logic 0 and output node charges to 1 otherwise if PDN was in OFF state the dynamic node remains in the logic 1 state.

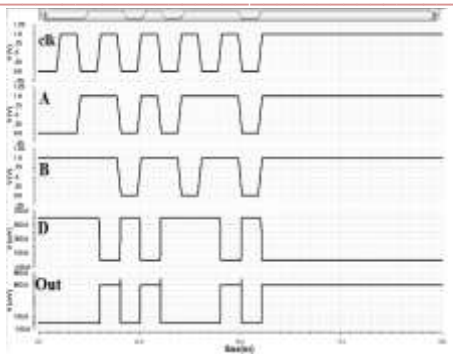

Figure 7. Output for the standard domino AND gate

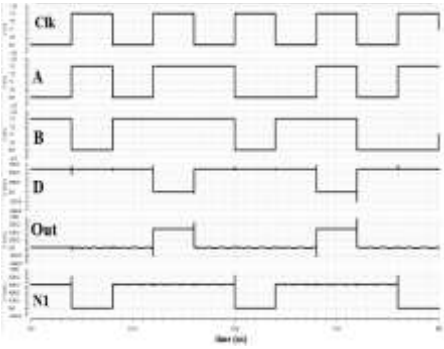

Figure 8. Output for FinFET domino AND with variable threshold voltage keeper

B. Dual purpose 4T FinFET

The simulation result of domino AND gate and a domino XOR with variable threshold keeper [9] is shown in Figure 8 and Figure 9 respectively. The signal N_1 makes the keeper operate with single gate providing high threshold voltage. This happens during precharge mode. When the circuit enters evaluation mode, given the PDN is ON i.e. A=1, B=1, dynamic node discharges to logic 0 and output node to logic 1. During this phase, the contention current gets reduced and speed is increased.

When the PDN is OFF i.e. A=0, B=0, the dynamic node remains in logic 1 and output node in logic 0 states. At this time, the signal N_1 is in logic 0 state which activates both the gates of keeper transistor with a low threshold voltage.

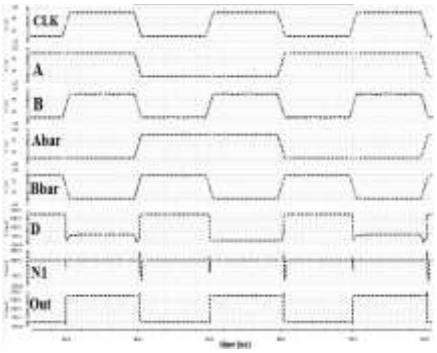

Figure 9. Output for FinFET domino XOR with variable threshold voltage keeper

C. Domino circuit design with gate-source modulation

The simulation result of domino circuit with gate-source modulation [10] is explained here. Figure 10 shows the result for domino XOR gate when the CLK transition is from 0 to 1,

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given PDN is in ON state. The XOR gate gets activated when the signals are A=0, B=1, Abar=1 and Bbar=0. As the CLK transition is from 0 to 1, dynamic node discharges to logic 0 and output node to logic 1.

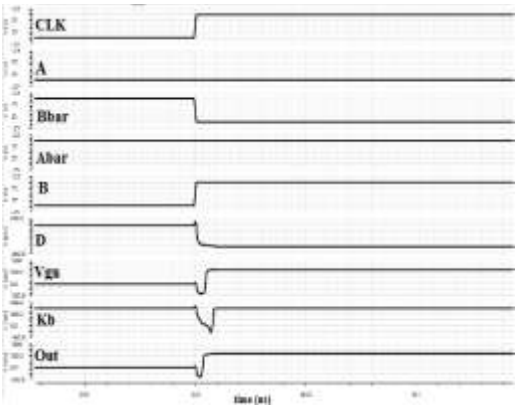

Figure 10. Output for XOR domino design with gate-source modulation with clock transition from 0-1 and PDN is ON

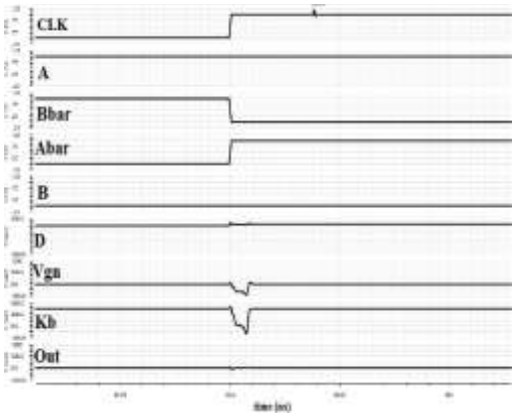

Figure 11. Output for domino design for gate-source modulation with clock transition from 0-1 and PDN is OFF

The Figure 11 shows output for domino XOR when the CLK signal transitions from 0-1, given PDN is in OFF state i.e. A=1, Bbar = 0, Abar = 1 and B = 0. The signal K_b shows the differential input to transistor T2 that provides gate-source modulation.

The comparison of results with respect to power reduction is displayed in Table 1. From the table we can infer that the circuit for domino FinFET with gate source modulation gives better result as compared to the standard circuit for domino logic and domino circuit having variable threshold keeper.

Table I: Comparison of power in different circuits

Circuit Mode	AND gate	XOR gate
Standard Domino	15.708µW	13.452µW
Domino with variable threshold voltage	9.476µW	9.402µW
Domino with gate-source modulation	9.317µW	8.00µW

IV. Conclusion

In this paper three types of domino logic design for AND gate as well as for XOR gate is designed in sub 32-nm FinFET. The three designs are standard domino logic, domino logic with variable threshold and domino logic with gate-source modulation having differential waveform at gate bias of transistor. For FinFET domino logic using gate-source modulation, the keeper transistor uses the 4T FinFET property of having coupling capacitance between front and back gates. From the results we can see that domino logic design with gete-source modulation shows a reduced power dissipation for both AND logic and XOR logic.

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