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Design of CMOS based ECG System for Bio-Signal Application

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Abstract— This work aims to present the design and realization of CMOS based ECG system using 45 nm technology. The main objective of this work is to extract noise figure, power, CMMR and gain of CMOS based OP-AMP for bio-signal application. The design of CMOS based OP-AMP for bio-signal application for different technology is already done. The design of OP-AMPs continues to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technologies. All the designed and simulation were done using cadence virtuoso tool.

Keywords- *CMOS,OP-AMP,ADC,ECG System*

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I. INTRODUCTION

Electrocardiography (ECG) system is the device used to transmit the electrical signals of the heart to the remote machine. These electrical signals are ECG signals which is sensed by electrodes. This signal is caused due to electrical activities in the heart. ECG signals have very low amplitude and frequency and, hence amplification is needed to strengthen this weak signal to high level signal [1]. The basic block diagram of ECG system and most commonly bio-medical signal as shown in Fig.1 and Fig.2 respectively.

Fig.1 Proposed ECG System

Signal	Frequency	Range
ECG	0.05-250Hz	5uV-8mV
EEG	0.5-200Hz	2uV-200uV
EMG	0.01-10kHz	50uV-10mV

Fig.2. Most commonly used biomedical signal

Normally bio-signal are the weak signal in the range of 5uV to 8 mV. Due to the weak voltage level, the signal is fed into an amplifier circuit to be amplified to a desirable voltage level then the output of amplifier is then fed into a low pass filter circuit The purpose of filter is to filter out the very low and high frequency noise components of the signals. The desirable analog output from the filter is then sent to S/H and ADC to become a digital signal. After that, these digital data will processed in PCs or microprocessors.

II. TWO STAGE OP-AMP

Operation amplifier is the key element of an analog processing system which performs the function of a voltage controlled current source with an infinite voltage gain. Operational amplifiers are an integral part of many analog and mixed-signal systems. The topology of the circuit designed is that of a standard CMOS op-amp. The first stage of an op-amp is a differential amplifier. This is followed by another gain stage, such as a common source stage [2] as shown in Fig.3. Design of the op-amp consists of determining the specifications, selecting the op-amp A_d (open-loop gain),CMRR(common mode rejection ratio),device sizes and biasing conditions, compensating the op-amp for stability, output range, and power dissipation[3-7].

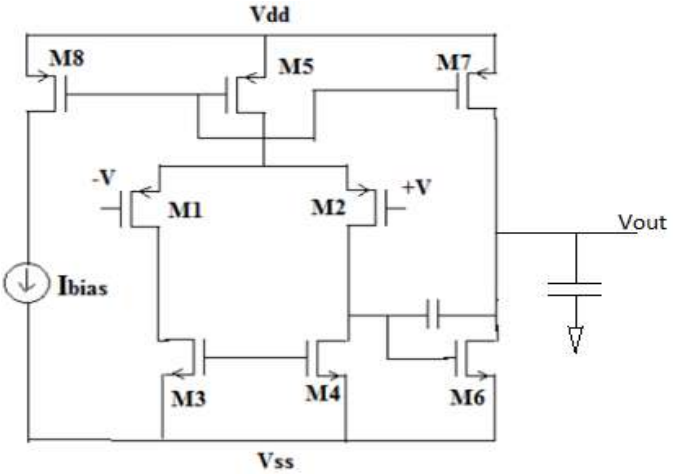

Fig.3. Circuit Configuration for a two stage OP-AMP with a p-channel input pair

In this schematic 1uA reference current and 1V power supply is used. The input signal of 5mV amplitude and 250Hz frequency is taken. Phase margin obtained 30.47 deg at gain crossover frequency 16.022MHz.

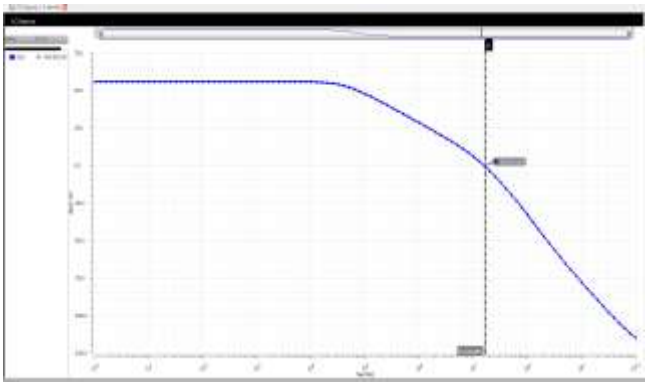

Fig.4. Bode Plot of Two Stage OP-AMP

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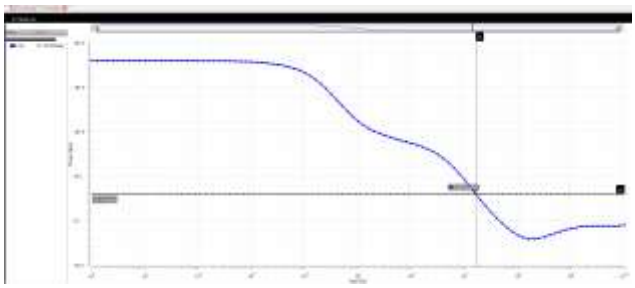

Fig.5. Phase Vs Frequency plot of Two Stage OP-AMP

The bode plot and phase vs. frequency output of two stage OP-AMP are shown in Fig.4 and Fig.5. Table 1 shows the simulation result of two stage OP-AMP.

Table 1.Simualtion Result of Two Stage OP-AMP

Process	**45nm CMOS**
Power supply	1V
Power Dissipation	1.138uW
CMRR	59.44dB
Gain	56.3dB
Phase Margin	30deg
Bandwidth	272.3kHz
Gain Bandwidth Product	15.39MHz
Slew Rate	~0

III. ANALOG TO DIGITAL CONVERTER (ADC)

For any application, analog-to-digital convertor (ADC) architecture is crucial for an overall system design. Some of the considerations are in terms of power consumption, accuracy, design complexity, speed etc. Fig.6 shows the typical block diagram of 3 bit Flash ADC. Analog to Digital Converter is the fastest way to convert an analog signal to a digital signal [8]. For 'N' bit converter, the circuit required 2^{N-1} comparators and a resistive divider with 2^N resistors. As shown in Fig.4 the Flash ADC consists '7'comparators, resister string, and 8:3 encoder. The analog input voltage is compared with reference voltage level which is generated from the resister string. The reference voltage for each comparator is least significant bit and that will be greater than the reference voltage for the comparator immediately below it. Each comparator produces a "1" when its analog input voltage is higher than the reference voltage applied to it otherwise the comparator output is "0"[8-9].

In this ADC, OP-AMP circuit is used as comparator. A CMOS comparator comprises of a current source for biasing the first stage differential pair followed by inverter stage for amplifying the differential pair output. The analog input signal is applied to the non-inverting terminal of the comparator and reference signal is applied to the inverting terminal of the comparator [9-11]. The output waveform of comparator as shown in Fig.7.

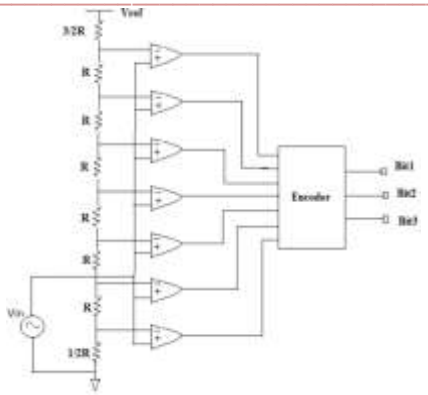

Fig.6. Circuit of 3 BIT Flash ADC

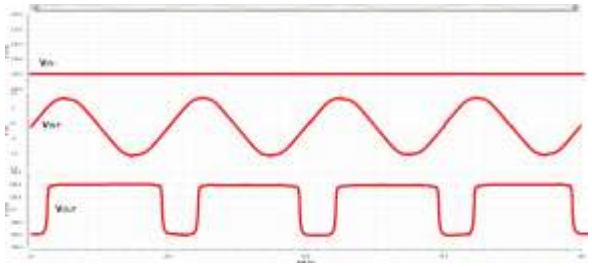

Fig.7. Output waveform of comparator

In Flash ADC, the priority encoder has a characteristic such that if two or more of its inputs are equal to '1' at the same time, then the input having the highest priority will take precedence. A digital encoder is a multi-input combinational logic circuit that converts the logic level "1" data at its inputs into an equivalent binary code at its output depending upon the priority [12-13]. The circuit diagram of encoder as shown in Fig.8 and outputs of priority encoder are given in Table 2 and the output waveform of encoder as shown in Fig.9.

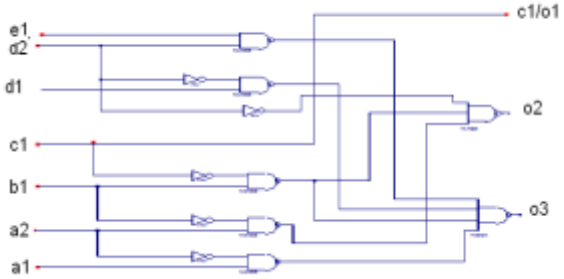

Fig.8. Circuit diagram of 8:3 binary encoder.

Table 2. Truth Table of binary encoder

INPUT CODE							BINARY CODE
E1	D2	D1	C1	B1	A2	A1	O1 O2 O3
0	0	0	0	0	0	0	0 0 0
0	0	0	0	0	0	1	0 0 1
0	0	0	0	0	1	1	0 1 0
0	0	0	0	1	1	1	0 1 1
0	0	0	1	1	1	1	1 0 0

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0	0	1	1	1	1	1	1 0 1
0	1	1	1	1	1	1	1 1 0
1	1	1	1	1	1	1	1 1 1

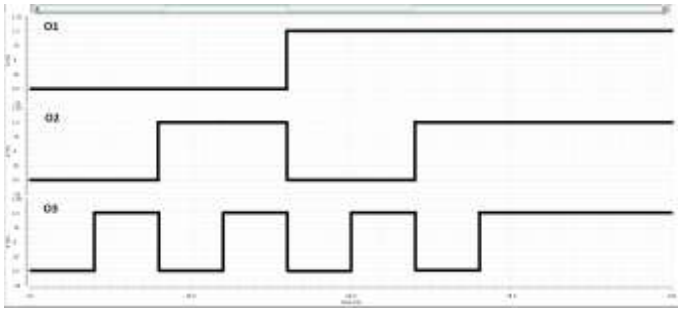

Fig.9. Output waveform of binary encoder.

IV. ECG SYSTEM

We propose an ECG system based on CMOS technology applicable for ECG monitoring applications. A block diagram of the system is shown in Fig.1.and schematic of ECG system as shown in Fig.10. An amplifier is designed using two stage op-amp with suitable gain, phase-margin, slew rate, bandwidth and CMRR. The ECG signal is received by this op-amp based amplifier and the amplified signal is then fed into a low pass filter circuit. The purpose of this filter is to filter out the very low and high frequency noise components of the signals. The desirable analog output from the filter is then sent to S/H and ADC to become a digital signal. After that, these digital data will processed in PCs or microprocessors. A high speed 3 bit Flash Type ADC is used for this purpose. The analog signal is converted into 3 bit digital signal with proper resolution.

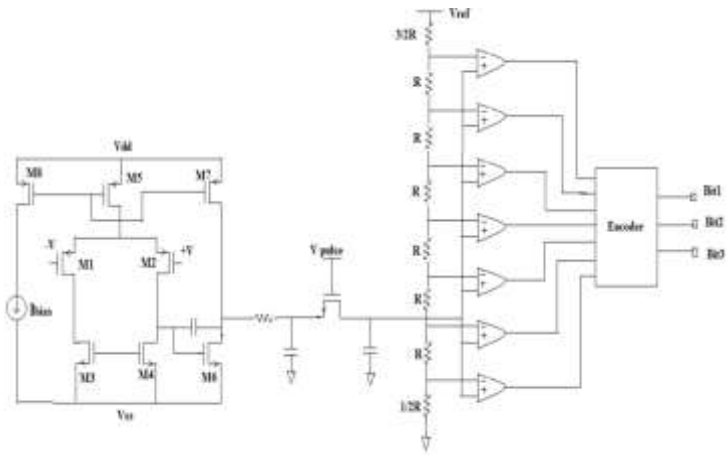

Fig.10. Circuit diagram of ECG System

CONCLUSION

This paper has detailed the design of a CMOS process based ECG system using high speed Flash Type ADC. The design has determined that the circuit gain is 56.3 dB and power dissipation is 1.138uW.

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