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Investigation on High Speed Double-Tail Comparator

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***Abstract*—** Comparator is a major building block of analog to digital converter (ADC) since speed of ADC is determined by the comparator. This paper discuss on high speed, low-power & low-voltage consumption comparators. This high speed comparator in Ultra Deep Sub Micrometer (UDSM) Complementary Metal Oxide Semiconductor (CMOS) technologies suffer low supply voltage. A typical single tailed and 2 double-tailed dynamic regenerative comparators are studied and investigated during this work. An inquiry on propagation delay of the device with various parameters is going to be carried out in this work. Study of various components of the total propagation delay and the relation of various parameters on individual delay components will be done**.**

Keywords- *Double tail Comparator, latching delay, dynamic clocked comparator, analog to digital converter.*

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I. INTRODUCTION

In an analog to digital converter (ADC) two analog signals or an analog signal and a reference signal is given to a comparator, which in turn provides digital Output. So comparator is the major building block of ADC. If the voltage difference between the two Input signals are greater than the threshold value, it will return a logic 1 as the Output, otherwise 0, thus converting analog signals to digital. Comparators used in high speed ADCs require high speed. So positive feedback circuit is used for comparator circuit.

High speed comparators incur low supply voltages notably when the threshold voltage of the device is not scaled relative to supply voltage of latest CMOS technology. Therefore, design of a comparator for low supply voltage is a challenging task. One method for getting high speed comparator is increasing the size of tail transistor used for supply voltage, providing large current in the circuit, compensating the die area as well as power. Sensitivity of the device for common mode voltage is limited due to low voltage operation. Instead of going for technology modification, comparator with low supply voltage can be developed by making some structure modification without much stacking of transistors between the power rails and only if they do not increase the complexity in the typical circuits.[1]

In this paper delay analysis of Typical Single-Tail comparator and double tail comparators for various architectures has been presented. This paper is arranged as follows. Part II- Investigation on the performance of the typical regenerative comparators and discussion on its merits and demerits, part III-Simulation results and delay analysis are addressed and part IV-Conclusion.

II. CLOCKED REGENERATIVE COMPARATOR

Clocked regenerative comparator has an extensive application in ADCs due to its fast decision making property as a result of strong positive feedback in regeneration phase. In this section a cyclopedic delay analysis of Typical Single-Tail comparator and double tail dynamic comparators is presented.

A. Typical Single-Tail Comparator

Fig.1. shows the schematic representation of a Typical Single-Tail comparator with large input impedance, output voltage swing, zero static power dissipation [2]. It has 2 phases of operation based on the CLCK input signal. When CLCK =0, reset phase. Both pMOS transistors T7 and T8 will be ON & transistor Ttail will be OFF. Nodes Out1 and Out2 are pre-charged to VDD, which activates the device. In the comparison state, when CLCK= VDD, transistors T7 and T8 are OFF, and transistor Ttail is ON. Output voltages (Out2, Out1), which has been pre-charged to VDD, start discharging with different discharging rates depending on the input voltage (IN1/IN2).If VIN1 > VIN2, Out1 will discharge faster than Out2. After a delay Out1 discharges to VDD – Vthp, resulting pMOS transistor (T6) to turn ON, that activates the latch regeneration. Thus Out2 charges to VDD and Out1 discharges to ground.

One of the main characteristics of comparator is its propagation delay. Total propagation delay of the circuit have two components: delay due to (1) t0 and (2) tlatch [3]. t0 is the delay due to capacitive discharge of load capacitor until the p channel transistors gets ON [4].
Discharge delay is given by,

$$t_0 = 2\frac{C_L \mid V_{thp} \mid}{I_{tail}} \qquad (1)$$

The second component, tlatch, represents the latching delay of two crosscoupled inverters. Device is expected to work properly when the output voltage difference, △Vo produced is equal to output voltage swing, △Vout = VDD/2. Threshold voltage of the device is assumed to be half of the supply voltage. Latch delay is given by,

$$t_{latch} = \frac{C_L}{g_{m,eff}}.\ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) = \frac{C_L}{g_{m,eff}}.\ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) \qquad (2)$$

For small circuits drain current of transistor T1 (I1) and drain current of transistor T2 (I2) is coming same.

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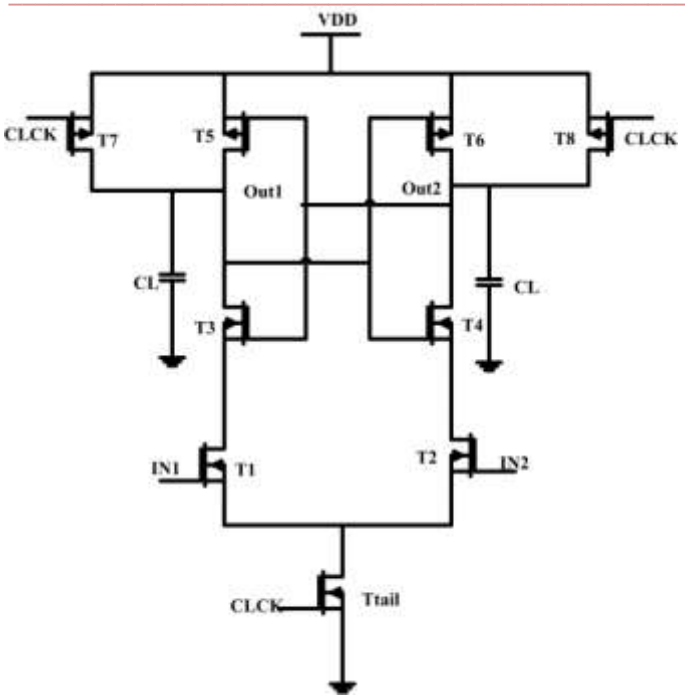

Figure.1.Schematic representation of Typical Single-Tail comparator

$$\Delta V_0 = |V_{outp}(t=t_0) - V_{outn}(t=t_0)|$$
$$= |V_{thp}| - \frac{I_2 t_0}{C_L} = |V_{thp}|\left(1 - \frac{I_2}{I_1}\right) \quad (3)$$

So △V0 will be small value. By using △V0, latch delay can be calculated using above given equations. But for this circuit drain current of transistor T1 (I1) and drain current of transistor T2 (I2) are equal in magnitude, so output difference voltage is 0 (3). If output difference voltage is 0, t0 becomes 0, discharge delay is 0. From (1) and (2) total propagation delay is directly related to load capacitance of the comparator, inversely proportional to Input difference voltage. Advantage of this circuit is that there is no static power dissipation since there is no rail-to-rail current path [1].

One drawback of this circuit is that, the supply voltage required to get a proper delay time is large due to stacked transistors in the circuit. It is because at start of decision making phase, transistors T3 and T4 will be ON, until either of the output voltage drops to small enough to make T5 or T6 ON to complete regeneration. Other drawback is that single tail transistor provides current for both cross coupled inverters and differential amplifier, where latch required large current for fast regeneration and small current to make differential amplifier in weak inversion.

B. Traditional Double-Tail Dynamic Comparator

Fig.3. shows the schematic representation of a traditional double-tail comparator. This topology has 2 tail transistors, provides current separately to differential amplifier and latch circuits. This topology enables rapid latching without depending on the input common-mode voltage (Vcm), and the small current in the input stage (small Ttail1) resulting low offset [5].

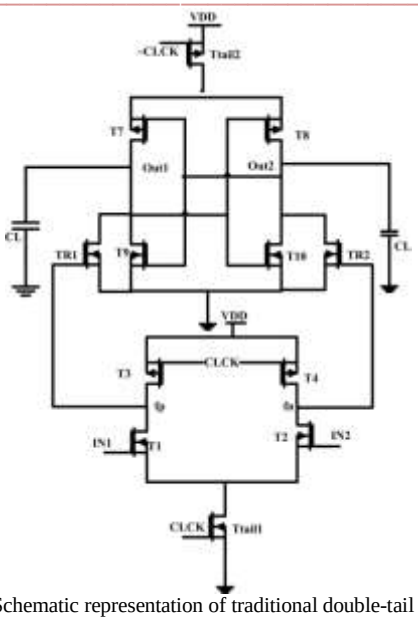

Figure.2. Schematic representation of traditional double-tail comparator

Working of the circuit is explained below. In reset mode CLCK = 0, Ttail1, and Ttail2 are OFF. Transistors T3 and T4 pre-charge fn and fp nodes to supply voltage. Transistors TR1 and TR2 discharges Out1 & Out2 to ground.

During regeneration mode (CLCK = VDD, Ttail1 and Ttail2 turn ON), T3-T4 turn OFF and fn and fp node voltages embark to decrement with various input voltages. A differential voltage △Vfn(p) has setup which depends on the input voltage. The transitional stage formed by TR1 and TR2 allows △Vfn(p) to the cross coupled inverters. By this input and output are properly shielded which results in, lesser kickback noise [6] ie. large variation in coupled regeneration node voltage through transistor parasitic capacitance to the comparator Input degrades the accuracy of the converter.

Delay calculation is similar to typical Single-Tail comparator (4), where delay consist of 2 components, t0 and tlatch. t0 is the delay due to capacitive discharge of load capacitor until the nMOS (T10 or T9) gets ON.

$$t_{delay} = t_0 + t_{latch}$$
$$= 2\frac{V_{Thn}.C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}}.\ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) \quad (4)$$

Total delay can be found from the transient analysis, Fig.4. It is the time when CLCK=1 to Output voltage difference becomes VDD/2. [6]

$$\Delta V_0 = V_{Thn.}\frac{\Delta I_{latch}}{I_{B1}} \approx 2V_{Thn}\frac{\Delta I_{latch}}{I_{tail2}} \quad (5)$$

Sizing of the tail transistors reduce the delay. Increasing the size of Ttail2 will provide large current in the latch circuit. It results in fast latching independent of Input common mode voltage. Size of Ttail1 is kept small, provides small current to Input stage, for low offset.

Delay depends on Input signals voltage difference. For a supply voltage of 0.8V, when Input signals voltage difference increases to 100mv, total delay gets reduces to 1.2ns. If the Input signals are with large voltage difference, comparator can easily compare the Input signals with less delay. But the comparator should be highly sensitive, such that it should be

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able to compare the signals with small common Input voltage difference. Traditional Double tail comparator compares the signals even if the Input signals voltage difference is 20mV. If the voltage difference between Input signals are less than 20 mV comparator will not compares the signals (CLCK period =5ns, V_{dd} = 0.8V , C_L =10fF, V_{cm} =700mV), .

Delay depends on supply voltage of the circuit also. As supply voltage increases delay decreases. If the supply voltage is less than 0.8V the circuit will not work properly. At 0.8V it is having a delay of 4.97ns (CLCK period =5ns, V_{dd} = 0.8V , C_L =10fF, V_{cm} =700mV).

Voltage difference at △Vfn/fp at t0 affects the Output voltage difference and so latch delay also. Therefore increasing △Vfn/fp reduces the delay of the comparator.

C. Double-Tail Dynamic Comparator

It has two additional control transistors and two switches. This toplogy also have two phases of operation [1]. During the reset phase CLCK is given 0, so both the tail transistors will be OFF and the control transistors will be ON. This will bring nodes fn and fp to V_{dd} . As a result intermediate transistors TR1 and TR2 pulls down the output to ground.

In decision making mode, CLCK will be 1, both tail transistors will be ON. Bottom tail transistor provides a direct discharging path for fn and fp to ground. Rate of discharging depends on the input voltage difference. If $V_{IN1} > V_{IN2}$, then fp will discharge faster than fn. At start of decision making phase T7 and T8 is ON which tries to bring Output nodes to V_{dd}, However before that TR1 will be OFF and TR2 will be ON making Out1 to charge to V_{dd} and Out2 to discharge to ground.

During this phase one of the switch will be ON and and other will be OFF. When the switch is ON it pulls down fn/fp to ground faster reducing the delay. If one node is charging to V_{dd} then the other should be discharged to ground faster, it is done by the switches TSW1 and TSW2.

As discussed for the previous comparators, total delay depend on various parameters such as Input voltage difference, frequency of the Input signal, supply voltage, load capacitance, W/L ratio of the tail transistors etc.

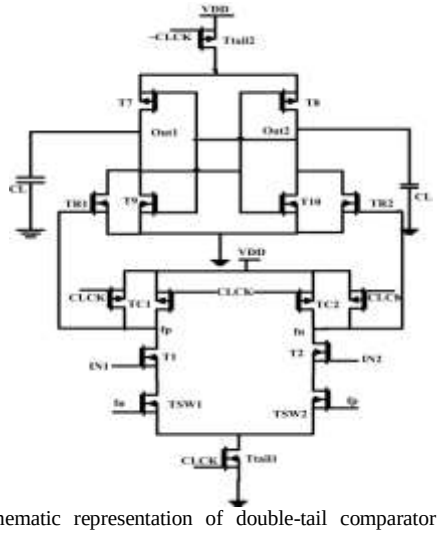

Figure.3. Schematic representation of double-tail comparator with control transistors

At a supply voltage of 0.8 V, comparator do not work properly with input voltage difference of less than 15m V. And for the same condition with the Input signal frequency less than 2.49MHz comparator do not get its threshold voltage, results in failure of operation.

III. SIMULATION RESULTS

In order to analyze the delay and power of typical Single-Tail comparator and double tail dynamic comparators, simulations are done in Cadence ® Virtuoso platform with 180nm CMOS technology for the constraints, input voltage difference and supply voltage.

Transient analysis of Typical Single-Tail comparator for a supply voltage of 0.8V, input voltage difference of 5mV, common mode voltage of 0.7V, sampling frequency of 900MHz, and load capacitance of 10f F is shown in Fig.4

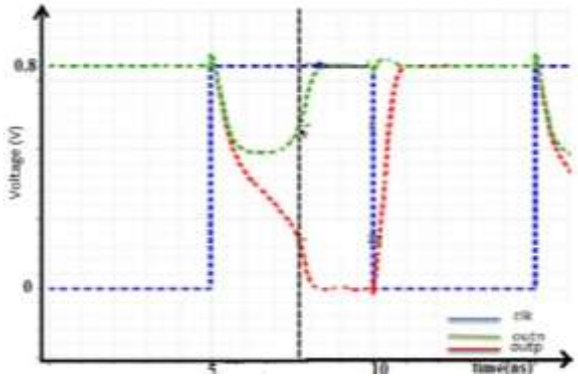

Figure.4. Transient analysis of typical single-tail comparator for Input voltage difference of 5mV, Vcm=0.7V, and V_{dd} =0.8V

TABLE 1 DELAY (NS)-TYPICAL SINGLE-TAIL COMPARATOR

Size of Input transistors(W/L)µm	2	4	6	8
Delay(ns)	4.974	4.306	3.248	2.9

In Typical Single-Tail comparator, as the difference in Input voltages increases, latch transistor get ON earlier, so that the fast latching regeneration independent of common mode voltage happen. Delay reduces as Input difference voltage increases. As the size of Input transistors increase, comparator makes a fast conversion, ie delay reduces. When size increases current through the transistors increases resulting Output voltages pulls to Vdd and ground easily. Table.1. Average power of the circuit is 3.38µW and energy per conversion is 33.8f.

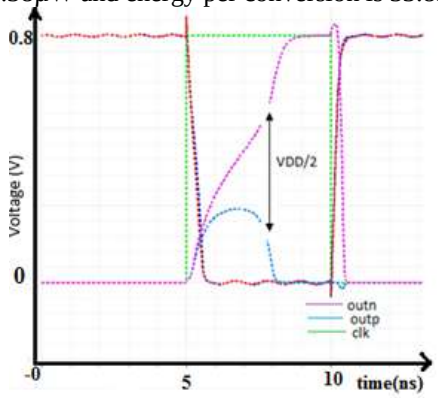

Figure.5.Transient analysis of traditional double-tail comparator

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Transient analysis of traditional double-tail dynamic comparator with a supply voltage of 0.8V, Input voltage difference of 15m V, common mode voltage of 0.7V, sampling frequency of 1.8GHz, and load capacitance of 10f F is shown in Fig. 5.

TABLE II. DELAY ANALYSIS OF TRADITIONAL DOUBLE TAIL COMPARATOR

	Delay(ns)				
W_{Ttail2}/ CLCK period	2 µm	4 µm	6 µm	8 µm	9 µm
5ns	3.889	3.512	3.115	2.911	2.838
15ns	4.380	3.512	3.115	2.911	2.838

In traditional double tail comparator delay analysis at input difference voltage=15mv, W_{Ttail1}=2µm is tabulated above Table.2. As the size of upper transistor increases, delay is getting reduced. But in this circuit static power dissipation occurs as there is direct rail-to-rail path.

Delay is getting more in double tail comparator than Typical Single-Tail comparator at same W_{Ttail1} of 2µm. For Typical Single-Tail comparator it is 2.522ns and for traditional double-tail compaator it is 3.889ns. For traditional double tail comparator delay can be reduced by increasing the size of top tail transistor Ttail2. Average power of the circuit is 4.306µW.

In double-tail comparator with control and switch transistors, both power and delay is reduced as compared with both typical single-tail comparator and traditional double-tail comparator.

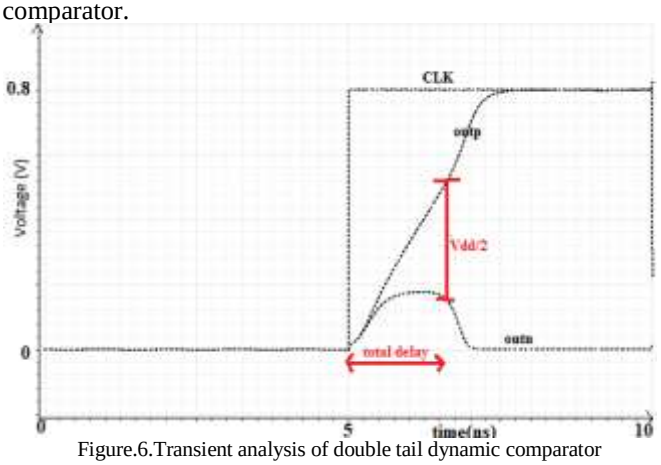

Figure.6.Transient analysis of double tail dynamic comparator

Transient analysis of double-tail comparator for a supply voltage of 0.8V, Input voltage difference of 15m V, common mode voltage of 0.7V, sampling frequency of 900MHz, and load capacitance of 10f F is shown in Fig. 6.

TABLE.III DELAY ANALYSIS OF DOUBLE-TAIL COMPARATOR FOR VARIOUS ΔVIN

ΔVin(mV)	6.1	10	20	30	50	100
Delay(ns)	4.97	4.16	3.18	2.38	2.17	1.58

Supply voltage and Input voltage difference are the main constraints which delay of the double-tail comparator depends on. As Input voltage difference increases switches will be operated faster and Outputs are pulled to V_{dd} and ground faster, so reduces the delay circuit .Table.3.

TABLE.IV DELAY ANALYSIS OF DOUBLE-TAIL COMPARATOR FOR VARIOUS W_2

W_2 (µm)	4	6	8	9	11
Delay(ns)	3.273	3.243	3.235	3.229	3.228

Impact of size of tail transistors on delay is less as compared with Typical Single-Tail comparator and traditional double-tail comparator. As the size increases delay is decreasing, but the rate of decrease is very less. Table.4. Average power of double-tail comparator is less compared with traditional double-tail comparator as there is no static power dissipation because of direct rail-rail current path. Average power is 3.47µW, less compared with traditional double tail comparator. Energy per conversion is 34.7f.

IV. CONCLUSION

In this work, we presented a comprehensive study on different types of comparator and its delay analysis. Delay analysis is done with various constraints being Input voltage difference, supply voltage, size of the tail transistors and size of input transistor. Amidst with input voltage difference and supply voltage circuits shows best delay variation.

Performance of a comparator used in ADC is assessed based on its delay and power. Compared to clocked regenerative comparator, traditional double tail comparator performs well as we size the tail transistors properly. Delay, power and energy per conversion signifies the effective functionality of the new double-tail comparator with traditional double tail comparator.

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