 ISSN: 2321-8169
102 - 105

Current Comparison Based High Speed Domino Circuits

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***Abstract*—**In order to achieve better performance we go for domino logic circuits, which cannot be obtained with the use of static logic circuits. In this paper, circuits for wide fan-in applications are proposed.It has better noise immunity and reduced leakage current without any degradation in speed. The technique which is used works on the basis ofthe comparison of worst case leakage current of pull-up network with the mirrored current of the pull-up network. The proposed technique decreases the parasitic capacitance on the dynamic node. To implement fast and robust circuits we can use smaller keeper transistors. As a result of this technique, the contention current is decreased and thereby delays and power consumption is reduced. The footer transistor is kept in diode configuration so the leakage current is reduced.It helps to achieve better noise immunity. The proposed circuit is compared with standard footless domino (SFLD), conditional keeper domino (CKD), high speed domino (HSD), leakage current replica keeper domino (LCR) and diode footed domino (DFD) based on the factors such as power consumption and delay.

***Keywords*—** *Power Consumption; Wide fan-in; Domino Logic; Noise Immunity;*

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INTRODUCTION

Domino logic is mainly used for high performance and high speed applications. Dynamic circuit's main limitation is that,cascading of dynamic circuits is not possible and voltage of dynamic node will be reduceddue to charge sharing. Domino logics play vital role in high fan in circuits. When the technology is scaled down, to obtain low power supply voltage is reduced and to have better performance threshold voltage is reduced. Leakage current will be increased as we decrease the threshold voltage. In new technology, major concerns are reduced leakage current and improved noise immunity[1].

In this paper,a circuit for wide fan-in applications is discussed. Which is current comparison based domino circuits (CCD). With the help of this circuit performance will be improved and power consumption and delay will be reduced.

I. DOMINO CIRCUITS

The most common domino logic circuit is the conventional standard footless domino (SFLD) circuit as shown in Fig. 1. Modifications are done in circuit level to improve the performance. Keeper transistor is given as a feedback from output. To maintain charge in dynamic node, the W/L ratio of keeper transistor is kept very low. The keeper transistor ratio K is defined as:

$$K = \frac{\mu_p \left(\frac{w}{l}\right)_{KT}}{\mu_n \left(\frac{w}{l}\right)_{EN}} \qquad (1)$$

Where, size of transistor is represented by symbols 'w' and 'l' and electron and hole mobility is represented by symbols μ_n and μ_p.

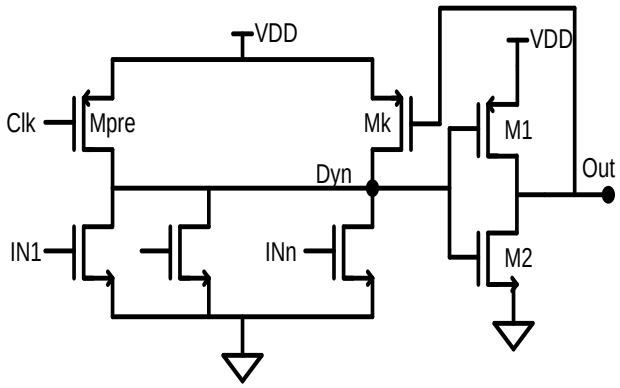

Figure 1. Schematic of 8 i-p OR gate using Standard Footless Domino Logic

Introducing keeper transistors decreases performance and increases power dissipation. Contention current will be there between the keeper transistors and evaluation network. Several techniques are introduced to rectify this issue[2]. Some of the techniques are mentioned here.

i) High Speed Domino Logic (HSD)

In HSD logic circuits, by applying clock delay contention current through keeper transistor and pull down network at the beginning of evaluation phase can be reduced. One of the main drawbacks of the circuit is that, leakage current in the circuit will not be affected by the extra circuitry, but it will consume extra power and area. HSD circuit is shown in Fig. 2. During precharge phase, clk is low, dynamic node will be precharged to Vdd. Transistor N_1 is off, P_1 is ON thereby charging the gate of $Q_2$to Vdd thus turning Q_2 off at the beginning of evaluation phase. During evaluation phase, clk is high, if any one of the pull down transistors is ON, domino node will discharge to "0" and output will be "1". If all the pull down transistors is OFF, dynamic node will remain at 1 thereby causing the output to be "1" [3] [4].

 ISSN: 2321-8169
102 - 105

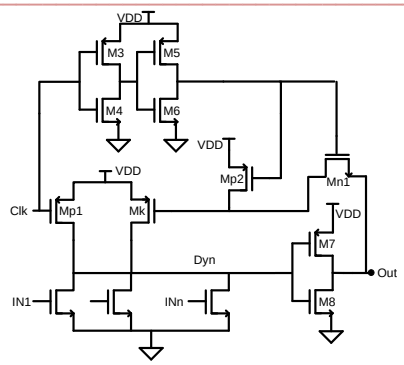

Figure2.Schematic of 8 i-p OR gate using HSD Logic

ii) Leakage Current Replica Keeper Domino (LCR)

The schematic of LCR circuit is shown in fig.3. A circuit with LCR keeper includes one extra series pFET and a shared replica current mirror. The current mirror circuit tracks the leakage current and it is copied into dynamic gate through transistor P_1. Assume that, I_{leak} is the leakage current of the dynamic gate, we use current mirror circuit to draw sf* I_{leak}, sf is the safety factor.ofnFET. NMOSnrpl is used in current mirror is to determine the worst case leakage current. By ratioing the transistor sizes the safety factor (sf) is set. Assume that transistors p_1, $p_3$and all nFETshave same channel length,then, 'sf' is given by:

$$sf = \frac{W_{nrl}}{\sum W_{ni}} * \frac{W_{p1}}{W_{p3}} \qquad (2)$$

W_{nprl}, W_{p1}, $W_{p3}$and W_{ni}denotes the width of transistors nprl,p_1, $p_3$and ni(i=0,…..n) [5][6].

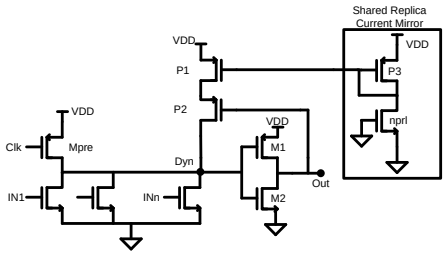

Figure 3.Schematic of 8 i-p OR gate using LCR Logic

iii) Diode Footed Domino (DFD)

The schematic of a DFD circuit is shown in Fig. 4. The SFLD logic circuit is modified by adding nmos transistor which is in diode configuration in series with the pull down network. The diode footer configuration decreases the subthreshold leakage due to stacking effect.There is some voltage drop across the diode connected transistor due to the leakage of pull down network.Body effect of the pull down transistors is increased due to the voltage drop across the diode transistor. This in turn helps in the reduction of sub threshold leakage. Performance of the circuit is degraded as diode footer configuration decreases the evaluation current. Mirror transistor is used to increase the performance of the circuit.

During precharge phase, transistor M3 is ON, which in turn turns off the M2 transistor. Short circuit through M2 transistor during precharge phase will be prevented. Output value drives the transistor M4. If the output is high during the evaluation phase,it will pull down the footer and precharge node to zero, thereby preventing any short-circuit power consumption during the evaluation phase in the inverter. As leakage power is reduced, only small sized keeper is needed. Upsizing the keeper transistor in SFLD circuits has the same effect as downsizing the mirrortransistor in diode-footed domino [7].

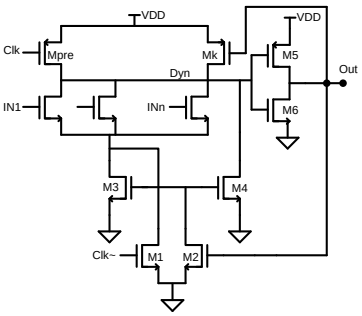

Figure 4. Schematic of 8 i-p OR gate using DFD Logic

iv)Conditional Keeper Domino (CKD)

The CKD circuit schematic is shown in Fig. 5. It consists of two keeper transistors. K1 transistor is the smaller keeper and K2 transistor is the larger keeper. As long as dynamic node is high, transistor K1 will be ON. At the beginning of evaluation phase, transistor K2 will be OFF. If the dynamic node is at high value for certain duration, the NAND gate output will be low and it will turn on the keeper transistor K2, therefore for the remaining evaluation phase, precharge node will remain at high. As we decrease the keeper delay,there will be improvement in leakage tolerance. As there is a limit on decreasing the keeper delay, this technique is limited. As the inverter is directly connected to the clock signal, power consumption will be increased if we try to reduce the keeper delay by increasing the size of inverter transistors. As the delay of inverter is sensitive to process variation it will make the performance and robustness of the circuit unpredictable [8] [9].

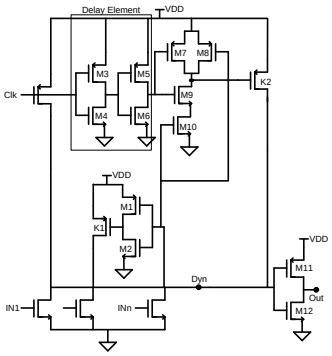

Figure 5. Schematic of 8 i-p OR gate using CKD Logic

III.CCD LOGIC DESIGN

The schematic of a CCD logic topology is shown in Fig. 6. As the number of inputs increases, dynamic node capacitance will be of larger value thereby reducing the speed. Noise immunity will also get reduced as the number

 ISSN: 2321-8169
102 - 105

of leaky paths increases. Noise immunity can be improved by adjusting the size of keeper transistor. Delay and Power consumption are also increased due to the effect of larger contention current. All the above mentioned problems can be corrected if we separate the pull down network from the keeper transistor. This can be done by using a comparison stage in between them where the current through the pull network will be compared with its worst case leakage current. [1].

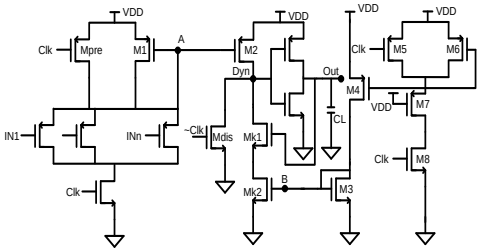

Figure 6.Schematic of 32 i-p OR gate using CCD Circuit

There are two phase of operation: i) precharge phase ii) evaluation phase.

i) Precharge phase:

Clock and input signal voltages are kept at lower and higher levels respectively. Voltage at dynamic node is reduced to a low value with the help of transistor M_{dis} and voltage at node A is raised to higher value with the help of transistor $M_{pre.}$ M_{pre}, $M_{dis,}$ M_{k1} and M_{k2} transistors are in ON state while the$M_{1,}$ M_2 and M_{elav}transistors are in OFF state.

ii) Discharge phase:

Clock signal is kept at higher value whereas the input signals can be either in higher or in lower levels. M_{dis} and M_{pre}transistors are at OFF state and $M_{1,}$ $M_{2,}$$M_{elav}$ and M_{k2}transistors are at ON state. If all the input signals are kept at higher value, then small amount of voltage will be established across M_1 due to leakage current. Keeper transistors in the circuit will compensatethe mirrored leakage current. If at least one of the transistors input is low, pull up current will be raised and voltage of node A will be decreased to lower voltage value. Dynamic node is charged to Vdd therefore output voltage will be decreased, thereby makingM_{k1} OFF.

IV.RESULTS AND DISCUSSIONS

The transistor size of CCD logic circuit for 8-,16-,32- and 64-bit OR gate are shown in Table 1.

The transient response of 32 i-p OR gate using CCD logic is shown in Fig. 7. Supply voltage of 1.8V is given to the circuit. In the simulation, only one of the inputs of the OR gate falls to lower level during the evaluation phase. Load capacitance C_L = 5fF. Clock is given as low to high i.e., during precharge clock is '0' and during evaluation clock is '1'. When clock is '0' dynamic node will be precharged to Vdd so output node will be '0'. When the clock turns '1', dynamic node will be discharged, as one input of the OR gate is in high level. So the output turns '1'.

TABLE I. Size of all transistors of proposed circuits for 8-,16-,32- and 64- bits OR gate

Fan-in	Wk1(nm)	Wk2 (nm)	Wpre (nm)	Weval(nm)	Wdis (nm)	W1 (nm)	W2 (nm)	W3 (nm)	W4 (nm)	W5 (nm)	W6 (nm)	W7 (um)	W8 (nm)
8	400	400	400	400	400	400	500	400	400	400	400	1	400
16	500	400	400	400	400	400	500	400	400	400	400	1	400
32	500	600	400	400	400	400	500	400	400	400	400	1	400
64	400	400	400	400	400	400	400	400	400	400	400	1	400

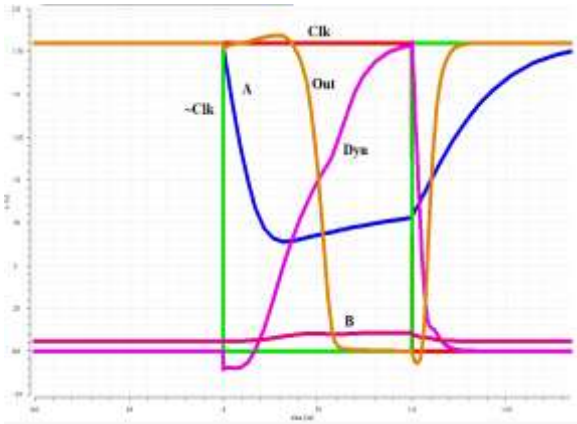

Figure 7. Transient response of 32 i-p OR gate using CCD Circuit

Fig. 8 shows the transient response of 8 i-p OR gate SFLD, HSD, LCR, DFD and CKD circuit. Supply voltage is given as 1.8V. All the inputs of the OR gate falls to high level during the evaluation phase. Clock is given as low to high ie, during precharge phase clock is '0' and during evaluation phase clock is '1'. When clock is '0', dynamic node (Dyn) will be charged to Vdd so output node will be '0'. When the clock turns '1', dynamic node will be discharged to low value as all inputs of the OR are in high level making the transistors ON. So the output turns '1'.

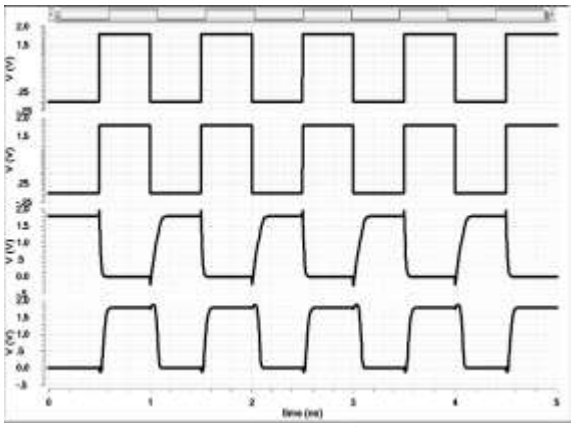
Figure 8. Transient response of 8 i-p OR gate

ISSN: 2321-8169
102 - 105

Power consumption and delay comparison of 8 i-p, 16 i-p, 32 i-p and 64 i-p using SFLD, HSD, LCR, DFD and CKDlogics are done. Values of power consumption comparison are shown table 2. Values of delay are shown in table 3.

TABLE II. Comparison of power consumption of various domino circuits (μW)

Fan-in	SFLD	HSD	LCR	CKD	DFD	CCD
8	146.8	201.5	123.9	361.2	200.9	70.55
16	198.0	239.7	159.7	391.3	396.6	74.87
32	369.4	313.8	230.3	463.5	466.1	78.00
64	387.7	443.6	355.1	597.0	643.8	87.21

The table.2shows the comparison of power consumption in various domino logic circuits. From the table we can understand that CCD logic circuits are having the least power consumption. It is showing a reduction of 51% to 77% when compared with the SFLD logic circuits. DFD logic circuits are having the highest power consumption. By seeing the table we can also understand that, as the number of inputs increases, power consumption also increases. Fig. 9 shows the graphical representation of power consumption by various domino logic circuits.

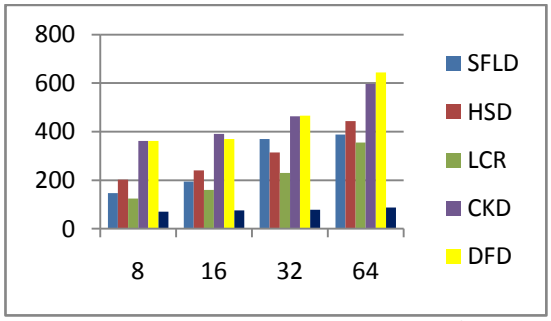

Figure 9. Power consumption variation with no. of inputs

TABLE III. Delay comparison of various domino circuits (ps)

No. of I/Ps	SFLD	HSD	LCR	CKD	DFD	CCD
8	75.58	70.18	73.80	78.3	76.42	60.21
16	102.5	100.8	100.5	112.4	109.3	97.23
32	189.6	157.7	152.0	170.2	167.4	141.6
64	252.9	259.1	250.3	271.5	260.2	242.1

The table.3 shows the comparison of delay in various logic circuits. From the table we can understand that CCD logic circuits are having the least delay. It is showing a reduction of 5% to 25% when compared with the SFLD logic circuits. CKD logic circuits are having the highest delay. By seeing the table, we can also realize that as the number of inputs increases, delay also increases. Fig. 10 shows the graphical representation of delay by various domino logic circuits.

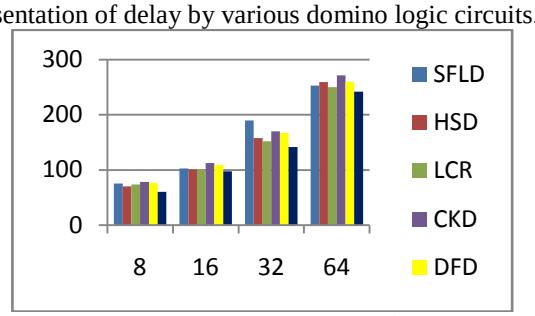

Figure 10. Delay variation with no. of inputs

V. CONCLUSION

This paper details the design of current comparison based domino logic circuit. As technology scales down, leakage current also increases, especially in the case of wide fan-in domino gates. This will lead to increased power consumption and reduced noise immunity. As the number of fan-in increases, contention current between keeper transistor and pull down network also increases. The CCD logic circuits overcome all these problems to certain extend. Thecircuit has higher performance as well as lower power consumption and delay when compared to standard footless domino, high speed domino, leakage current replica keeper domino, diode footed domino and conditional-keeper domino. Thus, the proposed circuit is suitable for implementing wide fan-in operations with better noise immunity, lower power consumption and time delay.

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