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Sleepy Keeper Approach: Performance Comparison of CMOS and TFET for adder circuits

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***Abstract*—**As technology is scaling down into deep submicron range, leakage power became one of the major issues in designing the high performing circuits. So leakage power (static power) dissipation along with dynamic power is playing a major role in the total power dissipation of a circuit. Different techniques were proposed and implemented over the time, but single has certain disadvantages. So This paper proposes a technique called sleepy keeper. Which is a advanced version of previously used technique of sleep transistor. In which we are using two more transistors in order to maintain the proper state of output, as floating output was one of the main disadvantages of sleep transistor approach.

Based on this technique we are designing 1 bit full adder circuit since full adder is one of the important circuits in digital processors. Here we are using both CMOS and TFET in 45nm technology in cadence virtuoso -64 tool. The static power dissipation, propagation delay and dynamic power are analyzed. It is observed that sleepy keeper approach performs better in terms of static power dissipation.

Keywords*—*Sleep Transistor; Full adder; Keeper transistor; Static Power dissipation; TFET.

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I. INTRODUCTION

In order to achieve high performance and area compaction technology is getting scaled down very rapidly. Therefore supply voltage needs to be scaled down and hence threshold voltage (V_{th}) is also scaling down. With less threshold voltage subthreshold leakage is becoming major issue in designing the VLSI circuits. Adder is a core element of arithmetic circuits and used in all types of processors. To reduce the static power dissipation various techniques were introduced time to time like Sleep transistor, Zig-Zag, leakage feedback [1] but each technique has its own limitations. Though CMOS plays a dominating role in digital market but to fulfill the requirements of growing market and expecting better performance in terms of power, area and functionality there is strong need of new type of device which gives better performance. Tunnel FET (TFET) is emerging as one of the promising device as a replacement of conventional MOS technology. TFET is a reversed biased p-i-n tunnel diode with different source-drain doping, with which we can achieve desired I_{on}/I_{off} over a low V_{dd} range. Moreover using TFET higher I_{on}/I_{off} ratio can be achieved. Therefore this paper gives the detailed analysis 1-bit full adder circuit using a new technique called Sleepy Keeper approach [2] and compared its results with previous techniques using both CMOS and TFET.

II. PREVIOUS WORK

In this section we review the base case and previously proposed approaches for leakage power reduction.

A. Base Case

The base case circuit is nothing but conventional basic complementary metal oxide Semiconductor. In this all the P-type and N-type transistors are placed complementary to each other. There is no special leakage power reduction technique in this conventional style [3].

B. Sleep

This is very popular approach for leakage power reduction. In this approach power gating technique is used, where two additional transistors one is P-type which is placed between V_{dd} and pull up network and other is N-type placed between GND and pull down network. The main purpose to use these extra transistors is to cut off the rail to rail connection when the circuit is in standby mode. Two extra transistors used are known as sleep transistors. So when the circuit is in active mode these sleep transistors gets turn on giving desired result with reducing delay, and when in standby mode gets turn off resulting low leakage power. The main disadvantage of this technique is that while transitioning from sleep mode to active mode it gives floating output states [3]. So there is need for another suitable approach.

C. Leakage Feedback

This approach was proposed to maintain the proper logic state during standby mode. This approach is based on sleep approach with two additional transistors. The input to these transistors is the output of an inverter which is driven by output of the circuit. The P-type transistor is placed parallel to header sleep transistor while N-type transistor placed parallel to footer sleep transistor. During standby mode sleep transistors are turned off but one of the transistors connected parallel to these sleep transistors will keep its connection to proper power rail. The main disadvantage of this approach is increase in area with additional inverter circuit.

III. TFET

The structure of TFET is almost same as that of MOSFET expect the middle intrinsic layer, the only thing TFET differs from MOSFET is its working mechanism. MOSFET switching mechanism is based on thermionic emission whereas TFET works on the principle of band to band tunneling (BTBT).

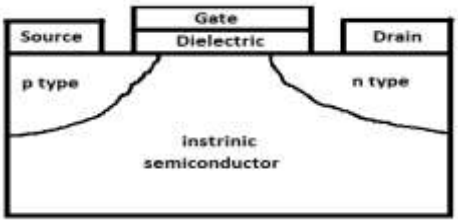

Fig.1 Basic structure of p-i-n TFET

 ISSN: 2321-8169
99 - 101

We can see in Fig.1 that there is intrinsic layer between source and drain. In TFET conduction band of intrinsic (i-region) region is aligned with the valance band of P region, when this occurs and after sufficient gate bias is applied the band to band tunneling is said to occur. The main reason behind TFET is better than MOSFET is the small subthreshold swing provided by TFET because of its band to band tunneling mechanism which gives less off current and very low power dissipation.

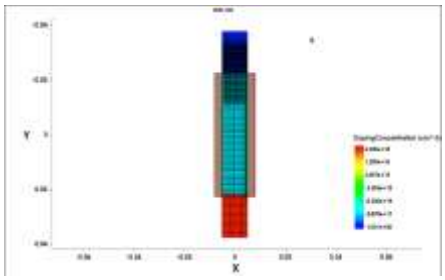

Fig.2 Structure of TFET.

Fig.2 shows the basic structure and doping concentration of 45nm Tunnel FET created using TCAD simulation. Hafnium oxide i.e. HfO_2 is used for gate isolation.

The material InAs is a low bandgap material which ensures high tunneling current. The improvement of gate control on electron tunneling can reduce the subthreshold swing [6]. So greater I_{on}/I_{off} ratio, higher g_m/I_{DS} and lower subthreshold swing are the main reasons behind considering TFET as strong replacement of MOSFET [7].

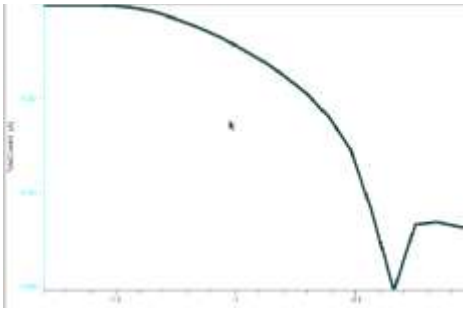

Fig.3 I_d Vs V_g plot of PTFET

Graph between gate voltage and drain current simulated in 45nm TFET technology for both PTFET and NTFET is shown in above figure Fig.3 and Fig.4 respectively.

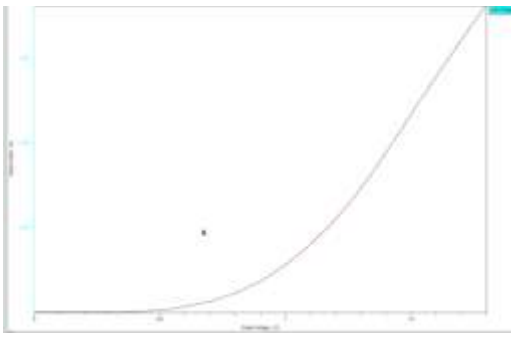

Fig.4 I_d Vs V_g plot of NTFET

IV. PRAPOSED FULL ADDER

A. Sleepy Keeper Approach.

In this section we describe the proposed technique for static power dissipation reduction and maintaining the proper state of output. As we can see in the following Fig.5 sleepy keeper is just a advanced version of sleep transistor approach. Two extra transistors one is P-type transistor which is connected parallel to footer transistor with one terminal connected to ground and second is N-type transistor connected parallel to header transistor with one terminal at VDD. The main reason behind using these two extra transistors is to avoid the floating output, which was the major disadvantage of previously used sleep approach. These two extra transistors are called as keeper transistors.

The input to keeper transistor is nothing but the already obtained output of the main logical circuit.

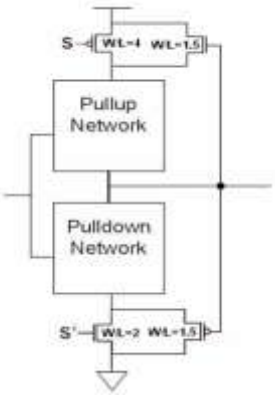

Fig.5 Sleepy Keeper Approach

To maintain the proper output state, suppose output of circuit is 1, so in sleep mode the N-type transistor which is connected to VDD will turn ON and it will maintain the proper output 1 and at the same time P-type transistor will turn OFF so avoiding rail to rail connection. Similarly to keep the value 0, P-type transistor will turn ON which is connected to ground will maintain the proper 0 value avoiding rail to rail connection.

Therefore using all the four techniques that is base case, sleep transistor, leakage feedback and sleepy keeper we simulated the 1 bit full adder circuit and calculated the propagation delay, static power dissipation and dynamic power dissipation in cadence virtuoso -64 tool. Following Fig.6 shows the 1 bit full adder circuit using sleepy keeper approach.

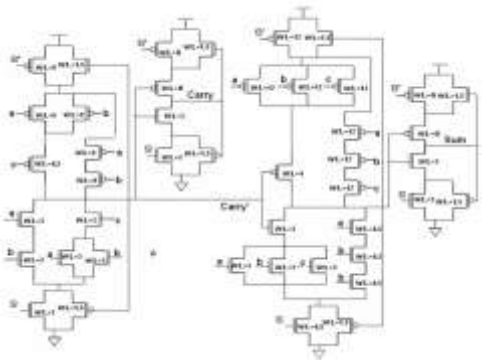

Fig.6 1 bit Full Adder Cell with sleepy keeper approach

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99 - 101

B. Methodology Used.

The main challenge in this approach is to size the sleep transistor in a proper way so that minimum leakage should be there. Therefore we should size the sleep transistor in such a way that minimum leakage should be there, so to obtain minimum leakage current V_{th} that is threshold voltage of the sleep transistor should be more. In order to achieve that we should make sleep transistor a little bit wider. But problem with wider sleep transistor is that, when device goes from sleep mode to active mode the sleep transistor wakes a little late compared to rest of the circuit and this causes floating output hence we have to go for keeper transistor.

For keeper transistor width should be small in order to achieve less current as I $\propto$ (W/L). Considering the delay, normal delay calculation is done using following formula [4].

$$\tau_d \propto \frac{C_L V_{DD}}{(V_{DD} - V_{T_L})^{\alpha}}$$

The delay of gate with sleep transistor is expressed as.

$$\tau_d^{sleep} \propto \frac{C_L V_{DD}}{((V_{DD} - V_{sleep}) - V_{T_L})^{\alpha}}$$

Where V_{sleep} is nothing but voltage of new virtual rails. So using sleep transistor propagation delay of circuit decreases. However there is a little increase in the delay in case of sleepy keeper compared to base case.

V. Simulation Results

We calculated the worst possible delay, static power dissipation and dynamic power dissipation for base case, sleep transistor approach, leakage feedback approach and sleepy keeper approach. We did the simulation using both CMOS and TFET with 45nm technology node and observed the results. We choose 1-bit full adder to compare our simulation results. Following Fig.7 shows the output of adder circuit with power signal in it. We can observe that all possible input patterns have been carried out, and design have properly responded to different input patterns.

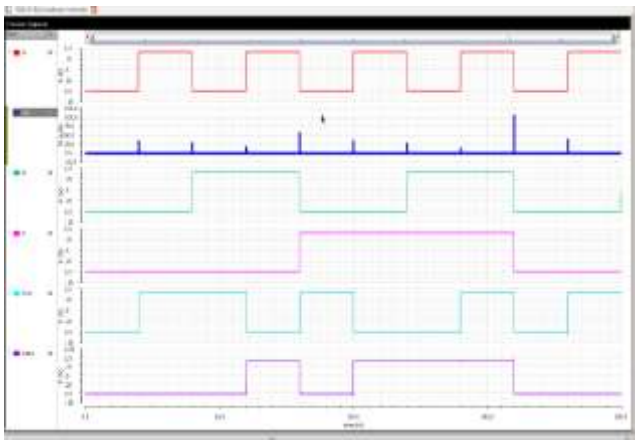

Fig.7 Simulation Results of 1-bit Full Adder

Following TABLE.1 shows the performance analysis of this design in terms of static power, dynamic power and propagation delay of both CMOS and TFET with 45nm technology node.

TABLE. 1 Performance Analysis

Technology	CMOS 45nm			TFET 45nm		
Approach	Static Power	Dynamic Power	Delay	Static Power	Dynamic Power	Delay
Base Case	18.60pW	26.53uW	40.05 nS	8.64pW	21.63uW	39.98nS
Sleep	5.324pW	29.16uW	20.00 nS	1.547pW	31.843uW	12.856 nW
Leakage feedback	45.32pW	93.95uW	184.4 nS	78.564 pW	63.452uW	87.253 nW
Sleepy keeper	0.919pW	43.57uW	8.133 nS	0.234pW	35.412uW	13.523 nW

VI. Conclusion

In this paper low leakage approach called Sleepy Keeper is presented, compared with other approaches like base case, sleep and leakage feedback for proposed 1-bit full adder using both CMOS and TFET. Based on the result analysis it can be concluded that sleepy keeper approach result in low static power dissipation saving the proper output states little increase in propagation delay compared to sleep transistor approach. Observing above results it can be stated that TFET give better ultra low power performance compared to CMOS and can be considered as a replacement for MOSFET.

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