Analysis and Design of a Current Mirror Trans-conductance Switchable Op-amp for Switched-Capacitor Integrators

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Abstract **–** A switchable operational amplifier (op-amp) that uses a switched capacitor integrator has an advantage such as low power consumption and wide gain-bandwidth product. The power reduction is achieve by apply switching samples at the input and output capacitors. These capacitors can be otherwise would contribute in increase in power consumption. During the first phase of the sample the opamp completely turned off, at this instance the input capacitor is fully charged, which later can be used to drive the opamp. On the next second sample phase charged energy in input capacitor passes through the integrator capacitor, which turns on the opamp. On the second clock cycle of the first phase the output of opamp is fed to the output capacitor. Measurement of 1volt switchable opamp for switched capacitor integrator show 44 dB dynamic range in bandwidth of 30 KHz with 52dB peak SNR and the power consumption of 186 microwatt.

Index Terms **-** *Circuits, operational amplifier (opamp), switchable opamp, switched capacitor (SC), switching.*

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I. INTRODUCTION

In this age where the market for mobile electronic systems such as wireless devices, consumer electronics, etc., is elaborating continuously, there is a tending requirement for the growth of low power and low voltage circuit strategies and system blocks. For portable applications the circuit operates with both low voltage and low power.

The low voltage of portable devices is on a high demand because they operate with less battery dimensions and weight. The battery lifetime increases with low power consumption. Certainly implementation of robust way in integrator is with switched-capacitor tactics. Their linearity and robust combined makes SC techniques. The high quality SC properties would be a advantage. However the problem with design for low power and voltage is switch-driving problem. The low supply voltage does not enough Vgs to turn on the transistor, where used as switches.

II. THE SWITCHED OPAMP TECHNIQUE

The technique of switched op-amp allows us to design SC circuits without using low threshold devices. It is observed from classic SC integrator, switches are classified into two firstly, switches which has one of its terminals fixed to a reference voltage or grounded and secondly the switches which has to transfer the total signal range, which are generally found at op-amp output. The aim of the switched op-amp to switches can be connected to either reference voltage or ground. The integrator shown in figure 1.

The switches are leaved for few consequence operating periods. During the integration, of the next stage output is grounded. This operation results the opamp is temporally off. The second consequence the switch is activate the integrator that we called as half delay mode.

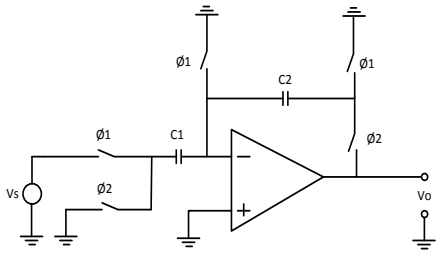

Figure 1: the half delayed SC integrator [9].

The conventional switched op-amp technique makes a better choice to take the input voltage level and it equal to output voltage level. The both voltage levels are at reference voltage. As a consequence phases, the output voltage swing is less than the available swing and the maximum possible in less switch over drive voltage.

III. THE LOW VOLTAGE BUILDING BLOCKS

In this section the building blocks are discussed for the design for low voltage.

A. Current mirror:

The simple current mirror circuit is used in designing of opamp first stage [9]. The one transistor is connected in diode mode and the both gates are connected, that means the output current is factor of input current by self-gain of device. When the unity gain attained the total input current passes to output as the load current. This is called as current mirroring.

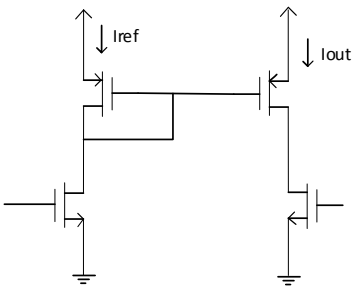

Figure 2: current mirror circuit [9].

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Under ideal conditions as shown in figure 2, the gain of the current mirror is independent to input frequency and output current is independent of voltage between output and common terminals. In ideal condition, the voltage between these two terminals is zero because the entire supply voltage is applied to current source.

B. Differential pair

In current mirror mode the gate voltage of Vg is fixed at current input node. If an additional transistor is added and it is connected to the input of current mirror with a source, this source voltage must be fixed.

If the input signal is fed at the gate of added transistor, a current is generated and added to current mirror current at output. If two voltages is applied to Vin+ and Vin- terminal the different of voltages is presented at bottom transistor as shown in figure 3[9]. The nmos driver is gives easy control of the output swing. But output swing at the threshold of that transistor.

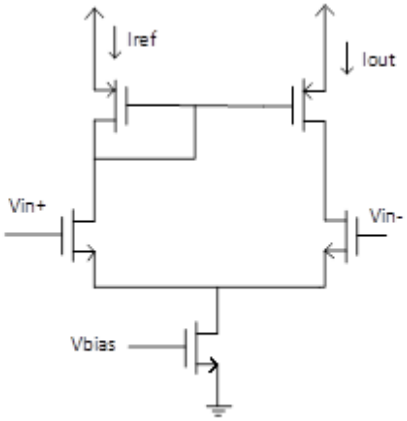


Figure 3: differential pair with nmos driver [9].

IV. OPAMP WITH SWITCHABLE TRANSCONDUCTANCES

The proposed current mirror opamp has an input trans conductance *Gm*, and total transconducatnce *KGm*, where *K* is the current gain [9]. Total output transconducatnce and its load is separated into two parts which in difference in 70% of *Gm* at one part and another 25% *Gm* at other part. The high *Gm* and its load is switched off during first sample pluses. The lower *Gm* is on all the time. The op-amp was designed for half-delay SC integrators as the output voltage is available at both the sample cycles.

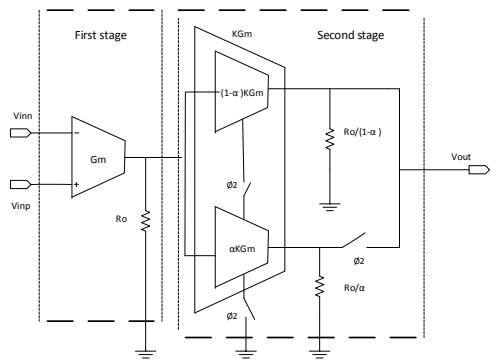
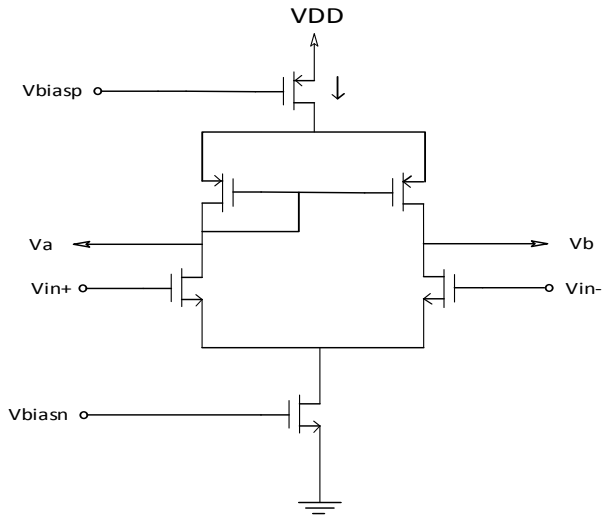


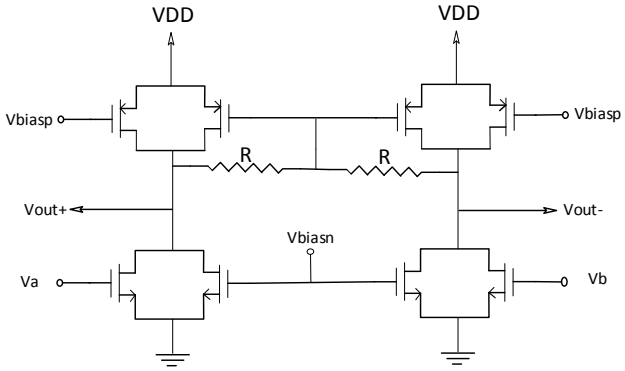
Figure 4: switchable transcoductance op-amp with first stage and second stage has divided into two [1].

V. DESIGN OF SWITCHABLE OPAMP

Consider a typical current mirror having a current gain of K. To design the switchable op-amp the output of the current mirror or current source transistor is divided with a ratio of α to $(1-\alpha)$. The α part is switched on while $\varphi 2$ pulses and off at $\varphi 1$. The output current is switched from *KIB* during $\varphi 2$ to $(1-\alpha)$ KI_B during $\varphi 1$. The achievable power reduction determined by the α and K. In the case of a half delayed integrator, the maximum switching α is limited by time required to turn on the opamp to restore the current at output node. Where as in fully delayed integrator the output capacitor is connected during the sample phase. The maximum value of α is depends on output capacitor.



(a)



(b)

Figure 5: circuit of opamp, (a) first stage [1] and (b) second stage [9].

Consider $K_I = C_2/C_1$ is the integrator's gain and current mirror opamp with G_m as trans conductance used in fully delayed mode of operation. Neglecting the parasitic capacitances, the feedback factors in two sample phases as β_1 and β_2 are:

$$\beta_1 = C_2/C_2 = 1 \quad (1)$$

$$\beta_2 = C_2 / (C_1 + C_2) \quad (2)$$

For the fully delay mode the load capacitance values during the both sample phase are:

$$C_{L2} = (C_1 C_2) / (C_1 + C_2) = \beta_2 C_1 \quad (3)$$

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$$C_{L1} = C_{1,\,next} \quad (4)$$

The closed loop time constant are:

$$T_2 = C_{L2} / \beta_2 G_{m2} \quad (5)$$
$$T_1 = C_{L1} / \beta_1 G_{m1} \quad (6)$$

Where $G_{m2} = G_m$ and $G_{m1} = (1- \alpha) G_m$

At the end of the phase 2 the output voltage is while step input applied with settling time T_{set} of op-amp

$$Vout = K\,Vin\_step\left(1 - e^{-\frac{Tset}{T2}}\right) \quad (7)$$

And

$$Vout = K\,Vin\_step\left(1 - e^{-\frac{Tset}{T2}}\right)\left(1 - \left(\frac{CL1}{C2 + CL1}\right)e^{-\frac{Tset}{T2}}\right) \quad (8)$$

VI. RESULTS

The switchable opamp was designed in a 1-V 45 nm CMOS process, with a current gain of K = 16, to achieve the following specifications.

- dc gain A_0 = 50 dB
- Unity gain bandwidth f_T = 272MHz(at CL=1pF)
- Phase Margin PM = 45^0 (at feedback factor 0.8)

Then it was designed for half delay SC integrator with following specifications.

- Sampling frequency = 125 MHz
- Sampling capacitor = 1.5pF
- Integrator gain = 1
- Next stage sampling capacitor = 0.5pF.

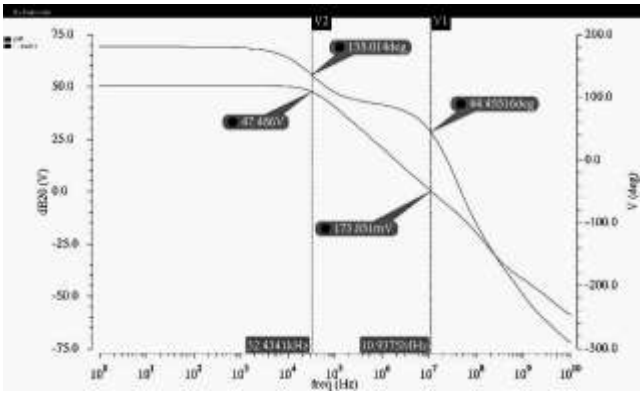

Figure 6.1: AC response of the opamp.

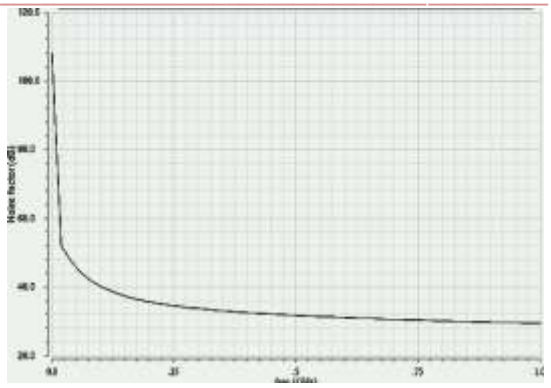

Figure 6.2: Input Noise (in dB) of opamp.

VII. CONCLUSTION

This work discuses on the design and analysis of the current-mirror op-amp with switchable transconductance values. Circuit operation and design details were as explained. Power saving optimization with switchable opamp method is performed.

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