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Built in Self-Repair Scheme for 3D SRAM Memories

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***Abstract*—** Today's world technology increasing day by day and in the memories progressing is required. Uses of more application, industry want additional memory size but if the size increased it may be affected to the power & area so that's why 3D memories are better option. In memories some time the faults are present, to reduce the affect of the fault the testing algorithms is generally used. There are many algorithms are use to reduced or repair the fault. Like BIST (Built in self test) Detect the fault if fault is available on particular location and BISR (Built in self repair) it use for repairing the memory cell with a spare cell memory.

Keywords- *SRAM, BISR, BIST, ORC, CUT, 3D MEMORIES*

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I. INTRODUCTION

Memory is a one type of storage device. It used for read and write operation. In market number of memories is available like-SRAM (static memory), DRAM (dynamic memory), both memories are random access memories .Flash memory EPROM (Erasable programmable read only Memory), (electrical programmable read only memory).for study purpose SRAM is easy to understand. In SRAM many models are their example 6T SRAM cell, 8T SRAM cell, 9T SRAM cell and 10T SRAM cell. In the 6T SRAM cell two invertors is connected in feedback. Enabling WL (world line) it's directly depend upon the output to the given corresponding inputs. For write operation there are none of extra circuitry required. But for read operation have to need sense amplifier. First individual cell made then array will develop by one single cell. For 2D array of size should be less compare to the 3D.Use for number of application at a one time the 3D memories are better option. It can reduce the power and its look like a cube.

3-D SRAM Memories communicate more efficiently with processing unit of processor increasing the performance. According to area, power and size 3D is much better to used for storage multiple applications. [1]

To make 3D memories become more critical. Increased a number of cell in one memory and transfer one memory into array is a difficult process. Different process might lead to new inter_die & TSV (Through silicon via) related defect. [1]

After building the memory the next step is fault testing, in these need to give possible number of inputs and measured if fault is detected or not. Detecting the fault is not an issue but modified or repair the fault is the important task. There are many methods to test and repair the fault, for test the coding styles is present. March C and March C- algorithms for testing also preferred for testing. Both March C and March C- are different fault detection techniques. For testing and repairing the memory cell there are two main techniques 1.BIST (Built in self-test) 2. BISR (Built in self repair) both are very useful designed for detecting and repairing memory. Going for 3D testing is tuff job because of the memory layers,each and every layer should be check , row and column vise and detect the fault for repair the cell require spare cell. The size of the spare cell should be same as the size of the memory cell then and then if the fault will be present in faulty cell it can replace with the spare cell. Carful about spare cell memories because when the memory will be replace with the faulty cell the address of the both memory location should be same then and then go for further procedures . [3][7]

II. BACKGROUND

A. Various Fault present in SRAM Memory.

SRAM Fault are categorized below 1)Stuck at Fault 2)Transition Fault 3)Coupling Fault 4)Coupling idem potent Fault 5)Coupling dynamic Fault 6)Bridge fault

1). Stuck at Fault: - Stuck at Fault defined as s_a_0 (stuck at zero fault) and s_a_1 (stuck at one fault) through their wire connection if it connected to VDD then s_a_1 fault will be detected or it connected to GND then s_a_0 fault will be detected.

2). Transition Fault: - Transition fault occurs when the (0 to 1) and (1 to 0) transition detected. If the transition occurs (0 to 1) it will detect rising fault and if the transition occurs (1 to 0) it will detect falling fault in the cell.

3). Coupling Fault: - Definition of coupling fault is when the variation occurs in j(coupling cell) cell it can be affected i(coupled cell) cell. < i,j >.

4). Coupling idem potent Fault:-It can be use for modified inversion coupling fault. Also defining new cell value.

5). Coupling dynamic Fault:-various changes occur in the cell its called coupling dynamic fault.

6). Bridge fault:- It occurs when any two wire will be short circuited .different types of bridge fault detected AND bridging fault ,OR bridging fault both will be depending upon their controlling value. Like for AND controlling value should be 0 and for OR controlling value should be 1.

7). Neighborhood pattern sensitive Fault (NPSF):-

Two type of neighborhood pattern sensitive fault occurs (1) Active NPSF

(2) Passive NPSF

Cell under test not change due to present of other cell. One cell creating disturbance and second cell will affected its call NPSF.

8). State coupling Fault: - It is similar to coupling fault. When the state changes it can be affected by coupling or coupled cell.

B. Built in Self-Test (BIST)Techniques.

Practical solution to the problem of testing Self Test (BIST) techniques constitute an attract VLSI circuits and systems. Input pattern monitoring concurrent BIST schemes input vectors arriving at the inputs of the Circuit Under Test (CUT) during normal operation Input pattern monitoring Concurrent BIST schemes are applicable to combinational CUT's and detect all permanent (as well as some of the transient) combinational (stuck-at) faults at the CUT(circuit under test)

C. Built in Self-Repair (BISR) Techniques.

The BISR is repair the memory which is reference good cell. A reconfigurable BISR circuit is realized to perform and the experimental results show that the BISR scheme can achieve high repair rate. Repair rate is the ratio of the number of repaired memory cell to the number of defective memory cell.

The area cost of the reconfigurable BISR is very small. [4] [8]

D. 3D Memory Architecture

3D Architecture of memories is achieved by the stacking layers of 2D memories. Stacked layers may be interconnecting by many ways; most common approach is wire bonding between the layers of 2D memory die. Up to few layers this method of stacking is effective but as the number layers increases the interconnect density is also increases and the wire bonding is only possible on the periphery of the IC. TSV (through silicon via) is the latest approach to provide high density of interconnection. Another approaches are Microbump in which bump are created on the surface of the die to make the interconnection between memory layers, and Contacless inductive or capacitive coupling between the die.[1]

III. SRAM READ AND WRITE OPRATION

Embedded memories various type of SRAM cells are available. Here, the 6T SRAM cell is used, implementation of 6T SRAM is very important to find possible faults in cell and also reduced that faults. In the write operation bother about only word line according to Fig. 1 If word line will high because here are already some value inside the memory and all function performance will be good and then its give accepted output. Fig 2.

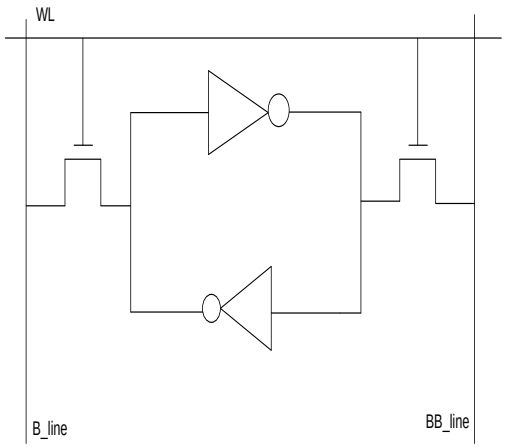

Fig 1. SRAM Memory Cell

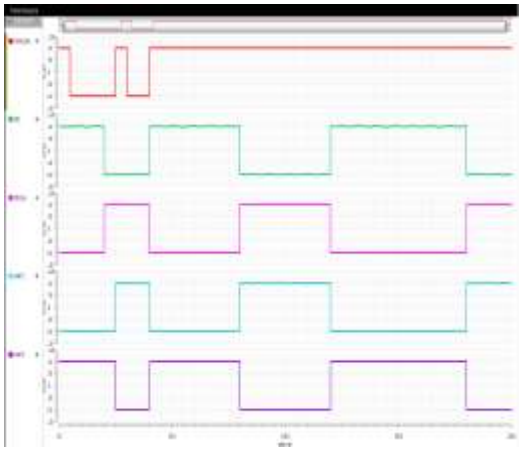

Fig 2. SRAM write operation

To Performing the read operation here sense amplifier is required. The Sense Amplifier Is Main Part of the SRAM Which Is Essential for the Read Operation.

There Are Mainly Three Operations in the SRAM
1. Write Operation
2. Hold Operation
3. Read Operation

During the read operation the bit and bit bar lines are kept at the high voltage. While read operation is going on, then from the one side of the cell is discharge from the pull down transistor .and at the side of the "1" data is stored from that part of the cell there no voltage reduction takes place.
During this process the data which is stored in cell may be flip due to the read operation so that the reason use of the sense amplifier.

The Main Specification of the Sense Amplifier Is as Follow
1. Sensitivity
2. Gain
3. Power Consumption

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The Sense Amplifier Is Divided In Two Part
1. Voltage Sense Amplifier
2. Current Sense Amplifier

The Voltage Sense Amplified Is Mainly Detect the Voltage Variation in the Bit and Bit bar When Ever the Slight Difference I voltage Is Occur Then It Will Provide the Short Path To the 0 Cell And Give The High Voltage to the One Side of the Cell in Which the 1 Data Is Stored. As it shown in Fig 3.Voltage Sense Amplifier Is Not the Fastest Sense Amplifier It Have the Low Speed Compare To The Current Sense Amplifier. The Main Reason Why It Faster Is Capacitance Effect of the Transistor.

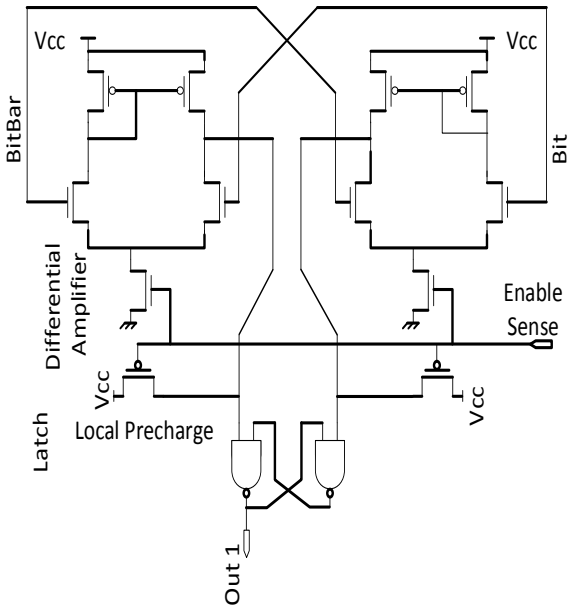

Fig 3. Sense Amplifier

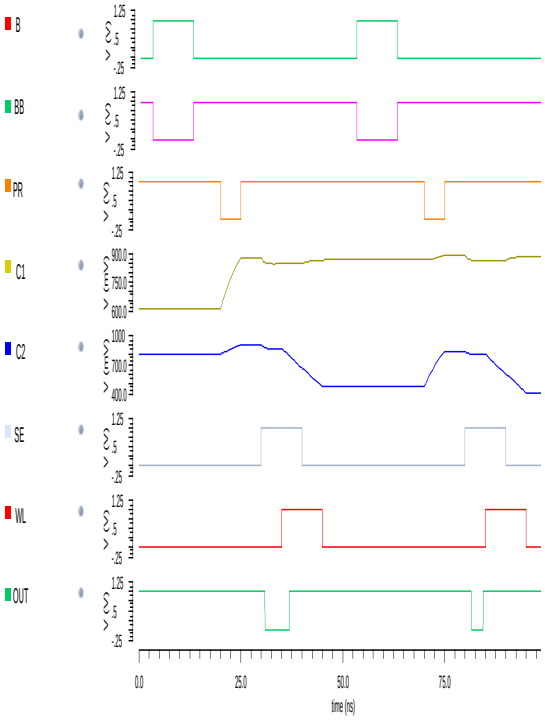

Fig 4. SRAM read operation

The SRAM read operation is shown in the fig.4 for read operation first the bit and bit_bar lines are recharge to "1" after that word line are high and then switch on the sense amplifier, the variation in bit or bit_bar voltage sense by sense amplifier and giv the output. The c1 and c2 are the capacitors which attached to the bit and bit_bar line.

IV. BIST MODULE

A. Test pattern generator

Test pattern generators are extensively used in BIST (built-in self-test) techniques, to test integrated circuits and systems. The BIST architecture basically requires four components namely, Test Pattern Generator (TPG), Circuit under Test (CUT), test controller and Test Response analyzer (TRA). There are Mainly Two techniques to generate Test Patterns: first, is using simple LFSR (linear feedback shift register) (Fig 5.) TPG and second, is using Cellular Automata (Fig 6.) LFSR.[2]

For test the circuit it required random test pattern generator. It is using in BIST (built-in self-test) techniques for testing the circuits. Here random pattern is required so create random pattern from counter, LFSR (linear feedback shift register) but due to some problems like power consumption is more for counter so here counter is avoided. The solution is cellular test pattern generator. An advantage of CA is the power consumption would be decreased correspondingly. [2]

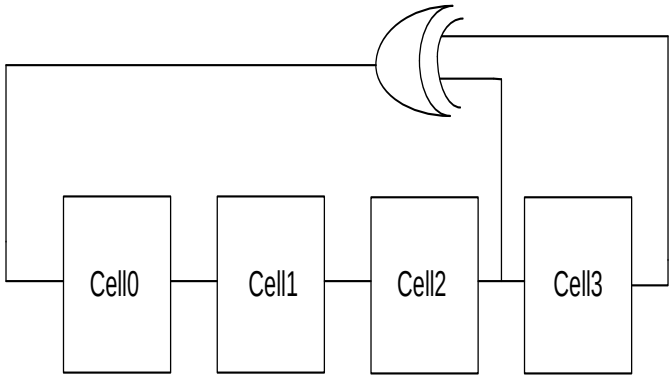

Fig 5Test Pattern generator

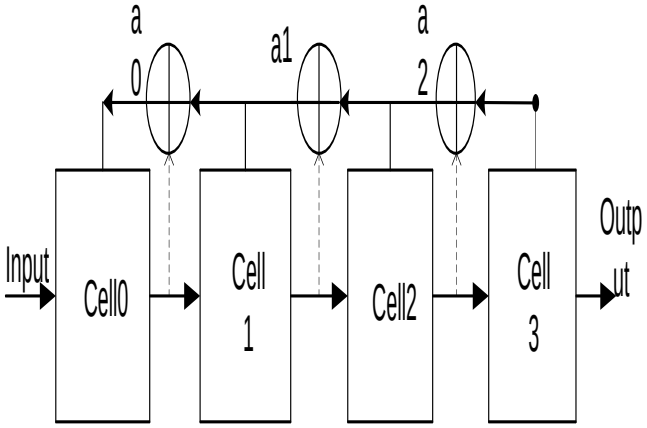

Fig 6. Cellular Automata

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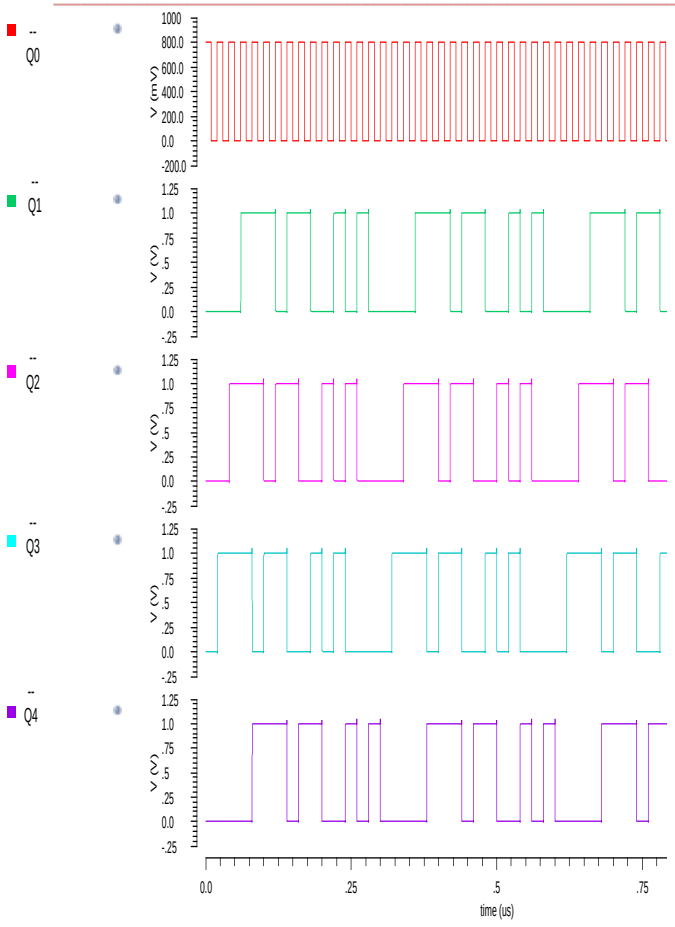

Fig 7. Simulation Result of Test Pattern Generator

The output waveform of test pattern generator are given in the fig. 7 it is 4 bit test pattern generator, after the 11 cycle the pattern are repeat in the top clock is showing after that output of the each flip flop is showing[7]

B. Fault Free SRAM cell

BIST Architecture in these module need fault free SRAM cell first of all what is fault free SRAM cell it defined as when the read and write operation performed it got the perfect output. (Fig 2. & Fig 4.) It means no fault available in SRAM memory. In this paper above mention different types of fault if SRAM cell may be give some not measured value then it shows that the fault should be there in SRAM cell but if it cannot find one of above fault which mention then it's a fault free SRAM cell. [8]

C. Faulty SRAM cell

In Faulty SRAM cell to detect the fault first forced the fault value either because of manufacture or device level fabrication some will be produce. For verification and testing purpose input is given as forcefully fault to the input memory cell and check for the possible number of input, output is correct or not. [7]

D. Comparator

Comparator is comparing the faulty and fault free cell output and give the comparison output. It can detect the fault is present or not, the result is shows in output response Fig 9.

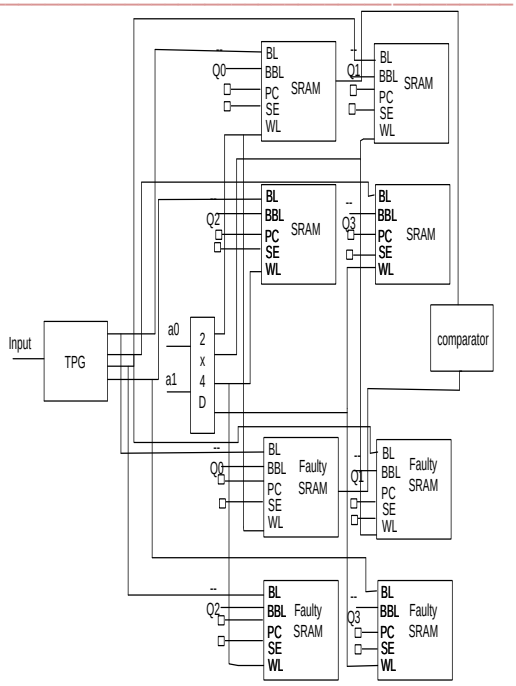

Fig 8. BIST Architecture

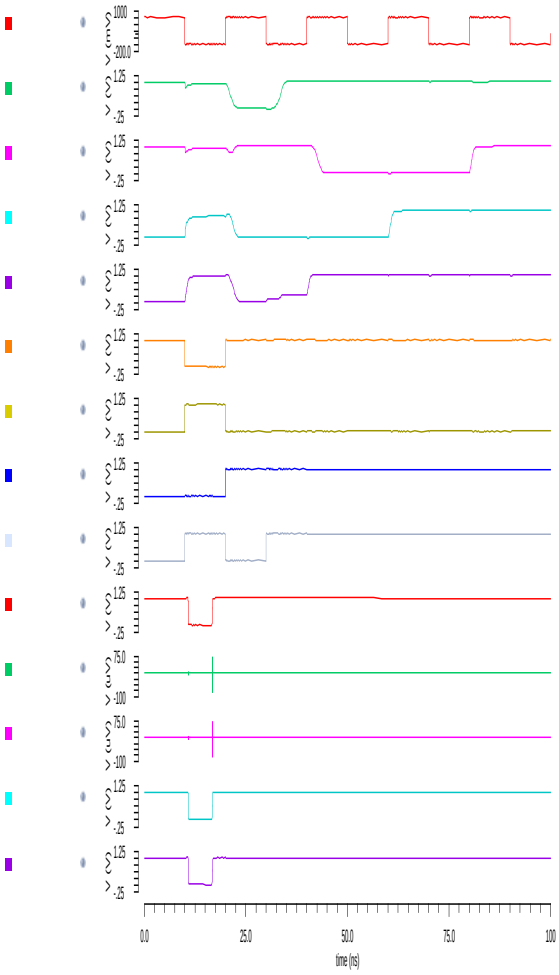

Fig 9 BIST output waveform

The BIST module is given and the corresponding output wave form is given in the fig. 9 first the TPG is generate the pattern

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which is act as the input for the SRAM cell, the write operation is previously described, after the write operation the read operation is perform the output of the corresponding SRAM faulty and good SRAM cell are feed into the comparator circuit the comparator circuit is detect the difference between the both SRAM cells if the any mismatch is available then it gives the output as "1". The output of the comparator circuit is now feed to the repair circuit which is repair the CUT circuit [9]

V. BISR MODULE

VI. REPAIR OF THE MEMORY

There are many process from which the yield of the memory can be improve, repair is a best technique. In the repair of the any memory the data of the cut (circuit under test) is transfer to the repair cell. [4] The main part of the repair is 3 1. Test 2. Analysis of the cell

3. Repair the Cell

Repair Flow

- Test
- Error Logging
- Bitmap
- Redundancy Analysis
- Laser Repair
- Test

To improve the yield of the memory BISR is good technique in the BISR the BIST is the main part of the BISR in the BIST the testing of the CUT is done. [9][8]

There are two memory circuit is present one is CUT and other one is the reference circuit, the reference circuit is the good cell means there are in this cell no Fault is present. By compare the output of faulty cell and the fault free cell the fault is detected by comparator circuit. As the proposed circuit there are two blocks are given of the good cell and faulty cell, and the third one is the spare cells, whenever the fault is occurring then the data of the faulty cell is transferred to the spare cells. Means the cells ha repaired. [5][7]

In the First decoder select the SRAM cell from which it will the reference and the CUT cell is selected. In the next operation cycle the read operation is done in this operation the output of both the cells are feed to the ORA circuit in which is the comparator is present and if there is fault is present then the output of the ORA circuit is high. The output of the ORA is connected to the latch circuit. [8]

The basic principal of the latch is the output of the latch is always low until the input is not high. Latches have three inputs clock, enable and the input. The output of the latch is control by the enable signal if this is low then the latch is not detecting the any of the input [4] So that in the initial cycles in which the enable signal is given as low so the output of the latch is low. In the next cycles the enable pin is high, then after than only the input is selected by the latch. [2]

When the read operation is performed the ORA output is goes to high value. So from that as from the. To improve the yield of the memory, BISR is good technique in the BISR the BIST is the main part of the BISR in the BIST the testing of the cut is done. There are two memory circuit is present one is cut and other one is the reference circuit, the reference circuit is the good cell means there are in this cell no Fault is present.[3] By compare the output of faulty cell and the fault free cell the fault is detected by comparator circuit. Now as the output of the ORA circuit is high so that the latch saves the high value. [9]

The output of the latch is feed to the control signal of the demux so when the low control signal is selected the i0 signal output so reference and the cut cells are selected.[3] Now if the error is occurring Then the ORA output is stored in the latch and the output of the latch is feed in to the demux. From now when ever the decoder is select that faulty cell to the demux the output is routed to the spire cell.[5][7]

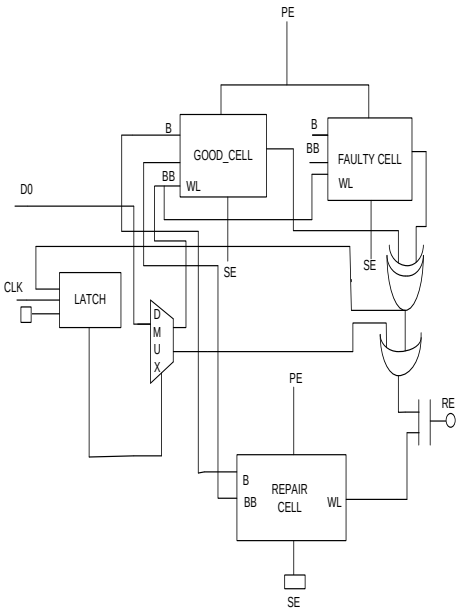

Fig 10 .BISR for single cell

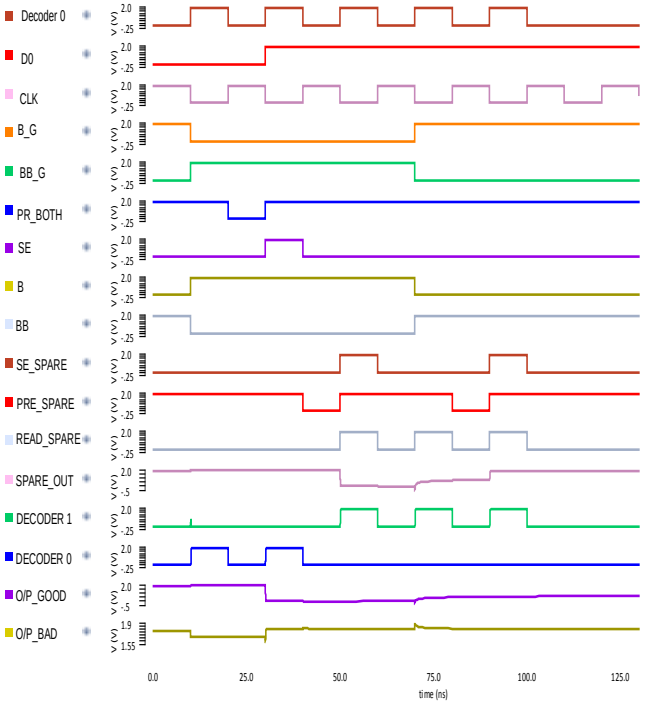

Fig 11. Output response of BISR

This waveform is for individual cell means the TPG circuit is added in this wave form, the output waveform of the BISR circuit is depict in fig. 11 in the decoder0 is connected from the Latch, D0 is for selecting the SRAM cell. In the first write operation is perform in which d0 is high, the d0 is feed into the MUX, it's output is depend upon the latch's output first latch output is 0 because in initial cycles it have to be force to 0 so the MUX give output in first port which is divert the data to the CUT and the reference SRAM cells, after that the read operation is done in which the again the on the D0 along with SENSE amplifier, the output of the read operation is feed to the comparator circuit which is find the fault in the CUT circuit and gives the output. If the fault is present in the CUT SRAM cell then the it activate the latch and the output of the latch is high. Now after this cycle whenever the read or write operation is perform then the MUX is redirect the input to the spare SRAM cell, once the fault is detected the all reda and write operation is done from the spare cell.[8]

A. BISR Model for 3D Memories

3D memories consist of stacked layers of 2D memories as shown in Fig 7. For BISR of 3D Memories, each layer incorporated with BIST architecture and each layer of memory array have spare cell to repair the array in that particular layer. Control circuit of BISR is common block global to all stacked layers. In 3D memory architecture extra decoder is required to select layer, at a time only 1 layer is activated and rest of the layer are isolated by the layer decoder. The output of layer decoder is used to enable the adders' decoder in each in each layer of 2D memory. The BIST circuits local to memory layer identify the fault in that layer and initiate the control signal for selecting the spare cell instead of selecting the faulty cell to repair the memory array in 2D layer. [1]

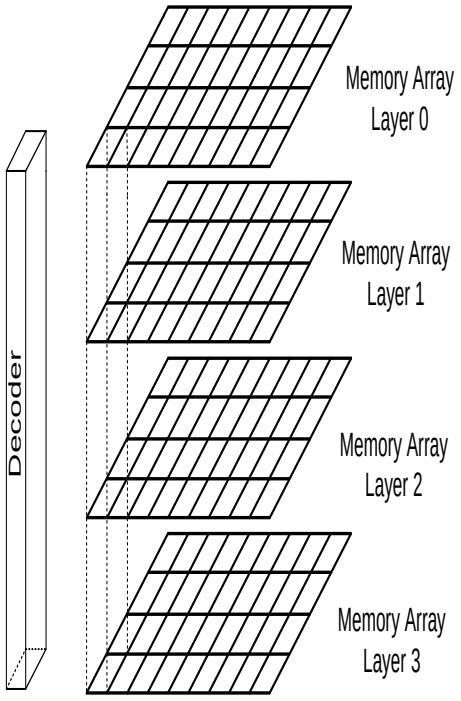

Fig 12. 3D Memories

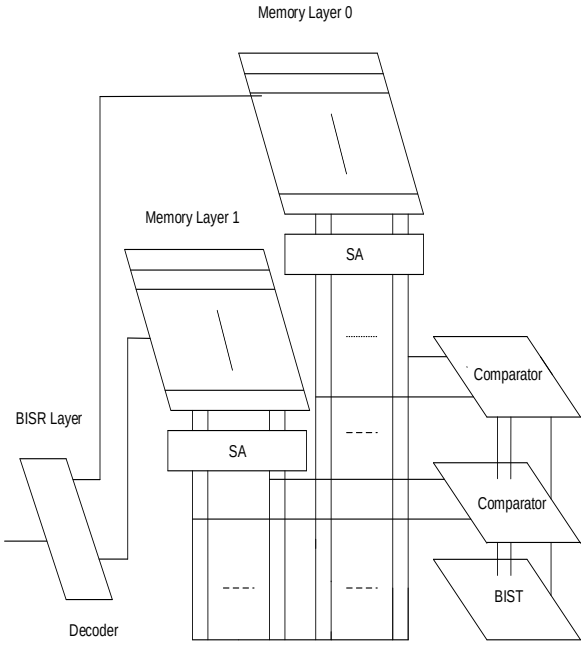

Fig 13.Built in Self-Repair Architecture for 3D Memories

VII. PERFORMANCE ANALYSIS

Performance of the BISR can be analyzed that if low power techniques is used then it reduce the power and delay of the circuit. As show below Table I.

Table I: Calculated Power and delay for Blocks used in BIST Architecture

	Power (w)	Delay (s)
TPG	73.003 nw	12.67µs
SRAM Cell	2.17µw	3.877µs
Faulty SRAM Cell	23.09 µw	8.087µs
BIST	79.007µw	56.787µs

The power and delay comparison shows in the table, 180nm technology is used. Test pattern generator is consumed lowest power in the table because it has less number of transistor. The BIST is combination of all the modules so the power consumption and delay is largest.

VIII. CONCLUSION

In this paper methodology to design BIST and BISR Modules are describing. Here BIST and BISR technique to detect the fault and repair the fault respectively in 3D memories. A low-transition TPG that is based on some explanation about transition counts at the output sequence of LFSRs has been presented. The future TPG is used to generate test pattern for test-the memory cell BISTs in order to reduce the switching activity while scanning test pattern into the scan chain. Furthermore, BISR algorithm for scan-chain ordering has been

presented. The effect of the anticipated design in the fault coverage, test-application time, and hardware area overhead is negligible. Comparisons between the proposed design and other previously published methods show that the Proposed design can be achieve better result for most tested standard circuit.

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