Controlling Method For Anti-Lock Braking System Using Cyclone II

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***Abstract*—** Most of the road accidents occur due to failure of brakes of vehicle. Therefore controlling the speed of vehicle is a basic & wide requirement of human life. Most of the methods of controlling speed are based on controlling braking system of vehicle and maintaining constant speed of both front and both back wheel of the vehicle. The antilock braking systems are designed to control the speed of the vehicle by adjusting difference between the rotations of each wheel. Here we plan to develop FPGA based detection of difference of speed of both wheels of vehicle and according to that controlling the speed of particular wheel. This will be done by Altera Cyclone II FPGA Board (EP2C20F484V7) & requisite hardware circuitry. Basic idea is to achieve reliable, consistent control that will result in improved performance of circuit. Set-up will consist of FPGA controller, hardware board is for operation control, model of vehicle & LCD display.

Keywords- *Antilock braking system (ABS), Brake system, FPGA, Speed Sensors.*

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I. INTRODUCTION

An anti-lock braking system (ABS) is a safety system that allows the wheels of a motor vehicle to continue interacting tractively with the road surface as directed by driver steering inputs while braking, preventing the wheels from locking up (that is, ceasing rotation) and therefore avoiding skidding. An ABS generally offers improved vehicle control and decreases stopping distances on dry and slippery surfaces for many drivers; however, on loose surfaces like gravel or snow-covered pavement, an ABS can significantly increase braking distance, although still improving vehicle control [2].

It does this by monitoring the wheel speed of sensed wheels and predicts when lock-up is imminent. The brake air pressure to the controlled wheels is then either held or released in a controlled way to allow the sensed wheel to turn at optimum wheel slip speed (< 10% slip). Additionally the ABS may disable the auxiliary brake system (retarder).

There are three elements to a typical ABS system:

- The Electronic Control Module (ECM), which monitors the wheel speed signals, computes the slip-performance on the sensed wheels and operates the modulator valves.
- The Wheel Sensors produce a signal with a frequency proportional to wheel speed
- The modulator valve that is controlled by the ECM to either block the brake air line to the brake chambers (thereby holding the brake pressure) or exhaust the brake line to the chambers (thereby reducing brake effort)

The objectives of braking systems are threefold:

1. To reduce stopping distances
2. To improve stability
3. To improve steerability during braking

These are explained below:

1. Stopping Distance:

The stopping distance is a function of the mass of the vehicle, velocity, and force. By increasing the braking force the stop distance will be reduce if velocity and mass remain constant. For all types of surfaces, there exists an increase in fiction coefficient which follows that by keeping all of the wheels of a vehicle near the maximum value, an ABS system can attain maximum force and, therefore, stopping distance will get reduce. This objective of antilock systems however, is tempered by the need for vehicle stability and steerability.

2. Stability:

As the maximum vehicles contain a reliable braking system, it is not necessary that force should be maximum. Maximum force will increase the problem of instability with different wheels of the vehicles. Maximizing force on the wheels will make the system unstable. If a braking system can result a rotational speed of both the real wheels should be same, so the friction coefficient will get increase and lateral force will get increase. This gives us a great stability and is an objective of braking systems.

3. Steerability:

Frictional force is required to get lateral forces and then we called it as we get great steerability. Good peak frictional force control is necessary in order to achieve satisfactory lateral forces and, therefore, satisfactory steerability. Steerability while braking is important not only for minor course corrections but also for the possibility of steering around an obstacle.

DSP processors and controllers are used for digital applications. But DSPs and controllers can not use for latest generation of applications that require not just higher performance too more elastic without increasing cost and resources. Further processors, controllers and DSPs are sequential machines that mean tasks are executed in sequence which takes longer process time to complete the same task. Processors and microprocessors are frequently used in such applications. Using universal processors or signal processors enables obtaining high computational efficiency but significantly increases the drive application cost. The processors designed for electric or electronic drive applications have relatively low computational power. Furthermore, the sets of interfaces offered by such processors in some application have to be replaced by specialized ones [1].

On the other way, the ASIC chips can be applied. Such an advance enables developing specially made digital interface as well as digital data processing system and even integration of integrated system [1].

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II. MODELLING

A. *Software Design*

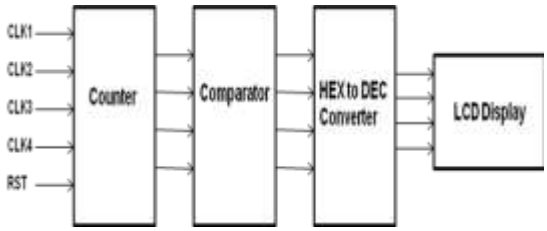

Figure 1 Software Design

Counter

In digital logic designing, a counter can store the number of bits for the various times or a any special event or process that has to be occurred, with respect to a clock signal. Figure 2 shows typical design for counter. Counters are sequential circuits that go through different states. They can be design using one or more number of flip-flops. The FF in the LSB of the bits structure is inverted with every clock pulse or with every cycle pulse. A flip flop in other position is inverted when all the bits in the LSB positions are 1. Synchronous counter have a same structure and can be designed with inverting flip flops and logic gates.

Comparator

It is a hardware design that gets the two different binary numbers and compares them. That's why it is called as comparator. Comparators are used any electronics devices as well controller design circuits.

Comparator also checks for different inputs and gives output as different of that input. Figure shows 4 bit comparator. It compares A with B. It shows the output as A=B or A>B or A<B. One of the examples is an XNOR gate, which is a design of basic digital comparator.

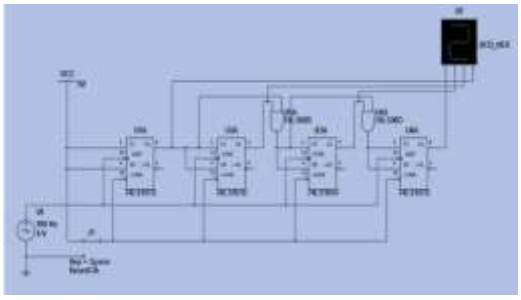

Figure 2 Counter Design

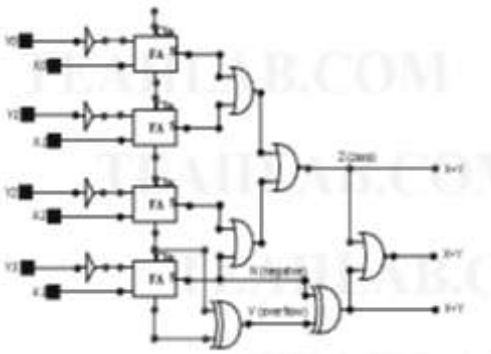

Figure 3 4-Bit Comparator

B. *Hardware Design*

Sensors

Here sensor detects the speed of a wheel by analyzing IR signal. A pair of IR LEDs can be used as motion detectors. The first IR LED is wired to emit LED and the second LED is wired to transmit a signal when it receives an IR input. When small hole on the wheel is not in front of emitted IR, wheel reflects the IR back to receiving LED and it produce the signal. When small hole on wheel is in front of emitted IR, receiving LED does not produce any signal. These two conditions produce a signal with digital value 1 and 0. This variation will be counted by Counter.

PWM System

Pulse width modulation (PWM) is a system for controlling analog circuits with a processor's outputs which is in the digital form. PWM is working in a broad range of applications, ranging from measurement and digital communications to device control application. PWM also work on the principle of time division.

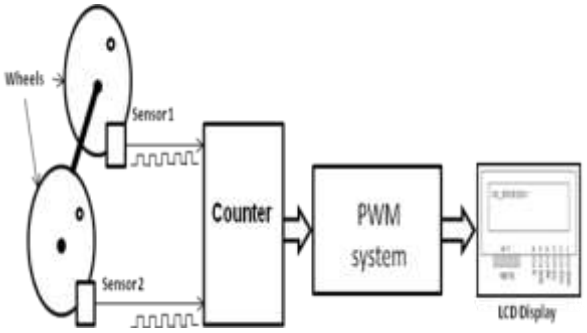

Figure 4 Hardware Design

Analogue Control circuits

Analogue circuits are used for controlling of voltages and currents directly, just like the volume in the radio. In a simple analogue radio, variable resistor is used to control the the volume of the radio. Resistance of the resistor is going to be increase or decrease with respect to the knob of the radio. This type of resistor is called as variable resistor or potentiometer. As the current flowing through the resistor increases or decreases, sound will get controlled. An analogue circuit is one, like the sound system whose output is inversely proportional with resistance of the resistor.

An analogue signal has a constantly changeable value, with unlimited range in both time and amplitude. For example, a nine volt battery is not having the complete 9v capacity. Its capacity will be less than 9V. Analogue signals are different from digital value because system always takes the value for finite set of values which are predefined.

Digital control Circuits.

By calculating analogue circuits digitally, system costs and power consumption can be severely decreases. PWM is a method for encoding analog signal into digital with respect to given levels. During the use of counters, the duty cycle of a square wave is modulated to convert a specific analogue signal into digital signal. The PWM signal is at rest digital because, at any given time, the full supply is either fully on or fully off. The voltage or current source is complete to the analogue load by means of a repeat chain of on and off pulses. The on-time is the time during which the DC supply is on and applied to the

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load, and the off-time is the periods during which that supply is off.

The main benefit of PWM is that loss of power devices is very less as compare to other devices.. When a switch is off means there is virtually no current, and when it is on, there is about no voltage drop transversely to the switch. Loss of Power, being the multiplication of current and voltages, it is nearly zero in the both the cases.

III. EXPERIMENTAL RESULTS AND DISCUSSION

RTL Design

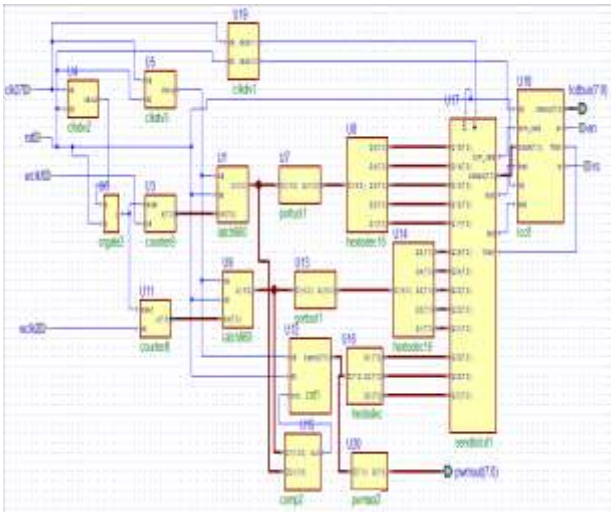

Figure 5 RTL Design

RTL design shows complete representation of VHDL code. Wclk1 and wclk2 are the two inputs from two wheels of the vehicle. These inputs are given to counter8 which counts the number of rotation in 1 sec. Simultaneously this count will be added in the latch860 and the complete result after 60sec will shows the count which is nothing but a speed of wheel in rpm(revolution per minute). This count is converted into decimal (ASCII in case of LCD) format and provide to LCD display.

Output of Counter8

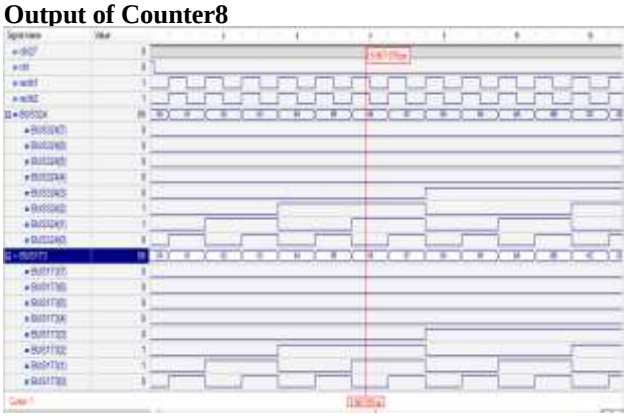

Figure 6 Output of Counter8

Output of counter result a count start from 0 and increases until the time delay of 1 second is over. As the time period is over, counter will get reset by clock. All the values of counter will be shown in hexadecimal format.

Input and Output of HEXTODEC16

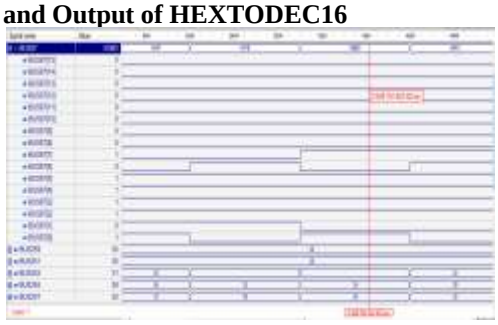

Figure 7 Input and Output of HEXTODEC16

Hex to decimal converter will convert the value in hex format into decimal format. But in this case it will be converted into the ASCII format. If the input of HEXTODEC is 00BD, then output will be 00190 in decimal format. But in ASCII format each digit in output will be separated and 3 will be added at the MSB side. Therefore above example will be display as 30, 30, 31, 39 and 30 on different pin. In the above waveform, BUS87 is input of HEXTODEC and BUS259, 251, 253, 255, 257 are the outputs.

Output of pwmsol2

Figure 8 Output of pwmsol2

Output of pwmsol2 will be given to the controller of motor. For the different wclk input of first motor, it gives the output to control the other motor. BUS270 is the input pin for motors.

FSM for LCD

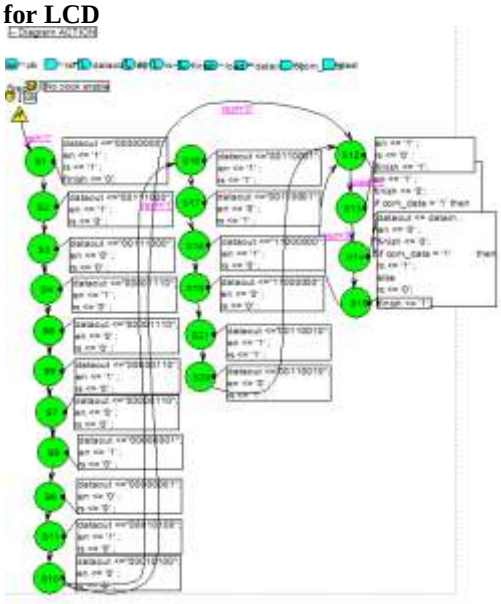

Figure 9 FSM for LCD

FSM of LCD consists of different states. S1 to S10 and S16 to S20 states are used for the initialization of display. Every two states having same count for 'dataout' and having a difference of 'en' pin. This initialization is done by using a standard LCD table.

IV. CONCLUSION

In this paper, the antilock braking system prevents wheels locking or skidding, no matter how hard brakes are applied, or how slippery the road surface. Steering stays under control and stopping distances are generally reduced. Integrated antilock brake systems combine motors to run the wheels, PWM network, IR sensor circuit and LCD display to display speed of motor. Non-integrated ABS consists of programming VHDL code for controlling of wheels speed. PWM network generate a voltage of required value to control the vehicle speed. This speed will be display on the LCD display for verification purpose. PWM system gets the different two inputs from two signals. Counter will count the number of cycles in that input and give the count. These two counts compare by the comparator. If these two counts are different then only ABS work, otherwise ABS will not work. The objective function is defined to maintain the wheel slip to a desired level so that maximum wheel traction force and maximum vehicle deceleration are obtained. In order to obtain the optimum value in a shorter time and in a much wider region, the error-based optimization approach is used. The method shows a much faster response in comparison with the genetic algorithm alone. The performance of the proposed controller is tested on the vehicle model considering the effect of dynamic load transfer from the rear to the front wheel, with the hydraulic brake system, for different road conditions. Simulation results show very good performance of the controller for different road conditions.

REFERENCES

[1] Ravindra P. Dhewale and Prof. P. B. Borole, " Designing Of Controller for Anti-Lock Braking System Using FPGA", International Journal of Engineering Research and Applications (IJERA) , Vol. 3, Issue 2, pp.693-695, March -April 2013.

[2] Chih-Min Lin and Chun-Fei Hsu, "Neural-network hybrid control for antilock braking systems", IEEE Transactions on Neural Networks, Vol.14, pp. 351 – 359, Mar 2003.

[3] Houhua Jing, "A Switched Control Strategy for Antilock Braking System With On/Off Valves", IEEE Transactions on Vehicular Technology, Vol.60, pp. 1470 – 1484, May 2011.

[4] Ngoc Quy Le and Jae Wook Jeon, "An Open-loop Stepper Motor Driver Based on FPGA", International Conference on Control, Automation and Systems 2007, Oct. 17-20, 2007.

[5] Ms. Shilpa Kale and Mr. S. S. Shriramwar, "FPGA-based Controller for a Mobile Robot", International Journal of Computer Science and Information Security, Vol. 3, No. 1, 2009.

[6] K. Ramasamy and A. Srinivasan, "Design and Implementation of a Complete Car Automation using FPGA", European Journal of Scientific Research, Vol.62 No.3 , pp. 448-452, 2011.

[7] Lennon W.K.., "Intelligent control for brake systems", IEEE Transactions on Control Systems Technology, Vol.7, pp. 188-202, Mar 1999.

[8] Cuidong Xu, Cheng, K.W.E., Lin Sha, Ting. W., Kai Ding, "Simulation of the integrated controller of the anti-lock braking system", 3rd International Conference on Power Electronics Systems and Applications, PESA , pp.1-3, 2009.

[9] Patra, Nilanjan; Datta, Kalyankumar, "Sliding mode controller for wheel-slip control of anti-lock braking system", IEEE International Conference on Advanced Communication Control and Computing Technologies (ICACCCT), pp.385-391, Aug 2012.

[10] Ahmad Mirzaei, Mehdi Moallem, "Design of an Optimal Fuzzy Controller for Antilock Braking Systems", IEEE Transactions On Vehicular Technology, Vol. 55, No. 6, pp.1725-1730, November 2006.