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An Implementation of PWM in FPGA for the Speed Control of DC Drives

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***Abstract*—** This paper suggest, a PWM base new method of controlling speed of DC drives using Field Programmable Gate Array (FPGA). A FPGA base Algorithm is used to generate the firing pulses required to for full wave phase control rectifier. Pulses are synchronized with main AC supply the delay of pulses determines the firing angle of driver circuit and hence the speed of rotation. The suggested control scheme has been implemented using XILINX FPGA SPARTAN 2 XC2S200 and tested using Thyristor driver circuit for direct current (DC) motor. Experimental results show that the speed of the DC motor can be controlled effectively.

Keywords- *Direct Current (DC), Field Programmable Gate Array (FPGA).*

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I. INTRODUCTION

The DC motors have been extensively used in the manufacturing fields and various approaches have been made to realize high performance speed control. DC motor is an device in which the electrical input determines the speed of the armature of a motor. The shaft of the DC motor can be keep to a specific speed by sending the control signal. These can be effectively utilized in many speed control systems subjected to external disturbances.

With successively improving reliability and performance of digital controllers, the digital control techniques have predominated over other analog counter parts. The advantages of digital controllers are:

- Easy to upgrade
- Less power loss
- Reduce sensitive to temperature variation
- Less components
- Improved efficiency
- Economical

The present methods which are reported till now are generally base on 8 bit Microprocessor. The control scheme have the advantages of flexibility, higher reliability and lower cost, but the challenging control requirements of modern power conditioning systems will overload most general purpose microprocessors and the operational speed of microprocessor limits the use of microprocessor in complex algorithms.

Microcontrollers and Digital Signal Processors are used for digital control applications but DSPs and Microcontrollers cannot further be equal with the new generation of applications that require not only higher performance but also more flexible without increasing cost and resources. The efficient control of the motor drive systems involves fast computational units. Signal processors and microprocessors are frequently used in such applications. Using universal microprocessors or signal processors enables obtaining high computational efficiency but significantly increases the costs of a drive application. Further microprocessors, Microcontrollers and DSPs are sequential machines that mean tasks are executed sequentially which takes longer processing time to accomplish the same task. The 16 and 32 bit processors designed for electric drive applications have relatively low computational power. Furthermore, the sets of interfaces offered by such processors in some application have to be replaced by specialized ones. Alternatively the ASIC (Application Specific Integrated Circuit) chips can be applied. Such an approach enables developing custom built digital interface as well as digital data processing blocks and sometimes even integration of ADC converters into one integrated circuit. Developing an ASIC chip is however expensive and laborious, therefore on the design stage of algorithm and interface development, FPGA based solution can be used.

The high speed hard wired logic can enhance the computation capability. The ASIC based technology provides a quick and economical solution for particular applications with huge market. Owing to the progress of technology, the life cycle of most modern electronic products become less than their design cycle. The appearance of FPGA has drawn much attention due to its shorter design time, reasonably priced and higher density [1]. The simplicity and programmability of FPGA make it the most favorable choice for prototype digital systems [2].

Different methods are used to control the speed of DC motor. The Kalman filter is used to estimate the instantaneous speed and position with low precision [3]. Disturbance suppresser is used in robust position control scheme for DC motors [4]. In Wrap digital position control around analog servos [5], the Microcontroller is used to control speed and to send the motion commands to the analog motor controllers. The Neural networks and Fuzzy logic control systems are also used to control the position of DC motors.

In this paper a new method of controlling speed of DC motor using FPGA is proposed.

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II. FPGA BASED CONTROL SCHEME

Fig. 1 shows the proposed block diagram of the system. It mainly consists of keyboard, ZCD, FPGA Controller, Driver and Motor.

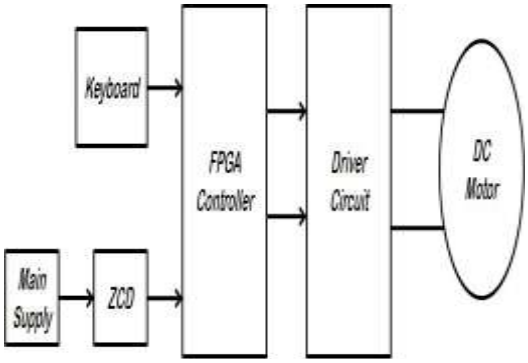

Figure 1. Proposed block diagram of FPGA base speed control of dc drives

A. Keyboard

The required angle is divided by 12 (i.e. 180/15) to get equivalent number; this number is entered as input through keyboard. It accepts Hex number as input. The keyboard consist of 4 Switches combination of this form 16 keys from 0,1,2,3,4,5,6,7,8,9 and hex value A, B, C, D, E and F. When a key is pressed then the corresponding output delay is generated.

B. Zero Crossing Detector (ZCD)

To have full control over the firing angle of the SCR/triac (from 0 to π radians), it is necessary to precisely detect the zero crossing of the sinusoidal input. Conventional zero crossing detectors cannot distinguish between start of positive half cycle or negative half cycles. Schematic of the zero crossing circuit that was implemented is shown in Figure 2

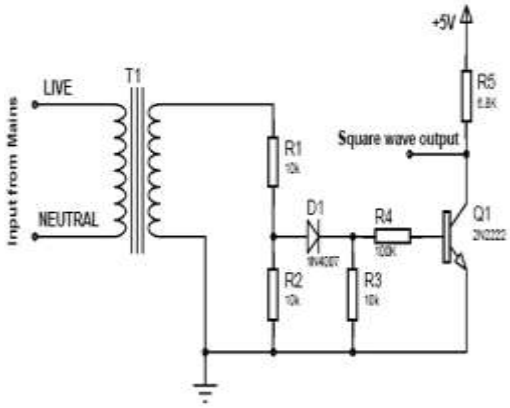

Figure 2. Zero Crossing Detector

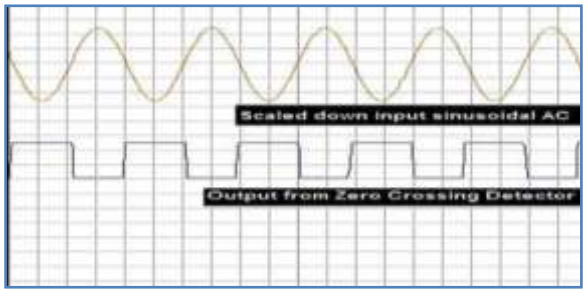

Figure 3. The result of zero crossing detector

C. FPGA Controller

FPGA Controller accepts input from the keyboard and ZCD. All the block of FPGA controller activated with the rising edge of ZCD input. Depend on the keyboard switches combination the controller unit in FPGA calculates the require delay. After the delay the high frequency square wave pulses are send to the driver circuit for firing the thyristor bridge circuit. The amount of delay directly decides the speed of DC motor.

The FPGA controller is design by using the counter and latch. The coding is performing in VHDL. The flowchart is shown in Figure 4

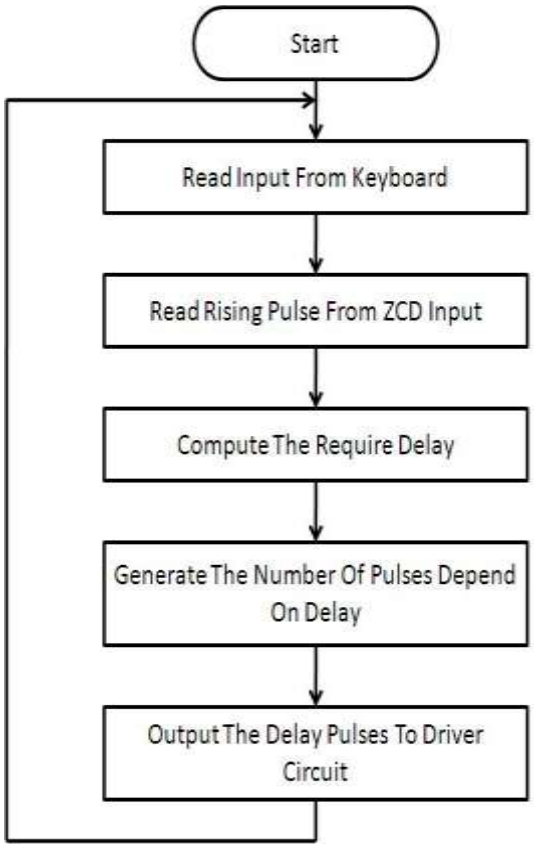

Figure 4. Flowchart

D. Driver Circuit

The output current of FPGA kit is very small that's why we require driver circuit. The driver circuit gives the required current to drive the motor. Generally, it is the bridge circuit made up of two thyrister and two power diodes. Input to the driver circuit is AC supply of 50Hz frequency and two input from FPGA controller to control the positive and negative cycle output power.

The output of FPGA controller determines the firing angle of bridge circuit. As the firing angle changes, output power of driver circuit differs. Hence finally speed of DC motor changes.

The motor can be configured for either velocity control or position control. The motor takes 15 pulses to rotate 360 degrees. For a rotation of 12 degree 1 pulse is required.

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Maximum speed is achieved when the delay is zero and minimum speed is achieved when the delay is highest.

III. RESULTS AND CONCLUSION

The simulation is done using XILINX 8.2 ISE software and FPGA SPARTAN 2XC2S200 Board is use to dump the program code.

The motor reaches the required speed in clockwise or anticlockwise direction in very less time. The simulation results for different inputs are shown in Fig. 5 & 6 with their respective delay time. In this design there is no problem of noise and electromagnetic interference over the mains power line as it is fully isolated from main supply line at both the input and output stages.

The design is an easy to realize, user friendly and cost-effective. The method is fully software upgradable which make it more suitable to drive more devices. Components used to implement this proposed design are also simple and all time available. As the input is in digital format speed can be precisely control and accurately predicted.

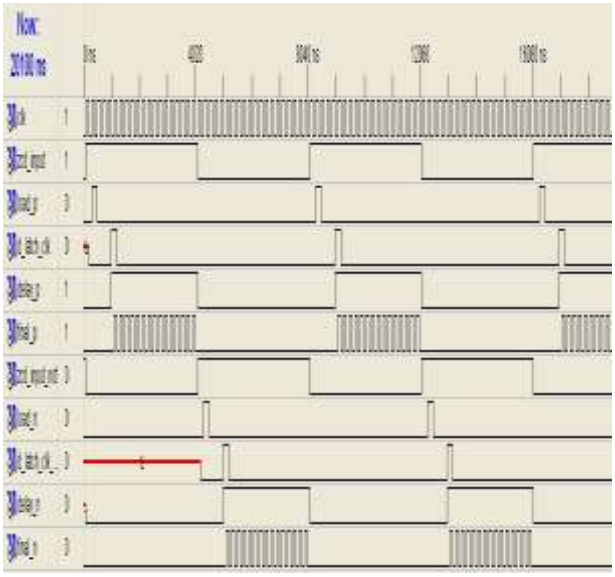

Figure 5. Results for minimum delay input

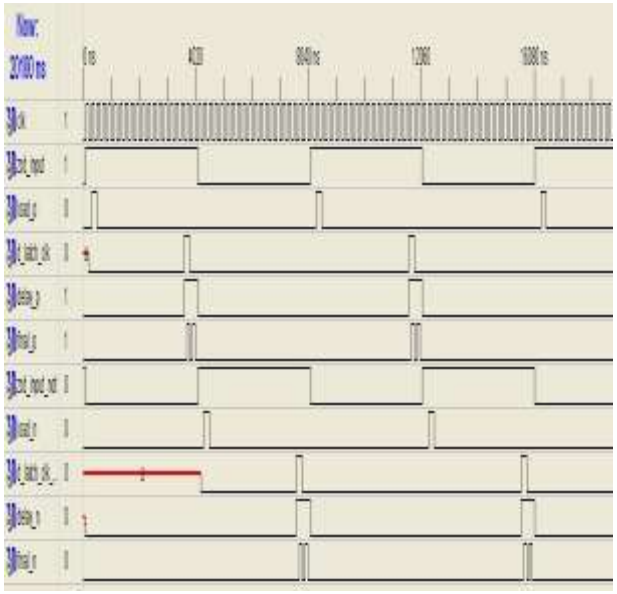

Figure 6. Results for maximum delay input

TABLE I. READING FOR TRIGGER PULSE FORM FPGA

Sr. No.	Input Data	Delay(ms)	No. Of Output Pulses
1.	0000	0.0000	13
2.	0001	0.6666	12
3.	0010	1.3333	11
4.	0011	1.9998	10
5.	0100	2.6664	9
6.	0101	3.3333	8
7.	0110	4.0000	7
8.	0111	4.6666	6
9.	1000	5.3333	5
10.	1001	6.0000	4
11.	1010	6.6666	3
12.	1011	7.3333	2
13.	1100	8.0000	1
14.	1101	8.6666	Zero
15.	1110	9.3333	Zero
16.	1111	10.0000	Zero

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