Classification of Power Quality Events In Power System Using ANN (Nueral Network)

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Abstract**—**Classification of power quality events (PQE) related voltage and current waveform fluctuations is a key task for power system performance. PQE classification method is based on the optimized time-frequency representation (OTFR) .Classification algorithm has been successfully tested and verified with many available power quality events that includes five classes. Algorithm is implemented on DSP based hardware system. The computing efficiency of this algorithm has been verified with the outputs.

Keywords*-Power Quality Events, Classification-OTFR, Neural Networks, DSP etc.*

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I. INTRODUCTION

The PQE classification approach is processed by two sequential processes: feature extraction and classification. The process of the feature exaction is to highlight a PQE waveform onto a low- dimension time-frequency representation (TFR), which is designed for improving the distinction between classes. To improve the classification accuracy, a distinct TFR is designed to break a class or its group from all other classes. Each separation procedure usually produce a binary decision. The classifiers has a Heaviside- function linear classifier and neural network classifiers with feedforward structures[3-4].

Several TFRs for the classification tasks are made by training signals from all classes. The design of TFR is the design of kernel function for shaping the time-frequency ambiguity plane. Parameters of classifiers are trained by the training signals from all classes. PQE waveforms are given to the system and classification performance of system is evaluated. A DSP based hardware system is implemented and real-time monitoring capability of this method is noted. This algorithm has been tested with many power quality events that cover five classes: voltage sags, swell , high-frequency capacitor switching, low- frequency capacitor switching, interruption and normal variations (noise)[2-3].

DSP-based hardware system can do processing a five-cycle (83.3 ms) PQE waveform within 11.2 ms. The real- time computing capability of this method is verified with these result. This paper throws light on building a new generation of high accuracy and high capability real-time PQE monitors by combining proposed methods with DSP technologies[7-8].

II. OPTIMAL TFR DESIGN AND CLASSIFIER TRAINING

A small group of PQE waveform events covering five PQ classes is used for TFR design and classifier training. This group consists of 50 signals from each class[6]. Hence, a total of 250 real world voltage waveforms are used for training purposes. In given algorithm, a process for classifying N signal classes requires N-1 kernels for N-1 TFRs. Since, five classes are under consideration, four different kernels are implemented: harmonics, sag, capacitor switching, and capacitor high-frequency switching kernel. Harmonics kernel is used for separating class harmonics from rest of classes. The sag kernel is for separating class sag from rest of classes. The capacitor switching kernel is for separating the class group from the remaining class[5].

TABLE 1. HARMONICS KERNEL

Location Co-ordinates	score J F1	Whether selected for feature location?
(22, 32)	33.94	Yes
(22, 612)	33.94	No, symmetric with (22, 31)
(622, 612)	33.94	No, symmetric with (22, 32)
(622, 32)	33.9499	No, symmetric with (22, 31)
All other locations	< 33.94	No

TABLE 2. VOLTAGE SAG KERNEL

Location values	Discriminant score, JF2	Whether selected for feature location?
(257, 3)	5.06	Yes
(257, 640)	5.06	No, symmetric with (257,3)
(385, 3)	5.0649	No, symmetric with (257, 3)
(385, 640)	5.06	No, symmetric with (257, 2)
(258, 3)	4.99	Yes
(258, 640)	4.99	No, symmetric with (258, 3)
(384, 2)	4.99	No, symmetric with (258, 3)
(384, 640)	4.9953	No, symmetric with (258, 3)
All other	< 4.9953	No

Table 1 and Table 2 show the process for designing only two kernels. Likewise rest two kernals can be designed. The number of feature points needed for every kernel is found by rigorous classification experiments[9-10]. The number of feature points is found from min to max, starting from 1. The optimal numbers of feature points for every kernel have been searched. Hence, nine feature locations are chosen for these four kernels. In Table 1 and Table 4, the column "*Location*" means the coordinate (n, t) on time-frequency ambiguity plane, where n represents discrete frequency shift(DFS), and t represents discrete timelag(DT) [1]. To design the kernel i, total 640x640 locations on the ambiguity plane are ranked based on their Fisher's discriminant (FD)scores J_{Fi} $(i$=1,2,3,4)[2], whose computation method is governed by equation (8) in [1]. The correlations of locations on the ambiguity plane are taken in the feature selection process. Because moduli of the points on the ambiguity plane are symmetric in nature according to both horizontal and vertical axes of the plane, always a group of four locations has identical Fisher's discriminant score(FDS). One of these four locations is selected as a feature location..

III. WAVEFORM PROCESSING ALGORITHM

As shown in Fig. 3.1, after the kernel design and classifier training are finalised, waveform processing algorithm becomes straight forward.

For a 640-point input, nine feature points are calculated. These nine real values are then serially sent to four different linear and ANN classifiers for making classification decision.

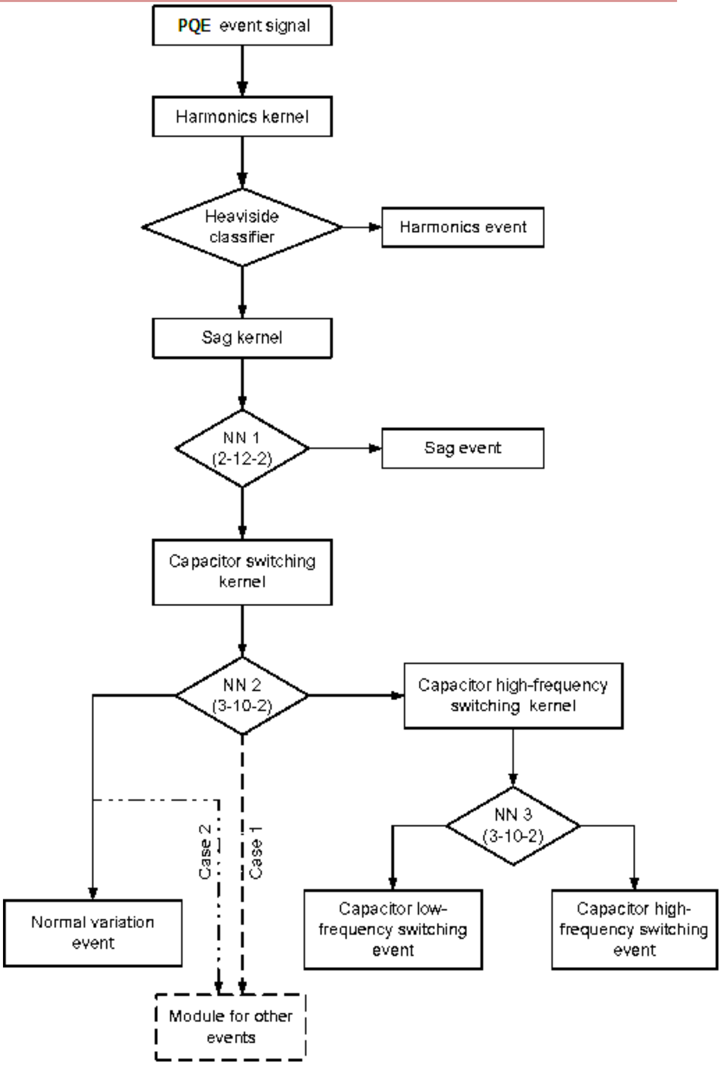

Fig. 3.1 PQE signal classification algorithm.

IV. DSP-BASED REAL-TIME HARDWARE IMPLEMENTATION

To evaluate and verify the real-time computing capability of algorithm, a DSP-based hardware system is implemented with proposed algorithm.

A block diagram for the system is shown in Fig,4.1 The algorithm is implemented with TI TMS320VC5XXX digital signal processor with TI THS1206 12-bit 6 MSPS A/D converter. In deployment mode, signal is passed through a potential transformer and then through ADC. In the testing mode, signal is fed either from a function generator or from a PC station .While response time of the system is observed and measured.

The TMS302VC5XXX is a fixed-point DSP processor having 128 KB of on-chip memory with 160 MHz clock speed, which can perform 160 MIPS. This DSP processor has a 17x17 parallel multiply accumulator unit which permits single cycle multiply accumulate operations.

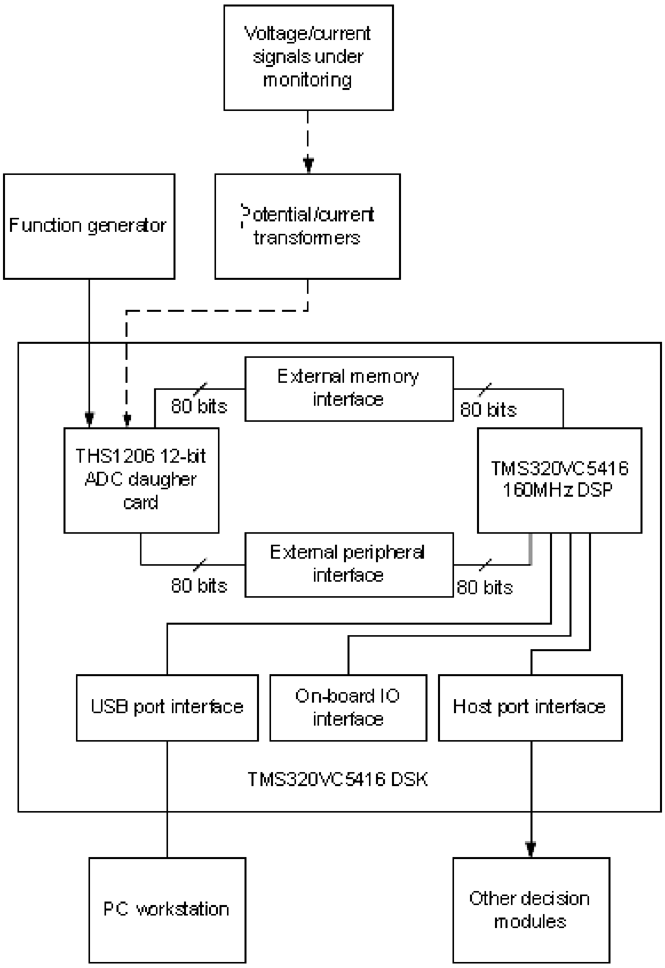

Fig.4.1-Block diagram of the hardware PQE monitoring system.

EXPERIMENTAL RESULTS

The detailed results are shown in table 5.1 and table 5.2 for various discussed PQE classifications.

V. CONCLUSIONS AND FUTURE WORK

Classification of voltage and current fluctuations in power systems is of utmost importance. A new classification algorithm for power quality event disturbances is proposed in this paper.

Classification strategy presented in this paper has limitation that many PQE disturbances can happen simultaneously in a power system. Based on the same feature extraction scheme(FES), a ANN classification approach, which can give more accurate and precise information.

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TABLE 5.1. STEP-BY-STEP RESULTS

Kernels acting	Signals in class			Signals in rest of classes		
	Testing events	Recognized events	Recognition rate	Testing events	Recognized events	Recognition rate
1. Harmonics	203	199	99%	657	656	99%
2. Sags	145	144	99%	516	515	99 %
3. Capacitor switching	176	172	98.0%	317	311	98%
4. Capacitor high-frequency switching	138	135	98%	179	172	96%

TABLE 5.2 RESULTS OF A POWER QUALITY EVENTS CLASSIFICATION EXPERIMENT WITH DIFFERENT PQE DATA

Different Classes	Testing events	Recognized events	Recognition rate
1. Harmonics	203	199	99%
2. Voltage sags	145	144	99%
3. Capacitor low-frequency switching	176	172	98%
4. Capacitor high-frequency switching	138	135	98%
5. Normal voltage variations	198	194	98.0%
Total	860	844	99.0%