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1 V, 45 NM CMOS Novel Successive Approximation ADC With UP DOWN and RING Counter as SAR Logic

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Abstract: In today's advance electronic and communication systems the role of high accuracy Analog to digital converters are of great importance. Nowadays, a larger percentage of mixed-signal applications requires for health care systems. Also the speed of the chosen ADC design matters a lot as we are connected with the real world signals.
SAR based ADC will provides us a better solution for various analog to digital systems. It is an essential device whenever data from the analog world, through sensors or transducers, should be digitally processed or when transmitting data between chips through either long-range wireless links or high-speed transmission between chips on the same printed circuit board.
The paper projects up down and ring counter as a logic for Successive Approximation Register (SAR logic for a ADC that is one of the best suited for low power. Here the resolution is of 4-bit and a power consumption of few milliwatts. SAR ADC is implemented in 45 nm CMOS technology with a power supply of 1V and pin out with 1.8 V.

Specifications: 4-bit ADC resolution, 0.12um technology, 1 LSB error, with control signal like Start of conversion (SOC) and End of conversion (EOC)

Keywords: ADC, Up down Counter, SAR, CMOS 45 nm, Low power, high speed.

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I. INTRODUCTION

In the past few years, more and more applications are built with very stringent requirements on power consumption. For electronic systems, such as wireless systems or critical health care systems, the power consumption is becoming one of the most critical factors. The stringent requirements on the energy consumption increase the need for the development of low voltage and low power circuit techniques and system building blocks.
Analog to Digital Converter (ADC), is an electronic circuit that converts continuous analog signals into discrete values.

An analog signal needs to be quantized in order to be converted in a digital one. An analog signal can take infinite values; quantization consists in the substitution of these infinite values into discrete and finite amounts of values.

There are two ways of formatting the SAR structure. Here we are implementing logical optimization for SAR based design by using two topologies as up down counter and ring counter as SAR logic.
SAR typeanalog-to-digital converters (ADCs) represents a lotof or majority of the ADC market for moderate-to-high-resolution ADCs. SAR ADCs provide up to 5Msps sampling rates with resolutions from 8 to 16 bits. The SAR architecture allows for high-speed, typically low-power ADCs to be packaged in small form factors for today's high demanding applications. With Microwind 3.5, we have designed 4 bit low power SAR ADC with 45 nm technology.

The most common low speed converter is the iterative converter. As shown in figure 1, it consists of a digital-to-analog converter, a counter and an analog comparator. Starting with the middle voltage range, the counter is decreased till the input voltage Vin is greater than DAC voltage Vdac.

II. UP DOWN COUNTER as SAR Logic

The most common low speed converter is the iterative converter. As shown in figure 1, it consists of a digital-to-analog converter, a counter and an analog comparator. Starting with the middle voltage range, the counter is decreased till the input voltage Vin is greater than DAC voltage Vdac.

The Iterative converter algorithm and a simple implementation with up/down counter of a successive approximation ADC is shown in Figure 2.

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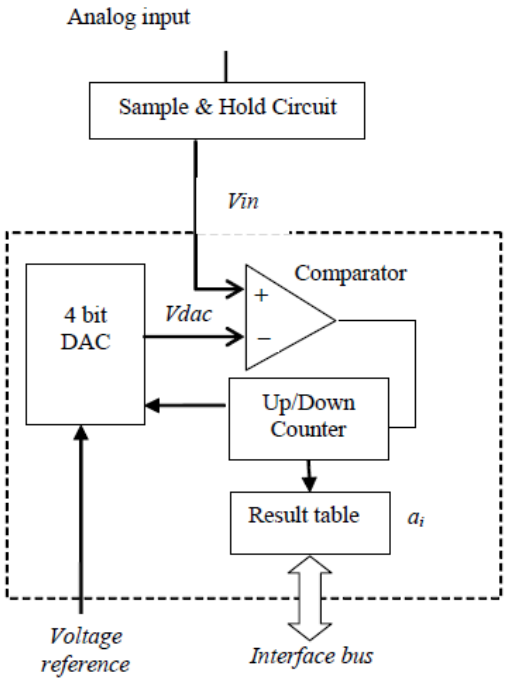

Figure 1: Counter as SAR ADC Block diagram

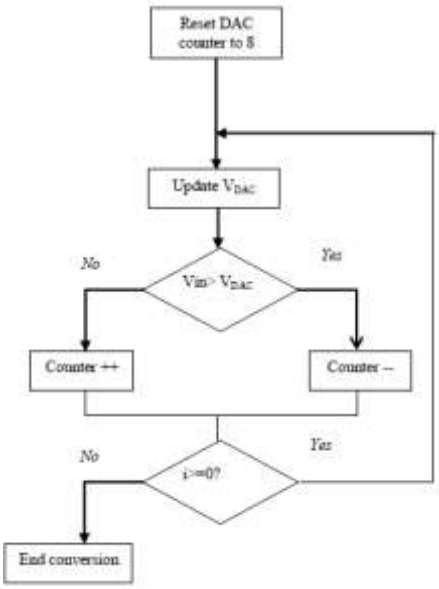

Figure 2: Iterative converter algorithm and a simple implementation with up/down counter

In the particular example shown in the figure, we suppose that Vin is a little higher that Vref/2. The SAR counter would increment, else would decrement to get close to Vin value.

We design the SAR counter logic by simplest method, an Up/Down counter to control DAC o/p.
It works by starting by binary o/p 8(1000), and then by determining whether Vin is larger or smaller than VDD/2, it decrements or increments.
The counter o/p and Vin is compared using comparator which gives the value of that count directly. The comparison is performed for the next count, and so on until all count are checked for below or greater than value 8.
The conversion would start with SOC signal and cycle finishes after 8 clock cycles, with active low EOC output.
This type of converter is called successive approximation converter. The complete process is faster than the iterative converter as only N comparisons are necessary.

Using Microwind EDA tool and DSCH, we have designed SAR components and analysed their simulation results to design SAR architecture for health care systems.

Table 1: Conversion Data Table for our ADC.

Analog Vtg I/P	ADC O/P	Decimal
0.0 V	1111	15
0.1 V	1111	15
0.2 V	1111	15
0.25 V	1101	13
0.32 V	1011	11
0.4 V	0111	7
0.5 V	0111	4
0.6 V	1010	3
0.7 V	0011	2
0.75	0011	1
0.8 V	0001	1
0.87	0001	1
0.9 V	0001	1
1.0 V	0001	1

UP Down counter as SAR logic designing consists of two major building blocks as

1. Up Down Counter
2. Output Register

The counter increments or decrements on the comparator input, it would start only with a pulse signal as Start of Conversion (SOC), lasting atleast one clock cycle.
If the Comparator is ‘0’, then the O/P would be 15 (1111), and if the comparator is ‘1’ all the time then the o/p would be 1 (0001).

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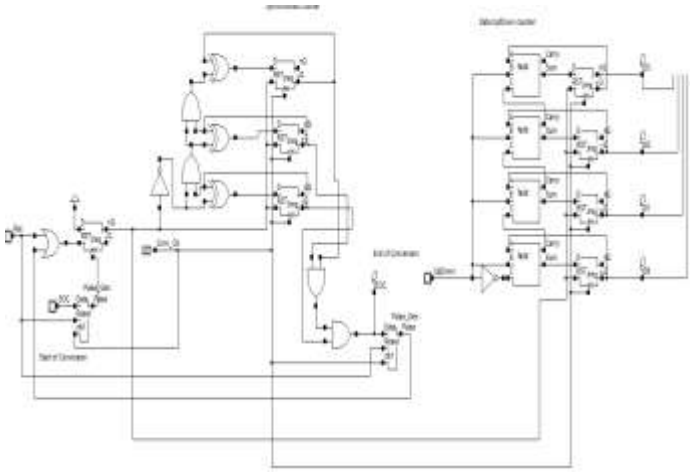

Figure 3: Up-Down Counter schematic

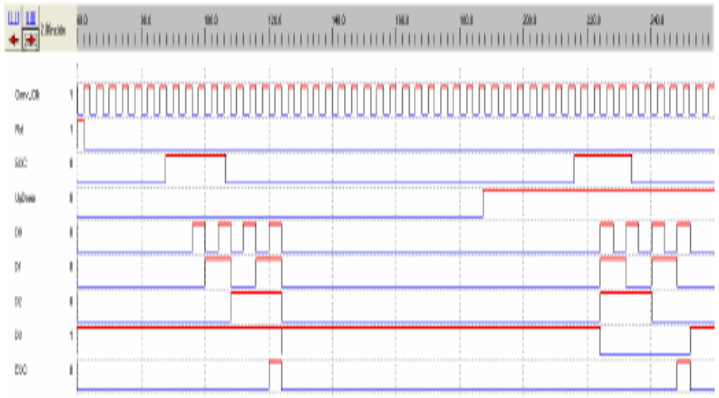

Figure 4: Up-Down Counter schematic simulation

We can observe that counter ends at higher counts ifUpDown signal is logic '0', else the counter would endat lower count value.

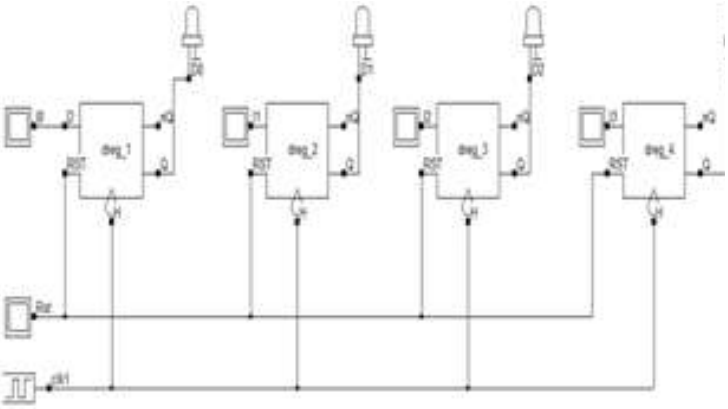

Figure 5: Output RegisterPhysical Design

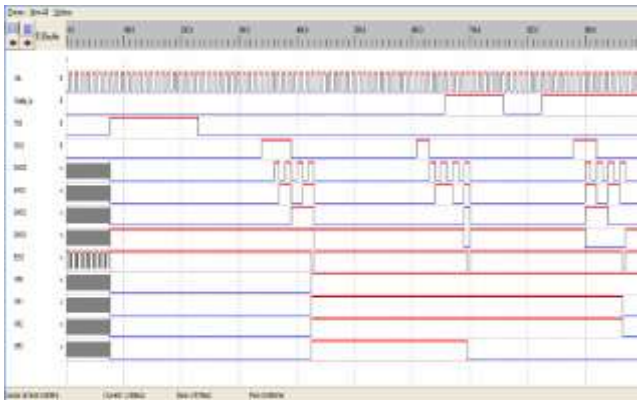

Figure 6: CMOS Layout of SAR AD

III. RING COUNTER AS SAR LOGIC:

A better solution as compared with up/down counter consists in examining the most significant bit an-1 first and then in determining whether Vin is larger or smaller than VDD/2. The comparator gives the value of that bit directly. Then, the comparison is performed for the next bit, and so on until all bits are extracted, finishing by the least significant bit a0. This type of converter is called successive approximation converter. The complete process is faster than the iterative converter as only N comparisons are necessary.

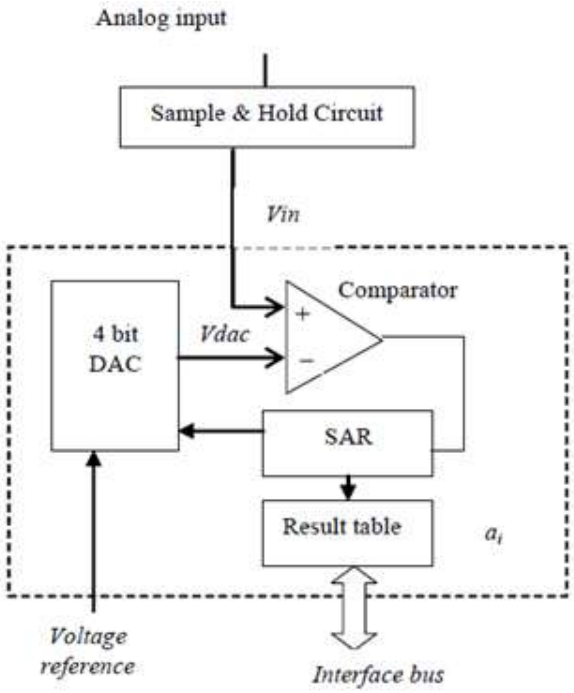

Figure 7: SAR Based ADC architecture

The schematic diagram of a successive approach converter is given in Figure 1. The analog input signal Vin is retained by a sample/hold circuit during the data conversion process. In the first clock cycle, the most significant bit ai of the successive approximation register (SAR) is set to 1. The DAC converts the SAR value to an analog voltage Vdac that is compared to Vin. If

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Vdac is smaller than Vin, the bit ai is validated at 1, and the SAR register is unchanged. Conversly, if Vdac>Vin, ai is set to 0. The DAC generation and comparisons processes are repeated for N clock cycles to complete the conversion.

Successive Approximation Register ADC represents the majority of the ADC market for medium to high resolution. This architecture requires just single comparator; an N-bit SAR ADC will require N comparison clock cycles and will not be ready for the next conversion until the current one is complete.

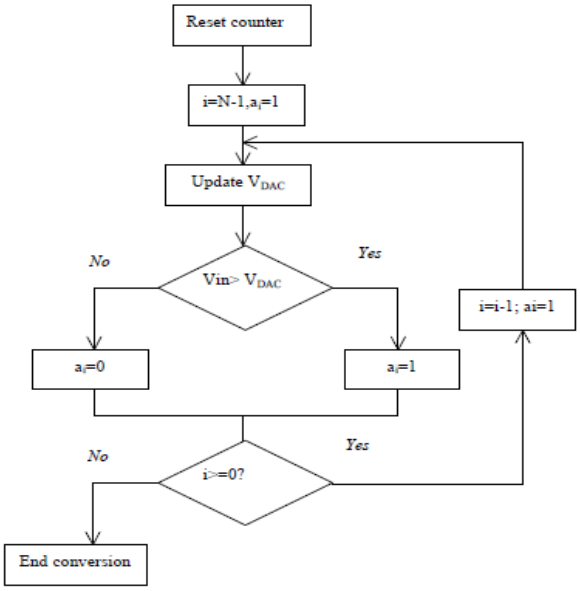

Figure 2: Iterative converter algorithm and a simple implementation

Microwind software tool provides you a simulation with respect to transient analysis for current and voltage.

Table 2: Conversion Data Table for our ADC

Analog Vtg I/P	ADC O/P	**Decimal**
0.0 V	0100	4
0.1 V	0100	4
0.2 V	0100	4
0.25 V	0100	4
0.3 V	0110	6
0.4 V	0111	7
0.5 V	1100	7
0.56	1100	12
0.6 V	1110	12
0.65 V	1110	12
0.7 V	1111	14
0.8 V	1111	15
0.9 V	1111	15
1.0 V	1111	15

Although the ADC has fair accuracy due to 4-bit architecture but it has good resolution on over N over reading for same input values.

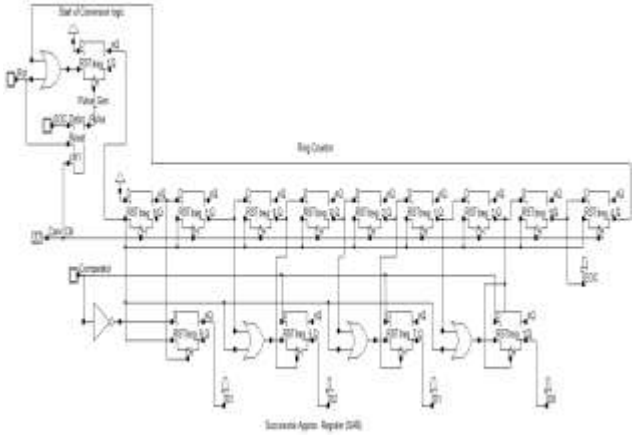

Figure 9: Design of ring counter based SAR logic

The counter based SAR ADC, it sets MSB. Then convert MSB to the corresponding analog output by using DAC. Then guess output will compare with the input. If Vin> half of ADC then it set the bit otherwise test the next bit. SAR ADC is capable of high speed and high resolution. They have low power consumption and low cost. They have medium accuracy and better tradeoffs between speed & cost. They have no pipeline delay.

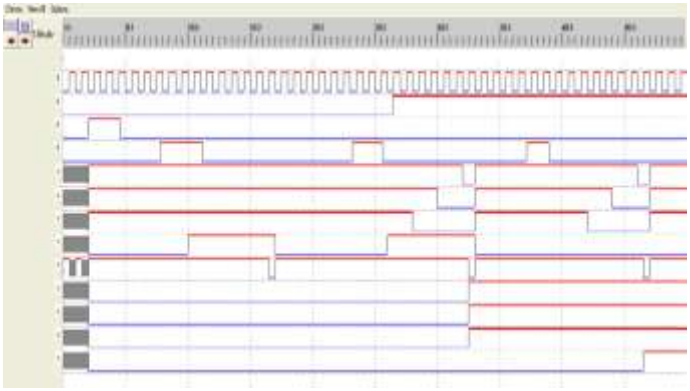

Figure 11: Simulation Results of SAR logic

The conversion end with EOC (end of conversion) signal, going active low to indicate end of conversion.The SAR logic o/p is given to DAC in the form of signal DAC3..0.

The DAC which we are using works on active low I/Ps, so this time we have inverted the o/p of SAR.

IV. SIMULATION RESULT:

For Health care systmes we are planning to design for, needs the high performance ADC.

The Microwind software tool provides you the way of simulation in all domains.

Case no. 1: Analog Input Voltage is Triangle waveform

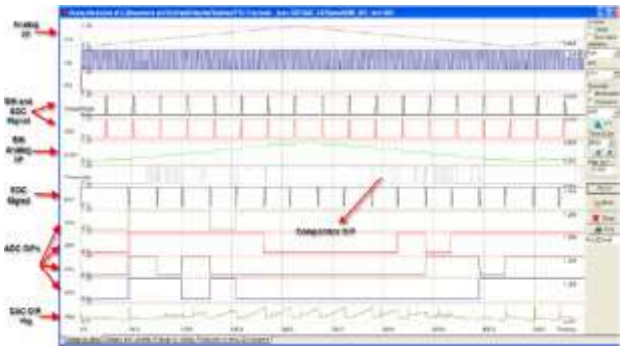

Figure 6: Transient analysis for Voltage

Here you can observe that of Vin >Vdac, the ADC gives lower count, and for Vin <Vdac , ADC gives higher count.

Case no 2: Analog Input Voltage is Square waveform from 0.3 to 0.8 V

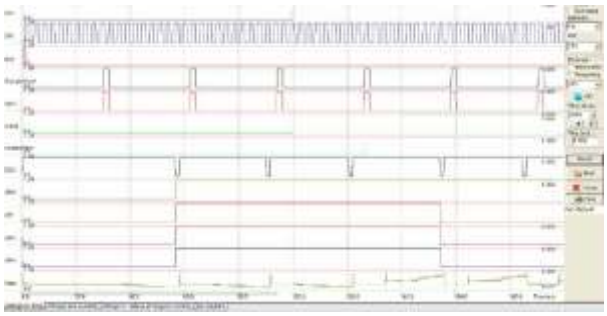

Figure 7: Transient analysis for volatge

Here you can observe that during initial period Vin (0.3v) <Vdac, the ADC gives higher count (1011), and later when Vin(0.8v) >Vdac , ADC gives lower count (0011).

Part I: For Ring Counter as SAR Logic:

Analog Input Voltage is Square waveform from 0 to 1.2 V	2.95mW
Analog Input Voltage is Square waveform from 0.3 to 0.8 V	2.76mW
Analog Input Voltage is Square waveform from 0.25 to 0.9 V	2.86mW
Analog Input Voltage is Sine waveform from 0.2V to 0.8V	2.79mW

Part II: For Ring Counter as SAR Logic:

Analog Input Voltage is Square waveform from 0 to 1.2 V	4.26 mW
Analog Input Voltage is Square waveform from 0.3 to 0.8 V	4.11 mW
Analog Input Voltage is Square waveform from 0.25 to 0.9 V	4.27 mW
Analog Input Voltage is Sine waveform from 0.2V to 0.8V	4.12 mW

V. CONCLUSION

In this paper, structure for up down counter logic and ring counter logic for designing of Successive Approximation Register based ADC.

Design logic is simple & easier to design. Although the ADC has fair accuracy due to 4-bit architecture but it has good resolution on over N over reading for same input values.
Also ADC has lower precision but it works good to learn about SAR based ADC design.

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