Review on: Performance Optimization of CSLA using HCA

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***Abstract*—** Adders form an almost obligatory component of every contemporary integrated circuit. There are different kinds of adder available out of which Carry Select Adder (CSLA) having best performance parameters. At present there is regular SQRT CSLA structure, in which the second level of SQRT is replaced by the Binary to Excess–I Converter (BEC) but still there is possibility to get better design in which optimization of area, delay is to be major concentrations as well as power requirement. RCA at its first level of CSLA requires more area. Hence this paper proposes CSLA with Han Carlson adder instead of Ripple Carry Adder (RCA) at its first level. In future, it can be observed from the results that compared with the CSLA with RCA and BEC at first and Second level, area and delay will reduce with comparable percentages when at the first level HCA will use at the first level 32-bit SQRT CSLA. This proposed logic is designed with VHDL technology in the XILINX 13.1 design suit.

***Keywords*—** *Binary excess converter(BEC),Han Carlson adder (HCA), Ripple carry adder(RCA), Carry Select Adder (CSLA), Regular SQRT CSLA, etc.*

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I. INTRODUCTION

Designing area efficient and less propagation delay VLSI systems has emerged as highly important because of the fast growing technology in mobile communications systems and computation. The mobile systems now becoming much thinner compare to that of earlier. There are also limitations to amount of power availability in the mobile systems as the battery also requires with small size. This is the reason why designers are now facing more constraints such as more speed, high throughput with minimum silicon area. That's why building area efficient and high performance adder cells are of great need. To reduce area needed for computational circuits, the size reduced into the deep submicron area and is commonly handled by the process engineering. There are different kinds of Adder designs have been proposed and implemented to minimise the power consumption. Logic minimization results in better area efficient designs as well as system throughput. The CSLA is used for computational systems to solve the problem of carry propagation delay by individually generating multiple carries and then select a carry to find out the sum from two individual adders. However, the CSLA is not area with the multiple pairs of RCA's to generate partial sum with carry input Cin=0 and Cin=1 then by using multiplexers the final sum and carry are selected with the help of. Section II of this paper reviews current logic and section III explains about modification in logic level which is replacement of first level of ripple carry adder (RCA) with Han Carlson Adder (HCA). Section IV includes results and comparisons. Finally the work is concluded in section V of this paper.

II. LITERATURE REVIEW

The reference 1 describes the power and area efficient carry select adder (CSA). Firstly, CSA is one of the fastest adders used in many data-processing systems to perform fast arithmetic operations. Secondly, CSA is intermediate between small areas but longer delay Ripple Carry Adder (RCA) and a larger area with shorter delay carry look-ahead adder. Third, there is still scope to reduce area in CSA by introduction of some add-one scheme. In Modified Carry Select Adder (MCSA) design, single RCA and BEC are used instead of dual RCAs to reduce area and power consumption with small speed penalty. The reason for area reduction is that, the number of logic gates used to design a BEC is less than the number of logic gates used for a RCA design. Thus, importance of BEC logic comes from the large silicon area reduction when designing MCSA for large number of bits. MCSA architectures are designed for 8-bit, 16-bit, 32-bit and 64-bit respectively. The design has been synthesized at 90nm process technology targeting using Xilinx Spartan-3 device. Comparison results of modified CSA with conventional CSA show better results and improvements. [1]

In this reference 2, the logic operations involved in conventional carry select adder (CSLA) and binary to excess-1 converter (BEC)-based CSLA are analyzed to study the data dependence and to identify redundant logic operations. We have eliminated all the redundant logic operations present in the conventional CSLA and proposed a new logic formulation for CSLA. In the proposed scheme, the carry select (CS) operation is scheduled before the calculation of *final-sum*, which is different from the conventional approach. Bit patterns of two anticipating carry words (corresponding to *c*in = 0 and 1) and fixed *c*in bits are used for logic optimization of CS and generation units. An efficient CSLA design is obtained using optimized logic units. The proposed CSLA design involves significantly less area and delay than the recently proposed BEC-based CSLA. Due to the small carry-output delay, the proposed CSLA design is a good candidate for square-root (SQRT) CSLA. A theoretical estimate shows that the proposed SQRT-CSLA involves nearly 35% less area–delay–product (ADP) than the BEC-based SQRT-CSLA, which is best among the existing SQRT-CSLA designs, on average, for different bit-widths. The application-specified integrated circuit (ASIC) synthesis result shows that the BEC-based SQRT-CSLA design involves 48% more ADP and consumes 50% more energy than the proposed SQRT-CSLA, on average, for different bit-widths.[2]

In this reference 3, to make addition operations more efficient parallel prefix addition is a better method. In this paper 16-bit parallel prefix addition has been implemented with the help of cells like black cell and white cell operations for carry generation and propagation. This process gives high speed computations with high fan-out and makes carry operations easier. This paper presents different types of parallel prefix adders and compares them with the Simple Adder. The adders are designed using Verilog HDL code and simulated and synthesized using Xilinx design suite 14.5 software tool and Modelsim altera 10.0c. In order to make it suitable for FPGA implementation, Han Carlson adder is modified using fast carry logic technique. The modified adder provides better performance over the Simple adder for the higher order bit widths.[3]

III. EXISTING LOGIC

As shown in the figure in the existing technique of CSLA includes three levels which include first level with 4-bit Ripple Carry Adder, second with 5-bit Binary to Excess Converter (BEC) block and then the third one with multiplexers block.

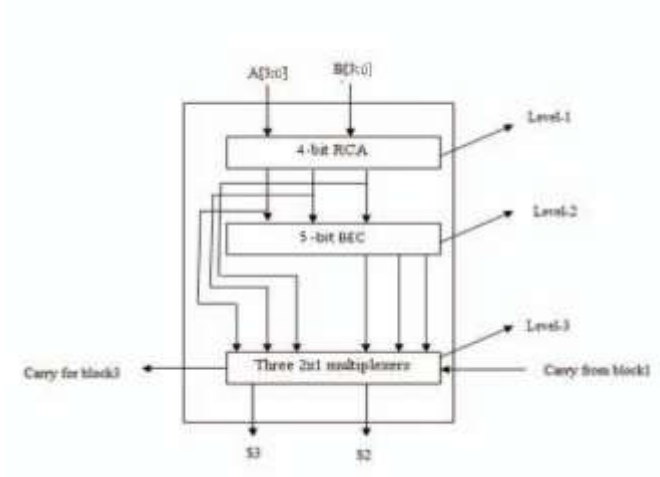

Fig. 1. Second block of SQRT CSLA with BEC instead of RCA in second level RCA

The drawbacks in the CSLA are large area needed as it uses RCAs at both the levels. For solving this problem and achieving increased area efficiency BEC is used instead of RCA with carry input Cin in the regular CSLA. An n+1 bit BEC is required for replacing n bit RCA. Second block of 4-bit SQRT CSLA with BEC at its second level is shown in figure.1. One input to the third level multiplexers is from output of first level RCA and another input is from BEC output. This gives the two different partial results in parallel and hence the multiplexer is need to select one of two outputs, the BEC output or the input corresponding to the control signal Cin.

IV. PROPOSED LOGIC IMPLEMENTATION

Though BEC technique with RCA in second level of CSLA reduces area and power still not up to considerable level and the design is incompatible with sub threshold level modifications. To overcome this, the proposed logic consists of HCA instead of RCA which is used in first level of second stage of CSLA. The figure 2 shows Second block of CSLA with HCA in first level RCA. This will reduce the critical path and hence delay would be reduced.

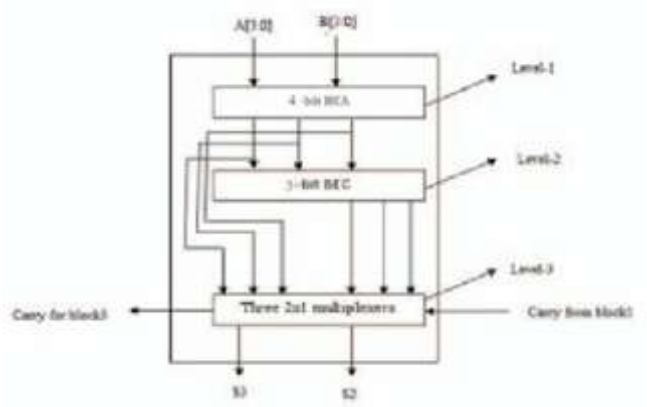

Fig. 2. Second block of CSLA with HCA in first level RCA

V. CONCLUSION

In this paper we studied all techniques related to CSLA and HCA. From the mentioned references it can observed that the critical path delay and area are not reduced to considerable level and by using this technique that is implementation of CSLA using HCA may produce better results. And this may be implemented for different kind of application where delay is critical parameter such as DSP processor, FPGA based applications, etc.

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