Implementation of Firing Scheme for Multilevel Inverter and its Hardware Implementation

Sarika D Patil
Department of Electrical Engineering
Rajiv Gandhi College of Engineering & Research, Nagpur
sdpatil79@gmail.com

Surbhi Patil
Rajiv Gandhi College of Engineering & Research, Nagpur
patilsurabhi91@gmail.com

Abstract:- The utility of multilevel inverters has been increased day by day. These converters are generally suitable for high voltage and high power application due to their ability to synthesize waveforms with reduced harmonics. Many topologies have been introduced, amongst these topologies the multilevel cascaded inverter is commonly used, as these are very popular and have many applications in electric utility and industrial drives. This paper proposes a method for calculating switching angles for firing circuit by using Newton -Raphson method. It involves the solution of non-linear transcendental equation whose solution is difficult to find. By calculating switching angles using N-R method, optimized switching angles can be calculated which will again reduce the certain number of harmonic components and THD as well. Firing pulses are generated through microcontroller ATMAEGA16 and the same results are validated through MATLAB simulation.

Keywords: *- Selective Harmonic Elimination PWM method (SHEPWM), Newton-Rapson (N-R) method, Cascaded H-Bridge Multilevel Inverter, MATLAB Simulink.*

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I. INTRODUCTION

Multilevel inverters have drawn increasing attention because of their applications in power systems and industrial drives. They can be efficiently used in the distributed energy systems in which, output ac voltage is obtained by connecting dc sources such as batteries, fuel cells, solar cells etc at input side of the inverters[1],[2],[3]. The ac output voltage obtained from the inverters can be fed to a load directly or interconnect to the ac grid without voltage balancing problems. In which each group of devices contribute to a step in the output voltage waveform. The steps are increased to obtain an almost sinusoidal waveform. The number of switches involved is increased for every level increment. Figure 1 shows the block diagram of the general multilevel inverter.

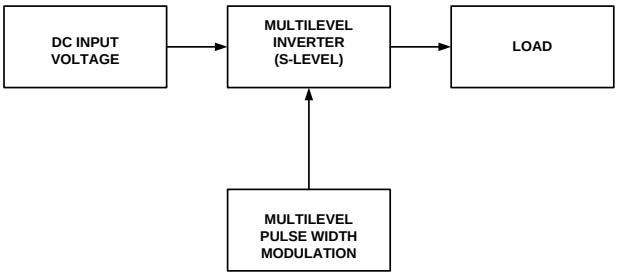

Fig.1 Block Diagram of Multilevel Inverter with Load

Compared to the single bridge inverter the multilevel inverter reduces the harmonics due to the multi switching process. The multilevel inverter produces different voltage levels by varying the switching sequence of the inverter. In multilevel inverter as the number of voltage levels increased the harmonics produced in the output waveform decreases relatively and vice versa[4],[5]. The cascaded multilevel inverter is one of the widely used topologies. It requires 'n' number of DC sources for '2n+1' number of level and it has the reduced number of switches compared to the other topologies of the multilevel inverters. Each H- Bridge is connected to the separate DC sources. Thus this topology provides high voltage at higher modulation frequencies with low switching losses[6].

A modified cascaded H-bridge Inverter is proposed in this project. To simulate the proposed method MATLAB / SIMULINK software is required. The basic structure of cascaded H Bridge multilevel inverter is shown in figure 1. Each inverter has dc as an input and output will be +Vdc, 0, -Vdc which is shown in figure 2.

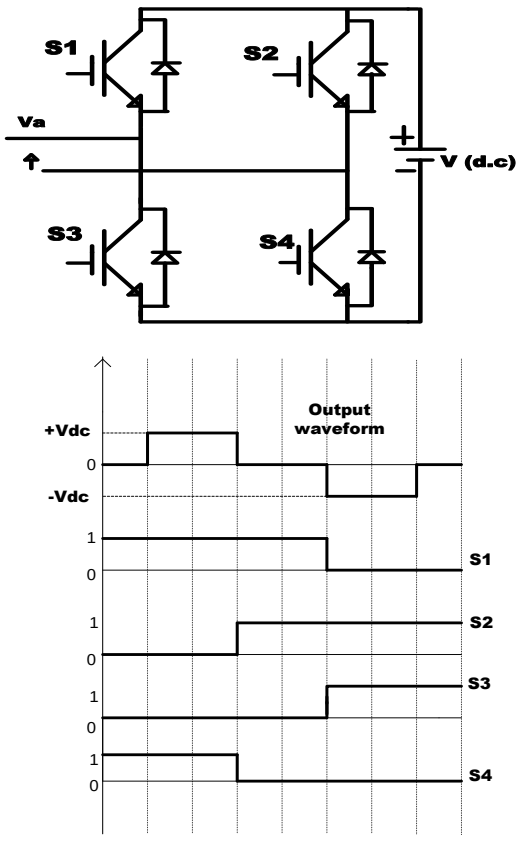

Fig.2 Output Voltage waveform for Three Level MI

II. PROPOSED MULTILEVEL INVERTER

In this paper, three level and five Level multilevel inverter is taken for a case study. This proposed converter uses less number of switches when compared to the other familiar topologies hence reducing initial cost because of the switch reduction. Multilevel inverter consists of IGBT switches and separate DC sources. By switching the IGBT at the appropriate firing angles, we can obtain the three levels and five level output voltage. IGBT is preferred because of its fast switching nature, low frequency and high power rating. Because of the reduction in the number of switches the initial cost reduces, controlling becomes easier, losses reduces due to the elimination of the harmonics, overall weight reduces as the usage of less number of components.

To produce multilevel output ac voltage using different levels of dc inputs, the semiconductor devices must be switched on and off in such a way that the fundamental voltage is obtained at desired value along with the elimination of certain number of lower order harmonics in order to have least harmonic distortion in the ac output voltage. For switching the semiconductor devices, proper selection of switching angles is necessary. The switching angles at fundamental frequency are obtained from the solution of non linear transcendental equations. These equations are known as selective harmonic elimination (SHE) equations. As the SHE equations are non linear transcendental in nature, their solutions may have simple, multiple and even no solution for a particular value of modulation index (*m*), moreover, it is difficult to solve these equations. To get all possible solution sets where they exist using simple and less computationally complex method is very difficult. Once these solution sets are obtained, the switching angles producing minimum total harmonic distortion (THD) in the output ac voltage are selected for switching of the power electronics devices. For these non linear transcendental equations or SHE equations iterative numerical techniques have been implemented for producing only one solution set. For this a proper initial guess and starting value of *m* for which the solutions can exist are required. It is difficult to guess the initial solution and the value of *m* for which solution exist. The switching angles have been calculated by using Newton Raphson (N-R) iterative numerical technique for specific range of modulation indices.

III. CASCADED MULTILEVEL INVERTER

The A multilevel cascade inverter consists a number of H-bridge cells that are connected in series per phase, and each module needs separate DC source for generation of voltage levels at the output of inverter.

$$\text{Vout} = \begin{cases} +V_{dc} & In_1, In_4 \text{ ON} \\ 0 & In_1, In_3 \text{ ON} \\ -V_{dc} & In_2, In_3 \text{ ON} \end{cases} \quad \ldots\ldots(1)$$

The switching inputs shown as Si, *i=1 to 4* in the Fig.2 allows obtaining output voltage. The H-bridge cells are serially connected over AC outputs to obtain expanded phase voltage levels. Cascade Multilevel Inverter (CMLI) is one of the most important topology.

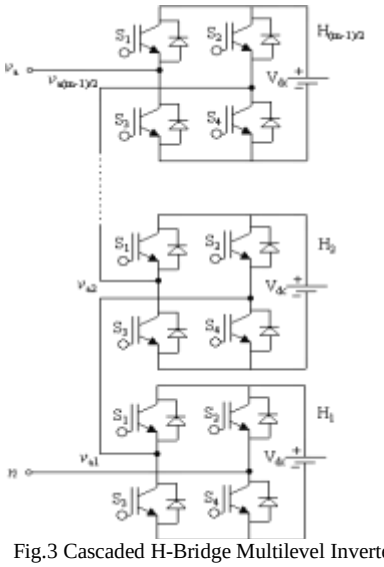

Fig.3 Cascaded H-Bridge Multilevel Inverter

The number of levels in the output phase voltage and line voltage are 2*s*+1 and 4*s*+1 respectively, where *s* is the number of H-bridges used per phase. For example, three H-bridges, five H-bridges and seven H-bridges per phase are required for 7-level, 11-level and 15-level multilevel inverter respectively. Fig. 4 shows a typical waveform produced by 7-level CMLI. The magnitude of the ac output phase voltage is the sum of the voltages produced by H-bridges. In the Fig. 4, α_1, α_2 and α_3 are the switching angles for three H-bridges in each phase. The magnitude and THD content of output voltage depends very much on these switching angles, therefore, these angles need to be calculated properly.

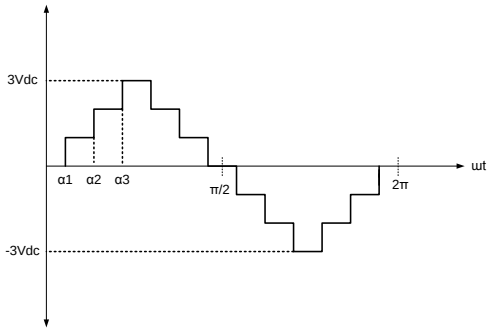

Fig. 4 Output phase voltage waveform for 7-level CMLI.

IV. SELECTIVE HARMONIC ELIMINATION

There are many popular methods are used to reduce the harmonics in order to get an effective results. The popular methods for high switching frequency are Sinusoidal PWM and Space Vector PWM. For low switching frequency methods are space vector modulation and selective harmonic elimination. The SPWM technique has disadvantage that it cannot completely eliminate the lower order harmonics, due to which it cause losses and requires high filter. SHE PWM technique uses many mathematical methods to eliminate specific harmonics such as 5th, 7th, 11th, and 13th harmonics. The popular Selective Harmonic Elimination

method is also called fundamental switching frequency based on harmonic elimination theory.

In general, the Fourier series expansion of the staircase output voltage waveform is given by eq.(1)

$$V_{an}(wt) = \sum_{n=1,3,5}^{\infty} \frac{4Vdc}{n\pi}(\cos(n\alpha_1) + \cos(n\alpha_2) + ... + \cos(n\alpha_s))\sin(nwt)$$

…… (1)

Where '*s*' is the number of H-bridges connected in cascade per phase and *k* is order of harmonic components and the switching angles should be between $0 \le \alpha_1 < \alpha_2 \ldots < \alpha_s \le \pi/2$.

From equation (1), the expression for the fundamental voltage in terms of switching angles is given by

$$\frac{4V_{dc}}{\pi}(\cos(\alpha_1) + \cos(\alpha_2) + ... + \cos(\alpha_s)) = V_1$$

…… (2)

The modulation index, *m*, is defined as the ratio of the fundamental output voltage (V_1) to the maximum obtainable fundamental voltage. The maximum fundamental voltage is obtained when all the switching angles are zero i.e.

$$V1max = 4sVdc/\pi,$$

therefore, $m = \pi V1/4sVdc$

For 7, 11 and 15-level cascade multilevel inverters, *s* = 3, *s* = 5 and *s* = 7 respectively. For example, in case of 7-level CMLI, only two harmonic components (in general, 5th and 7th) can be eliminated. From equation (1), the expressions for fundamental voltage in terms of *m*, and lower order harmonic components, when they are eliminated, can be written as for 7-level CMLI.

$$\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) = 3m$$
$$\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) = 0$$
$$\cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) = 0$$

…… (3)

The equation (3) are transcendental equations, known as selective harmonic elimination (SHE) equations, where unknown parameters are switching angles. The first equation of the set of equations given by (3) determines the magnitude of fundamental voltage for a given value of *m*, and the remaining equations eliminate selective harmonic components. The equations (3) are to be solved by employing N-R method in such a way that all possible solutions for a given value of *m* are obtained[8].

These equations are solved by using algorithm of N-R method which given as

1) Assume any random initial guess for switching angles (say α_0) such as $0 \le \alpha_1 < \alpha_2 \le \pi/2$.
2) Set $m_1 = 0$.
3) Calculate F(α_0), B(m_1) and Jacobian J(α_0).s
4) Compute $\Delta\alpha$ during the iteration using following equation, $\Delta\alpha = J^{-1}(\alpha_0)(B(m_1) - F(\alpha_0))$.
5) Update the switching angles i.e. $\alpha(k+1) = \alpha(k) + \Delta\alpha(k)$.
6) To bring switching angles in range solve the following equation $\alpha(k+1) = \cos^{-1}(abs(\cos(\alpha(k+1))))$.
7) Repeat steps (3) to (6) for number of iterations to attain error goal.
8) Increment m_1 by a fixed step.
9) Repeat steps (2) to (8) for range of m_1.
10) Plot the switching angle as a function of m_1 and different solution sets would be obtained.
11) Take one solution sets at a time and compute complete solutions set for the range of m_1, where it exists.

V. RESULTS & CONCLUSION

By using N-R algorithm Gate pulses are generated at different switching angles shown in Fig. 5.

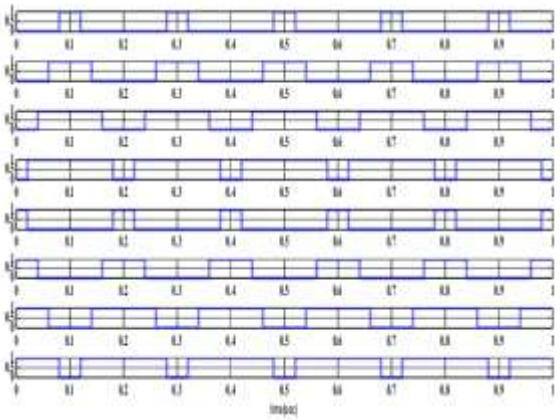

Fig. 5 Generation of gate pulses at different switching angles.

These firing pulses are given to IGBT switches for operation. Matlab Model of three level and five level can be implemented by using such switching techniques and therefore output voltage of three level and five level can be shown in Fig. 6 and Fig. 7.

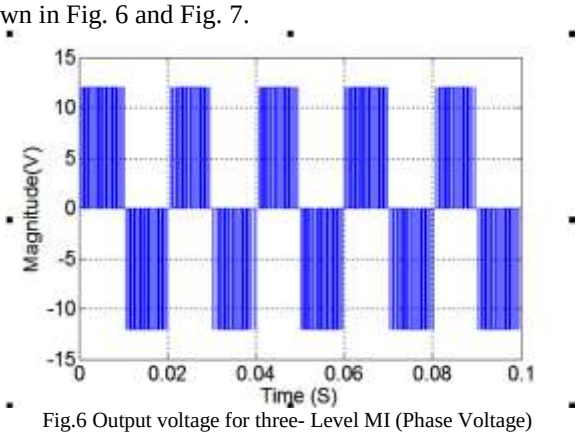

Fig.6 Output voltage for three- Level MI (Phase Voltage)

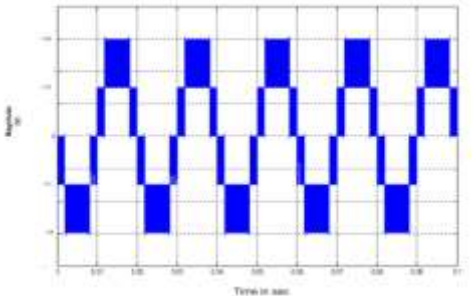

Fig.7 Output Voltage for five- Level MI (Phase Voltage)

VI. HARDWARE RESULTS

These firing pulses which is to be given to IGBT switches for operation are programmed by using microcontroller ATMEGA16. In this programming PORT A is used as a output port. The Flow chart for programming is shown in Fig.8.

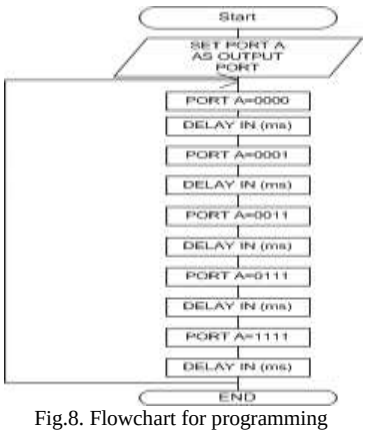

Fig.8. Flowchart for programming

The hardware for microcontroller ATMEGA16 and its output is shown in Fig.9, and Fig.10 respectively

Fig.9. Microcontroller IC ATMEGA16

Fig.10. Generation of Gate Pulses by ATMEGA16

The hardware implementation for Five Level multilevel inverter is shown in Fig.11. In this hardware, MOSFETS IRF840 are used as a switching devices. TLP 250 is used a driver circuit and firing pulses are provided by microcontroller IC ATMEGA16. The complete setup for five level multilevel inverter with switching circuit and is shown in Fig.11 and Fig. 12 respectively.

Fig. 11 The complete setup for five level multilevel inverter

Fig.12 Complete Hardware Setup

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