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Analysis of Cascaded Multilevel Inverter with Other Topologies

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Abstract:-Multilevel inverters have been important devices developed in recent years, showing to their capability to increase the voltage and power delivered to the load. Researches done based on basic inverter topologies shows that, Multilevel inverters have been widely used in medium and high-voltage applications as they have many advantages such as low power dissipation on power switches, low harmonic and low electromagnetic interference (EMI) outputs. For getting the improvement in inverter performance and quality of output, the different methods has been implemented such as, use of various switching strategies, use of Low Pass Filter to eliminate higher order harmonics ,use of Multilevel Structure in order to reduce harmonics and THD. The Selective harmonic elimination method for the staircase voltage waveform generated by multilevel inverter has been studied extensively in the last decade. The selective harmonic elimination method for 3-Pahase 7-Level Multilevel inverter using simple PWM Technique is proposed in this paper. MATLAB Simulink environment is used to simulate the results.

Keywords- *PWM – Pulse Width Modulation, FACTS-Flexible AC Transmission System, MLI- Multilevel Inverter, CHB-Cascaded H-Bridge, NPC- Neutral point Clamped, FC- Flying Capacitors*

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I. INTRODUCTION

Recently Multilevel Inverters are widely used in many industrial applications, where the requirement is medium voltage and high power [1],[2]. Multilevel Inverter has been widely used for chemical, oil, and liquefied natural gas (LNG) plants, water plants, marine propulsion, power generation, energy transmission, and power-quality devices [3], FACTS Devices [4]. According to Survey carried out in [3], cascaded multilevel inverter reaches the higher output voltage and power levels upto 13.8 kV, 30 MVA. Multilevel inverter is also playing important role in Renewable energy application for utility interface with grid [5].

While in comparison with traditional two-level voltage source inverters, multilevel inverters have several advantages. The main advantage of multilevel inverter is that is stepwise output voltage. This advantage results in higher power quality, lower switching losses, higher voltage capability moreover; it also reduces the cost with transformer less system at the distribution side. It has low distortion and low dv/dt, can draw input current with very low distortion, can generate smaller common-mode (cm) voltage, thus reducing the stress in the motor bearings, also it can operate with a lower switching frequency[6]-[8]. Desired output can be obtained from multilevel inverter with several number of dc voltages as inputs. If the number of levels is increased the output voltage and current waveform approaches to the sinusoidal waveform. The different topologies**,** control strategies and modulation techniques used for Multilevel inverters are presented in [3], [9]. There exist three commercial topologies of multilevel voltage-source inverters: neutral point clamped (NPC) [10], cascaded H-bridge (CHB) [11], and flying capacitors (FCs) [12].

TABLE I

COMPARISION OF M-LEVEL INVERTER ACCOURDING TO TOPOLOGIES

	Single Phase Topologies		**Three Phase Topologies**		
	Half Bridge	**Full Bridge**	**Diode Clamped**	**Flying Capacitor**	**Cascaded**
THDV (%)	163	156	36,9	33,1	32,4
Main power switches per phase	2	4	2(m-1)	2(m-1)	2(m-1)
Clamping diodes per phase	0	0	(m-1).(m-2)	0	0
DC Bus capacitor	2	2	(m-1)	(m-1)	(m-1)/2
Balancing capacitor per phase	0	0	0	(m-1).(m-2)/2	0
Total material for m=5	-	-	24	18	10
Control Scheme	Regular PWM	Regular PWM	SHE-PWM, SPWM, SVM	SHE-PWM, SPWM	SPWM, SVM
Applications	< 2kV	< 2kV	Motor drive, STATCOM	Motor drive., STAT COM	PV, Motor drive, STAT COM, Batteries

Cascaded multilevel inverters are based on a series connection of several single-phase inverters. This structure is capable to produce medium output voltage level as number of inverters increases. The Quality of output waveform of voltage and current can be improved by connecting three to ten inverters in series as presented in [13]. An exhaustive study of Multilevel Inverters and its applications in various fields is carried out continuously over last few years

II. GENERAL CASCADED MULTILEVEL INVERTER.

Cascade Multilevel Inverter (CMLI) is one of the most important topology in the family of multilevel and multipulse inverters. It requires least number of components with compare to diode-clamped and flying capacitors

type multilevel inverters and no specially designed transformer is needed as compared to multipulse inverter. It has modular structure with simple switching strategy and occupies less space [1], [3]. The CMLI consists of a number of H-bridge inverter units with separate dc source for each unit and is connected in cascade or series as shown in Fig. 1.

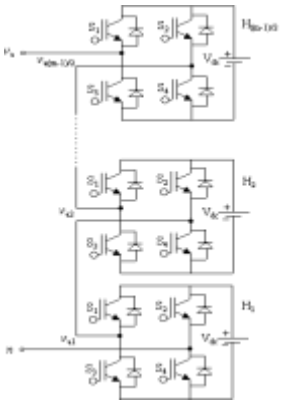

Fig. 1 configuration of single –phase Cascaded Multilevel Inverter

Each H-bridge can produce three different voltage levels: $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to ac output side by different combinations of the four switches S_1, S_2, S_3, and S_4. The ac output of each H-bridge is connected in series such that the synthesized output voltage waveform is the sum of all of the individual H-bridge outputs.

Fig. 2 shows the main H-bridge cell of one inverter used for implementation of the multilevel inverter. The full bridge inverter module includes four power switches to form an H-bridge. A multilevel cascade inverter consists a number of H-bridge cells that are connected in series per phase, and each module requires a separate DC source to generate voltage levels at the output of inverter. The objective of this paper is to develop a robustly designed inverter block with mathematical model for SPWM modulator to minimize THD ratios and compare to other conventional models. The inverter output values will be discussed for several switching frequencies and modulation indices applied to modulator.

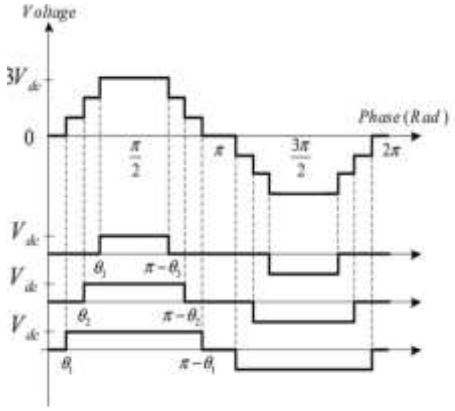

Fig. 2 Output voltage waveform of 7-level Cascaded Multilevel Inverter

Fig. 2 shows the output voltage waveform for 7-Level inverter The full bridge inverter module includes four power switches (IGBTs) to form an H-bridge as shown in Fig.1. A multilevel cascade inverter consists a number of H-bridge cells that are connected in series per phase, and each module requires a separate DC source to generate voltage levels at the output of inverter.

Switching states	Output voltages	S1	S2	S3	S4	S5	S6	S7	S8
+2	+2Vdc	1	1	0	0	1	1	0	0
+1	+1Vdc	1	1	0	0	1	0	1	0
0	0	1	0	1	0	1	0	1	0
-1	-1Vdc	0	0	1	1	1	0	1	0
-2	-2Vdc	0	0	1	1	0	0	1	1

Table.2 Switching table of single –phase Cascaded Multilevel Inverter

The switching inputs shown as In1, 2 in the Fig. 1 will allow obtaining output voltages. The H-bridge cells are serially connected over AC outputs to obtain expanded phase voltage levels and therefore, the total output level is the synthesize of cells' output of each H-bridge as shown in Fig.2.The output levels of each phase and each line voltage will be as shown in eq (2) and eq (3) respectively [19].

$$m = 2s + 1 \quad \text{Eq. 2}$$

$$\text{Switching devices} = 2(m-1) \quad \text{Eq. 3}$$

$$\text{DC Bus capacitors} = (m-1)/2$$

where's' is the number of bridges, 'm' is the number of levels.The ratio of DC voltage source naturally affects the output levels of a cascade multilevel inverter. The Fourier series expansion of the general multilevel stepped output voltage is shown in Eq. 4.

Where *n* is the harmonic number of the output voltage of inverter.

$$V(wt) = \sum_{n=1}^{\infty} Vn \sin(nwt) \qquad \text{Eq. 4}$$

Where

$$V(n) = \frac{4Vdc}{n\pi} \sum_{n=1}^{\infty} \begin{matrix} \cos(n\theta i) & for\ odd\ n \\ 0 & for\ even\ n \end{matrix}$$

The switching angles can be chosen to obtain minimum voltage harmonics. To satisfy fundamental voltage and to eliminate 5th and 7th harmonics, three nonlinear equations are as follows.

$$V1 = \frac{4Vdc}{\pi} [\cos(\theta 1) + \cos(\theta 2) + \cos(\theta 3)] \ldots \ldots \text{Eq. 5}$$

$$V5 = \frac{4Vdc}{5\pi} [\cos(5\theta 1) + \cos(5\theta 2) + \cos(5\theta 3)] \ldots \text{Eq. 6}$$

$$V7 = \frac{4Vdc}{7\pi} [\cos(7\theta 1) + \cos(7\theta 2) + \cos(7\theta 3)] \ldots \text{Eq. 7}$$

$$\text{Subject to } 0 < \theta 1 < \theta 2 < \theta 3 < \frac{\pi}{2}$$

For an 7-level cascade inverter, there are three H-bridges per phase i.e. $s = 3$ or three degrees of freedom are available; one degree of freedom is used to control the magnitude of the fundamental voltage and the remaining degrees of freedom are used to eliminate 5^{th} and 7^{th} order harmonic components as they dominate the total harmonic distortion [5]. The above stated conditions can be written in

support of above statement, an example is presented in which four solutions were computed for modulation index, m = 0.55 to 0.553as shown in Fig.3,Fig.4,Fig.5,Fig.6respecticvely. As m was incremented in steps of 0.001, it is observed that solutions are much sensitive to rather than the initial guess and rate of convergence is very high because all switching angles are in feasible range in all iterations. It may be noted that different initial guesses may produce different solutions for a particular value of m , but all solution sets will be produced (when they exist) if m is varied sufficiently in small steps.

III . Analysis & Simulation Results of 3 – Phase 7 level Multilevel Inverter

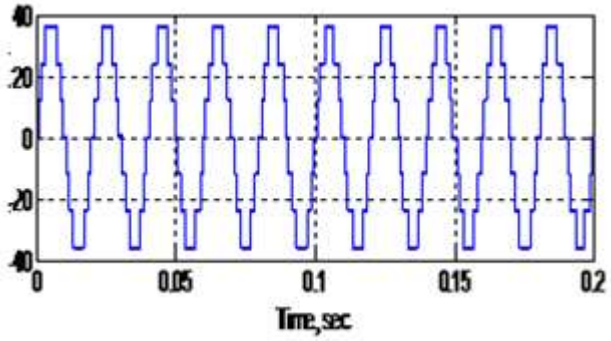

Fig. 7 Plot of Phase Voltage

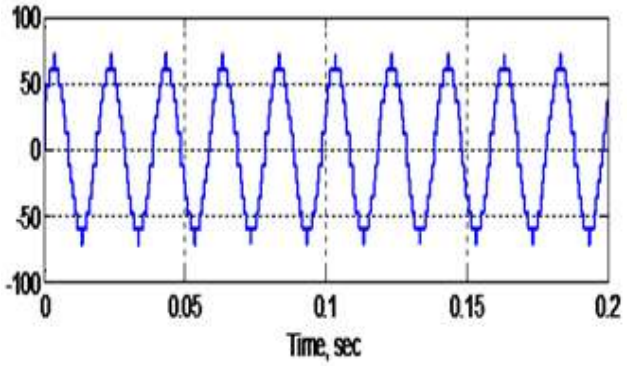

Fig. 8 Plot of Line Voltage

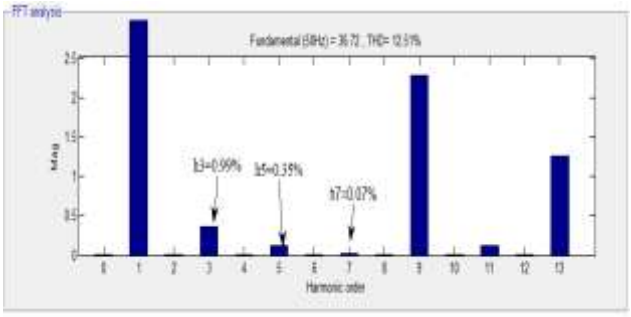

Fig. 9 bar Graph of FFT Analysis of Line Voltage

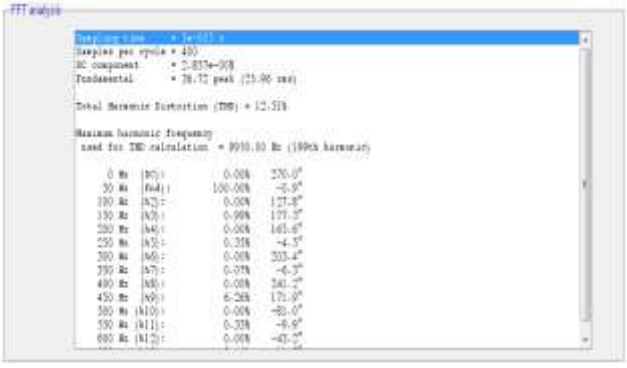

Fig. 10 List of Harmonics for FFT Analysis

IV. CONCLUSION

In this paper, a three-phase 7-level cascaded multilevel inverter with SPWM control has been presented. The results for Phase Voltage & Line Voltage for 7-Level Multilevel Inverter is shown in Fig.7 and in Fig.8.Whereas Harmonics and THD reduction is shown in Fig. 9 & Fig.10.The results obtained from simulation of Matlab-simulink shows high quality output. Also the Results shows harmonic contents & THD are greatly reduced by using Newton-Raphson Algorithm

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