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Data encoding schemes for reducing power consumption in Network on Chip

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***Abstract*—** In this paper, we design three different encoders to minimize power in network on chip. As we move in silicon technology paradigm from deep submicronmeter technology to ultra deep submicronmeter technology power dissipation rises. And this power dissipation begins to combat with network interface and router in communication system. The proposed system is very transparent and does not require any extra changes in router and link architecture. Proposed techniques assist to lower dynamic power dissipation and energy consumption without any degradation of performance and with very low area overhead.

Keywords- *Coupling switching activity, data encoding, low power, network-on-chip (NoC), power analysis.*

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I. INTRODUCTION

As the technology shrinks, many transistors can hold on smaller chip area. But at same time, it affects transistor performance and power gain. Chip multiprocessor (CMP) is more superior than traditional monolithic processors because of parallel and simultaneous execution of multiple programs or threads. When the cores on Chip multiprocessor (CMP) increase in number, network on chip becomes a better option than bus based design used for interconnection within the processor cores.

The advances in fabrication technology allow designers to implement a whole system on a single chip, but the inherent complexity of design of these systems makes it difficult to fully explore the potential of technology. So Systems-on-Chip (SoCs) design is based on the reuse of predesigned and pre-verified intellectual property core that are linked with special communication resources that must handle very tight performance and area constraints. With these application-related constraints, deep submicron effects pose physical design challenges for long wires and global on-chip communication. One solution to beat those challenges is to change from a fully synchronous design paradigm to a globally asynchronous, locally synchronous (GALS) design paradigm.

A Network on-Chip (NoC) is an infrastructure essentially composed of routers linked by communication channels. It is suitable to support the GALS paradigm, since it provides asynchronous communication, scalability, reusability and reliability.

The growing market for portable battery-powered devices adds a new dimension power to the VLSI design space previously characterized by speed and area. Power consumption is directly related to battery life as well as costly package and heat sink requirements for high-end devices. In order to ensure the final system complies to the desired function, thermal and cost requirements, the power consumption issues must be addressed during the design of all subsystems in a SoC, including the interconnect structure. Capacitances induced by long wires is a problem related with power consumption. Such problem is minimized in NoCs, since point-to-point short wires are used between routers. However, NoCs consumes power in routers, diminishing the apparent advantage in terms of power when compared to busses. The power consumption in a NoC grows linearly with the amount of bit transitions in subsequent data packets sent through the interconnect architecture. One way to reduce power consumption in NoCs in both wires and logic, is to reduce the switching activity by means of coding schemes. Many schemes were proposed and all of them suggesting communication architectures using bus.

II. LITERATURE SURVEY

The Network-on-Chip (NoC) paradigm has evolved to replace ad-hoc global wiring interconnects. With this approach, system modules communicate by sending packets to one another over a network. NoCs typically employ wormhole routing, i.e., each packet is divided into smaller units called flits, which are forwarded individually on links. NoC routers typically employ virtual channels which allows them to transmit several rows in parallel by interleaving their flits on a single outgoing link.

Chip accessibility is increasing day by day. In literature, many paper published for low power consumption. This paper mainly focused on link power reduction. The techniques such as shielding [10], increasing line to line spacing [11] and repeater insertion [3] are applied before for reducing power dissipation in network on chip.

There is classification of data encoding schemes. In first, encoding done by considering self switching activity on indivisual bus lines. And it ignores coupling activity. Bus invert (BI) and INC-XOR techniques are come under this category. In this, power dissipation increases due to coupling switching activity because of coupling capacitance. So, these techniques are not suitable for deep submicronmeter regime.

Second category, mainly focus on reducing power dissipation caused by coupling switching. And it can be done using extra control lines. But it increases design complexity and decoding logic becomes complicated.

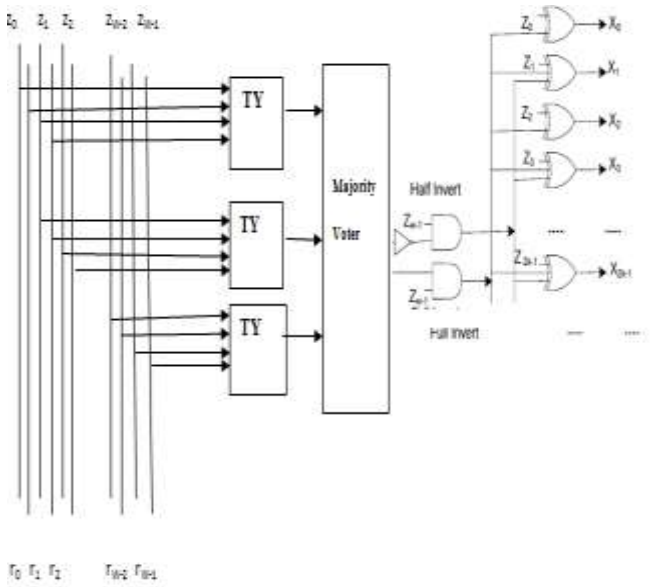
III. PROPOSED METHOD

We present the proposed encoding scheme whose goal is to reduce power dissipation by minimizing the coupling transition activities on the links of the interconnection network. Let us first describe the power model that contains different components of power dissipation of a link. The dynamic power dissipated by the interconnects and drivers is

$$P = [T_{0\to1}(C_s + C_l) + T_c C_c] V_{dd}^2 F_{ck} \quad (1)$$

Where T0→1 is the number of 0 →1 transitions in the bus in two consecutive transmissions, Tc is the number of correlated switching between physically adjacent lines,Cs is the line to substrate capacitance, Cl is the load capacitance, Cc is the coupling capacitance, Vdd is the supply voltage, and Fck is the clock frequency. One can classify four types of coupling transitions as described. A Type I transition come in exist when one of the lines make transition and other remains as it is. In a Type II transition, one line changes from low to high and the remaining one makes transition from high to low. A Type III transition occurs when both lines make transition simultaneously. And the last type, when no change in both lines.

A. Scheme I:



. Fig 1: encoder design of scheme I

In scheme I, comparison is made between previous and current data. And then come to conclusion that odd inversion or no inversion of current data is made. And decision made by encoder causes reduction in link power.

1) Power Model: the dynamic power on link after odd inversion of flit is,

$$P' \propto T'_{0\to1} + \left(K_1 T'_1 + K_2 T'_2 + K_3 T'_3 + K_4 T'_4\right) C_c$$

where T0→1, T1, T2, T3, and T4 are the self-transition activity, and the coupling transition activity of Types I, II, III, and IV respectively.

Odd inversion should occur or not is decided by given condition,

$$T_y > \frac{(w-1)}{2}$$

B. Scheme II

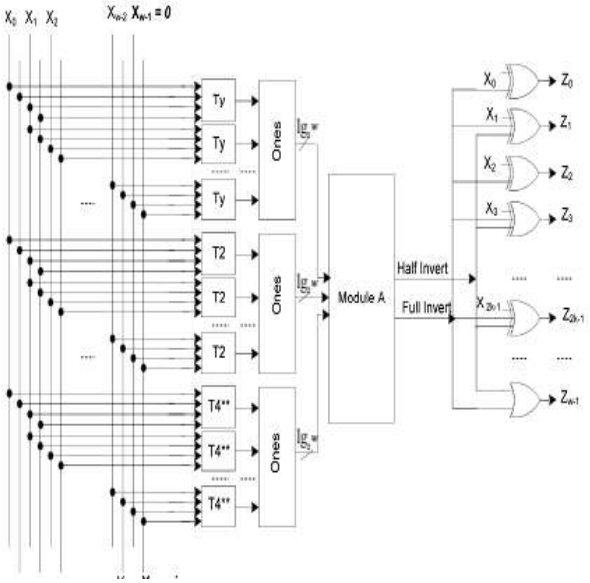


Fig 2: encoder design of scheme II

In scheme II, two types of inversion are used, either odd or even. And if, none of these causes reduction in link power then, no inversion is made.

Current data and previous data get compared and then decided which inversion is made, for having lowest power dissipation. In encoder, there is wth bit, which is used to tell if odd or full inversion occur (inv=1) and for no inversion (inv=0).

P, *P'* and *P''* are the power dissipation at a time when the flit is transmitted with no inversion, odd and full inversion by the link respectively. Power reduction exist in odd inversion condition when

$$P' < P \text{ and } P' < P'',$$

odd inversion condition is obtained as,

$$2\left(T_2 - T_4^{**}\right) < 2T_y - w + 1 \quad T_y > \frac{(w-1)}{2}$$

full inversion condition is as,

$$2\left(T_2 - T_4^{**}\right) > 2T_y - w + 1 \quad T_2 > T_4^{**}$$

If no condition is satisfied then no inversion will be done.

C. Scheme III:

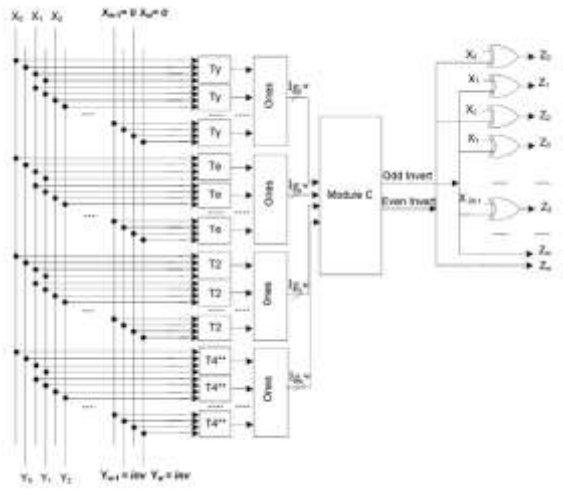


Fig:3: encoder design of scheme III

Condition when Full inversion,

$$2\left(T_2 - T_4^{**}\right) > 2T_y - w + 1, \quad \left(T_2 > T_4^{**}\right)$$
$$2\left(T_2 - T_4^{**}\right) > 2T_e - w + 1.$$

condition when odd inversion,

$$2\left(T_2 - T_4^{**}\right) < 2T_y - w + 1, \quad T_y > \frac{(w-1)}{2}$$
$$T_e < T_y.$$

No inversion is made when above mentioned conditions are satisfied.

IV. RESULT

The result of simulation are get by using Xilinx software. Here, scheme I minimizes type I and type II transitions by using encoder made by scheme I. Scheme I uses odd inversion. Scheme II reduces type II transitions and it uses odd inversion or full inversion. And in scheme III, it uses either odd inversion or even inversion according to the satisfactory condition.

By reducing transitions switching and coupling switching activity will get reduce. Proposed method is used to reduce dynamic power dissipation. By using these proposed architecture, dynamic power dissipation reduces.

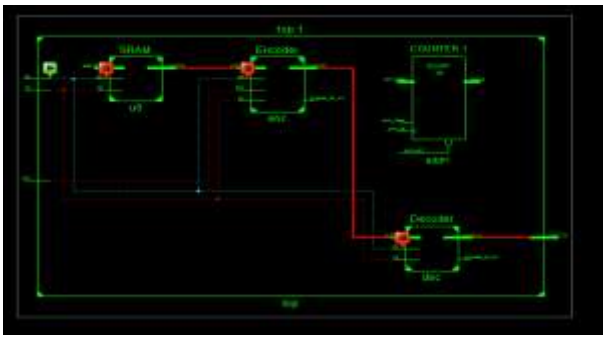


Fig 4: RTL view

Fig 5: Simulation result of scheme I

Fig 6: Simulation result of scheme II

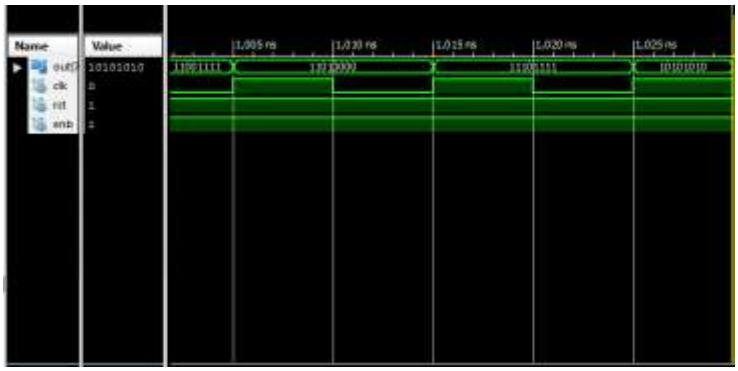


Fig 7: Simulation result of scheme III

V. CONCLUSION

In Network on Chip, links are mainly considered as a source of power dissipation. And power dissipation due to links will increase as technology shrinks means when we move towards deep submicronmeter technology. Our proposed scheme, minimizes power dissipation occurred because of links. It not only reduces switching activity but also coupling switching activity. Because of this, dynamic power dissipation reduced. The encoders made by scheme I, II, III are implemented by considering power dissipation and area. They are made by using Xilinx software. These schemes allows saving of power dissipation and reduction in area utilization with less area overhead.

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