International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169
Volume: 4 Issue: 5 146 - 149

Design of Transmitter & Receiver of UART in VHDL

Miss. M. A. Choudhari *
(PG Scholar)
Comm(Electronics) Engg
S.D.C.E Selu (Kate)
Wardha,
manalichoudhari082@gmail.com

Mr. S. B. Pawar
Assistant General Manager
Uttam Value Steel Pvt.Ltd
Selukate,Wardha

Prof. S. M. Sakhare
Assistant Professor,
Dept.of E & C Engg
S.D. C.E.Selu (Kate)
Wardha, India
shaileshsakhare2008@gmail.com

***Abstract*:-** Universal Asynchronous Receiver Transmitter (UART) is mostly used for serial data transmission protocol that supports full-duplex serial communication. In UART the transmitter is most important device for transmission of data and Receiver is for receiving the data. So here designing the asynchronous transmitter and receiver for UART. Hence number of UART is proportional to number of channels therefore we proposed to design UART using master slave configuration.

Keyword:-*Universal Asynchronous Receiver Transmitter, VHDL Implementation, Serial Communication Protocol, Status Register, Master Slave.*

*****

I. INTRODUCTION:

. Universal Asynchronous Receiver Transmitter (UART) is mostly used serial data transmission protocol to support full-duplex serial communication. UART has many advantages, such as simple resources, unfailing performance, strong anti-jamming capability, easy to control and understand and so on. It becomes one of standard integrated peripherals of various processors, such as chips 8250, 8251, 16550. It contains a parallel-to-serial converter for data transmitted from the computer and a serial to parallel converter for data coming in by way of the serial line. Parallel communication increases the cost so here uses the serial communication protocol. The UART also has a buffer for temporarily storing data from immediate transmissions. we proposed to design UART using master slave configuration.

The UART implemented with VHDL language is included into the FPGA to achieve compact, stable and reliable data transmission. Various designs are found in literatures for UART has different systems have different requirements and which require data communication between its functional units. In recent years the researchers has proposed various UART designs like automatic baud rate synchronizing capability, predictable timing behavior to allow the integration of nodes with imprecise clocks in time-triggered real-time systems, recursive running sum clean to remove noisy samples, integration of only core functions into a FPGA chip to achieve compressed, stable and reliable data transmission to keep away from waste of resources and decrease cost, programming logic to enable interfacing between asynchronous communications protocols and DSP having synchronous serial ports. UART has only one port to transmit and receive the data. So here increases the number of port using Master Slave. This frame was received at the receiver input where de-framing was done and only the data bits are available in parallel form at the receiver output has LCR, Baud Rate Generator (BRG), transmitter and Receiver as its functional units.

II. ASYNCHRONOUS TRANSMITTER:

The transmitter accepts parallel data from peripheral/processor, makes the frame of the data and transmits the data in serial form on the Transmitter Output (TXOUT) terminal. The baud rate generator output will be the clock for UART transmitter

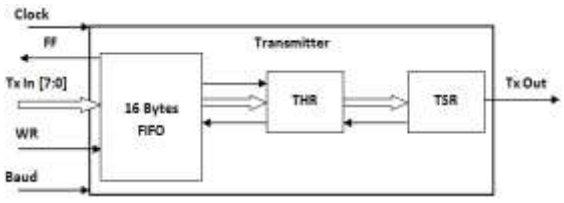

Fig. 1: UART Transmitter

Data is loaded from the inputs TXIN0-TXIN7 into the Transmitter FIFO by applying logic high on the WR input. If words less than 8 bits are used, only the least

significant bytes are transmitted. FIFO is 16-byte register. When FIFO contains some data, it will send the signal to Transmitter Hold Register (THR), which is an 8-bit register. At a same time, if THR is empty it will send the signal to FIFO, which indicates that THR is ready to receive data from FIFO. If Transmitter Shift Register (TSR) is empty it will send the signal to THR and it indicates that TSR is ready to receive data from THR.TSR is a 12-bit register in which framing process occurs.The status check using status register.

III. ASYNCHRONOUS RECEIVER:

The received serial data is available on the RXIN pin. The received data is applied to the sampling logic block. The receiver timing and control is used for synchronization of clock signal between transmitter and receiver.

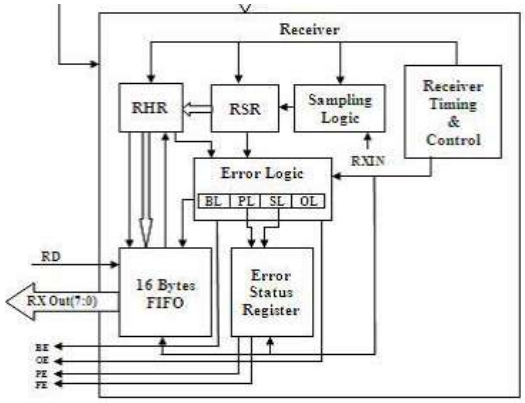

Fig. 2: UART Receiver

Whenever it goes low sampling and logic block will take 4 samples of that bit. If all four are same it indicates the start of a frame. After that remaining bits are sampled in the same way and all the bits are send to Receiver Shift Register (RSR) one by one where the entire frame is stored. RSR is a 12 bit shift register. The receiver sampling is 16 times to that of the transmitter baud rate. In the architecture of UART receiver (fig. 4), initially the logic line (RxIn) is high.

Now if the Receiver Hold Register (RHR) is empty it sends signal to RSR so that only the data bits from RSR goes to RHR which is an 8 bit register. The remaining bits in the RSR are used by the in tte sense of error logic block. Then, if receiver FIFO is empty it send the signal to RHR so thats the data bits goes to FIFO [14]. When RD signal is asserted the data is available in parallel form on the RXOUT0- RXOUT7 pins. The status register [5], [9] is implemented with flags for error logic operations performed on the received data. The error logic block handles 4 types of errors: Parity error (PE), Frame error (FE), Overrun error (OE), Break error (BE). If the received parity does not match with the parity generated from data bits, PE bit will be set which indicates that parity error occurred. If receiver fails to detect correct stop bit or when 4 samples do not match frame error occurs and FE bit is set. If the receiver FIFO is full and other data arrives at, RHR overrun error occurs and OE bit is set. If the RXIN pin is held low for long time than the frame time then there is a break in received data and break error occurs and BE bit is set.

IV. RELETED WORK:

The various researchers have worked on the Design of UART in VHDL.Some researches reviewed are as follows:

[1]This paper focuses on the VHDL implementation of UART with status register which supports asynchronous serial communication. The paper presents the architecture of UART.

[2] This paper focuses on the design of a UART chip with embedded Built-In-Self-Test (BIST) architecture using FPGA technology. The paper starts by describing the actions of UART circuit using VHISC Hardware Description Language (VHDL).

[3]This paper focuses on the design of quick UART. The paper starts by describing the behavior of UART circuit using VHDL. In the result and simulation part, this paper is focus on the bit errors detection. Besides, in the Baud Rate Generator part, the Baud Rate Generator is incorporated into the UART design before the overall design is synthesized.

[4]In this paper, Baud rate generator is used to offer the position time of sending and receiving data for transmitter module and receiver module.

[5]This paper was introduced universal asynchronous serial protocols, described the role of UARTs, and defined the basic situation for winning data transmission.

V. SIMULATION RESULT:

A. Simulation result of transmitter:

The fig. 10 shows the serial transmission of data. Data transmitted is "10101010". This 8-bit data is loaded to transmit shift register and start, stop & parity bits are added to form the frame inside TSR and sent to TXD. When the reset is 0 and transmit is 1, the transmitter starts transmitting the data. i.e. the data starts shifting out from the transmitter shift register. Since the desired baud rate is 9600bps, the bits are shifted out on TxD line at the interval of 50MHz/9600=5208 clock cycles. Similarly all the bits are sent. The serial transmission is observed at TXD pin along with frame format (1 logical low start bit, 8-bit data (LSB to MSB), parity bit and finally logical high stop bit).

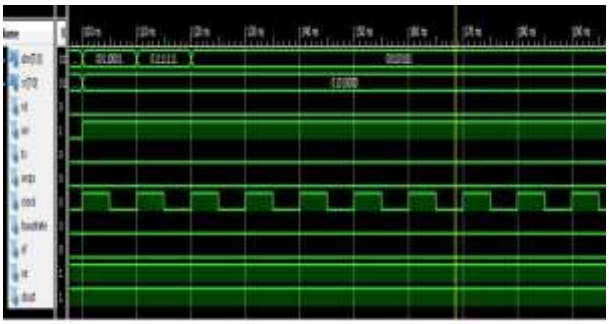

Fig:- 3. Output Of Transmitter

B. Simulation result of Receiver:

The UART receiver converts the serial data into parallelform and makes it available atRxData[7:0]. The Serial datais received at RXD pin. Each bit is sampled and the sampledbit is saved into receive shift register. From this, the frame
bits viz. start, parity and stop bits are discarded in RSR andwritten to receive FIFO, RxData. The 8-bit data simulated is"11111111". Further received data will be stored in the remaining FIFO locations. Fig. shows the reception of
serial data.

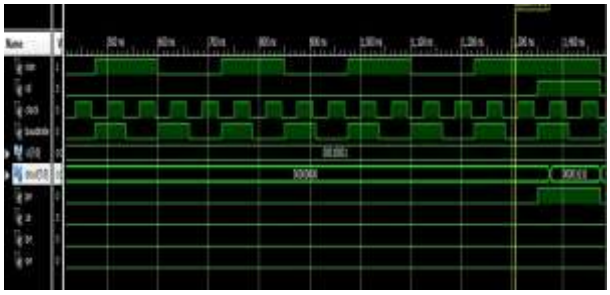

Fig:- 4. Output Of Receiver

VI. CONCUSION:

Universal Asynchronous Receiver Transmitter (UART) is mostly used serial data transmission protocol to support full-duplex serial communication. UART have advantages, such as simple resources, reliable performance, strong anti-jamming capability, easy to operate and realize. Implementation using VHDL is essential to achieve compact, stable and consistent data transmission to avoid waste of possessions and decrease cost. UART was implemented using different techniques to realizecompressed stable and reliable data transmission but single UART can communicate only with single channel. Hence number of UART is proportional to number of channels therefore we proposed to design UART using master slave configuration.

REFERENCE

[1] Naresh Patel, et al, "VHDL Implementation of UART with Status Register", in IEEE International Conference on Communication Systems & Network Technologies, 2012, pp 750 – 754.

[2] M. Y. I. Idris, et al, "A VHDL Implementation of BIST Technique in UART Design", in IEEE Conference on Convergent Technologies for Asia Pacific Region, 2003.

[3] J. Norhuzaimin, et al, "The Design of High Speed UART", in IEEE Asia Pacific Conference on Applied Electromagnetics, 2005, pp 306 – 310.

[4] He Chun Zhi, Yin-shui, Xia; Lun-yao, Wang; "A Universal Asynchronous Receiver Transmitter Design", in IEEE International Conference on Communication & Control, 2011, pp 691 – 694.

[5] ArpitaTiwari, Ravi Mohan &DivyanshuRao, "FPGA Implementation of Advanced UART Controller using VHDL", in International Journal of Research in Engineering & Technology, Vol. 2, Issue 8, Aug 2014, pp 23-32.

[6] Neeta Choubey, Mr. H. R. Singh, "Implementation of UART with Status Register and APB", in International Journal of Art & Humanity Science, Volume 2 Issue 4, July-August 2015, pp 01-10.

[7] H. Yuan, J. Yang, and P. Pan, “Optimized design of UART IP soft core based on DAM mode,” 2010 the 5th IEEE Conference on Industrial Electronics and Applications, Taichung, Taiwan, June. 15-17, 2010, pp. 1907-1910.

[8] Fang Yi-yuan; Chen Xue-jun; "Design and Simulation of UART Serial Communication Module Based on VHDL," Intelligent Systems and Applications (ISA), 2011 3rd International Workshop on Digital Design, vol., no., pp.1-4, 28-29 May 2011.

[9] Yamani IdnaIdris, MashkuriYaacob, A VHDL Implementation of BIST Technique in UART Design, Faculty Of Computer Science And Information Technology, University Of Melaya, 2003.

[10] Charles Roth, “Digital System Design using VHDL”, Cengage Learning, 2010.