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Development of Multiplier & Divider Architecture for Convolution and Deconvolution Algorithm Based on Ancient Indian Vedic Mathematics

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***Abstract*—** Convolution and deconvolution is the most important operation in digital signal processor, it is widely used in the area of in digital signal processing. Multiplier and divider are the important blocks of convolution and deconvolution algorithm but both the operations required more time and power consumption. This paper introduces the concept of developed multiplier and divider using Vedic mathematics. Architecture of multiplier and divider is developed with the help of Urdhvatriyagbhyam and nikhilam sutras. These sutras are implemented in VHDL and result is simulated by using ModelSim and Xilinx ISE.

Keywords- *convolution; deconvolution; urthvatriyagbhyam; nikhilam; vedic mathemetics;*

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I. INTRODUCTION

The operation of convolution and deconvolution is mostly used in digital signal processing. Digital signal processing plays very important role in many areas like electronics and electrical engineering. Discrete convolution and deconvolution is the center of many applications in Digital signal processing and image processing. However researcher may struggle with the convolution and deconvolution because of the concept and computation required number execution step those are slow and tedious to perform operation like multiplication and division. Excess time consumption, power consumption and complexity are the major problem in engineering which motivates to focus on different techniques which are easy to implement. So that many researchers trying to developed and improved the performance of convolution and deconvolution system by using advance algorithm and hardware. Vedic mathematics is the unique solution for the problem of convolution and deconvolution. Many branches of engineering use Vedic mathematics, specially use in digital signal processing .Vedic mathematics has total sixteen sutras and sub sutras which covers the all mathematical branches such as statistic, algebra, geometry and trigonometry. For the implementation of multiplier and divider two sutras are used one is Urthvatriyagbhyam which is use for multiplication and second is Nikhilam sutra which is use for performing division operation.

II. VEDIC MATHEMATICS

Veda is the Sanskrit word which is derived from the root 'ved', meaning is known as without limit. Vedic mathematics was reconstructed by Swami Bharti Krishna Tirthaji Maharaj from ancient Indian Vedas. It is based on sixteen principal which is term as sutras. Vedic mathematics is a very interesting field which includes effective algorithm which is applied on various engineering branches like digital signal processing. The result of vedic mathematics save the computational time. From the sixteen sutras of Vedic mathematics this paper uses two sutras Urdhvatriyagbhyan and Nikhilam for the design of multiplier and divider architecture.

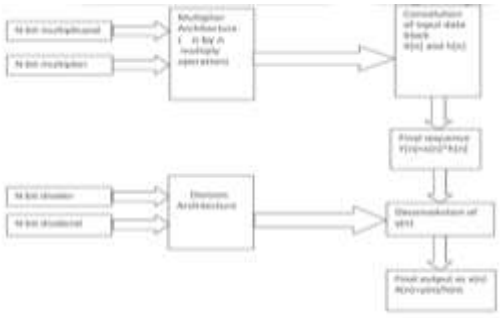


Figure1. Block diagram of Convolution & Deconvolution Architecture

A. *Convolution Method*

Convolution is the base of Digital signal processing. In this approach system combines two different signal and produce third signal with the knowledge of impulse response of system. Convolution takes two functions as input and developed third output signal [4].

$$Y(m) = X(m) * H(m) \quad (1)$$

$$Y(m) = \sum_{k=-\infty}^{\infty} X(m)H(m-k) \quad (2)$$

Consider X (m) is first length sequence (1, 2, 3, 4) and H (m) is second length sequence is (2, 1, 1, 3). The convolution of X (m) and H (m) given below

X (m)	1	2	3	4
H (m)	2	1	1	3

		2	4	6	8		
			1	2	3	4	
				1	2	3	4
					3	6	9	12
Y (m)	2	5	9	16	13	13	12

B. Deonvolution Method

Deconvolution is the reverse processes of convolution. Deconvolution is an operation which takes one input which convolved sequence Y (m) and second input sequence is H (m) and produce third output sequence which is original sequence X (m).

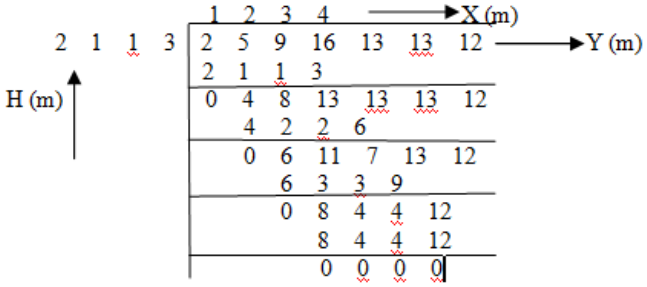


Figure.2. Example of Deconvolution Method

III. SYSTEM DESCRIPTION

A. Vedic Multiplier

Multiplier is designed by using Urdhvatriyagbhyam sutras among all traditional multiplier Vedic multiplier is faster multiplier which reduce excess time, power consumption and occupies less area. Vedic mathematics provides simplest way to perform multiplication.

To illustrate the multiplication algorithm, let us consider the multiplication of two binary numbers X3 X2 X1 X0 and Y3 Y2 Y1 Y0. The result of this multiplication may be more than four bits and output is Z0 Z1 Z2 Z3 Z4 Z5 Z6 Z7. Diagram for multiplication of two 4-bit numbers shown in below.

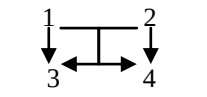
X3 X2 X1 X0

Y3 Y2 Y1 Y0

Z7 Z6 Z5 Z4 Z3 Z2 Z1 Z0

Consider the two binary numbers X3 X2 X1 X0 and Y3 Y2 Y1 Y0. The result of this multiplication may be more than four bits and output is Z0 Z1 Z2 Z3 Z4 Z5 Z6 Z7.

Z (0) =X3.Y3
Z (1) =X3.Y2+X2.Y3+C0
Z (2) =X3.Y1+X2.Y2+X1.Y3+C1
Z (3) =X3.Y0+X2.Y1+X1.Y2+X0.Y3 +C2
Z (4) =X2.Y0+X1.Y1+X0Y2+C3
Z (5) =X1.Y0+X0.Y1+C4
Z (6) =X0.Y0+C5
Z (7) =C6



3: 4+6: 8

B. Vedic Divider

Nikhilam sutra is use for designed Vedic divider, the meaning of Nikhilam Navatascaramam Dasatah means all from 9 and the last from 10. Consider the example 34 divide by 8. Firstly find the 10' complement of denominator the divide the numerator by an 'i' such that if many digit present at right of 'i' as there are digit in denominator.

8		2	
1	2	3	
0	2	8	
1	4	1	1
1	5	3	

- In the first step we take 10's complement of denominator and 8's 10's complement is 2.
- In second step numerator has been divide by the 'i' there are many digits present to the right side of the 'i'.
- After that we put a zero below first digit of the numerator.
- Now add the digits in that column of numerator to got a sum of 1 (1 + 0 = 1) and multiply it by 2 which is 10's complement of 8 then we got 2 (1 x 2 = 2). Put this value below the next digit of the numerator.
- Continuously follow this process up to last digit.

IV. STIMULATION RESULT

The Vedic Multiplier proposed in this paper is simulate and synthesized using Xilinx and ModelSim

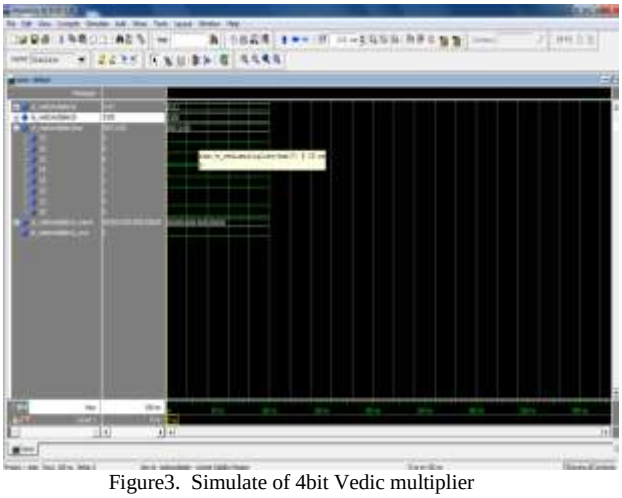


Figure3. Simulate of 4bit Vedic multiplier

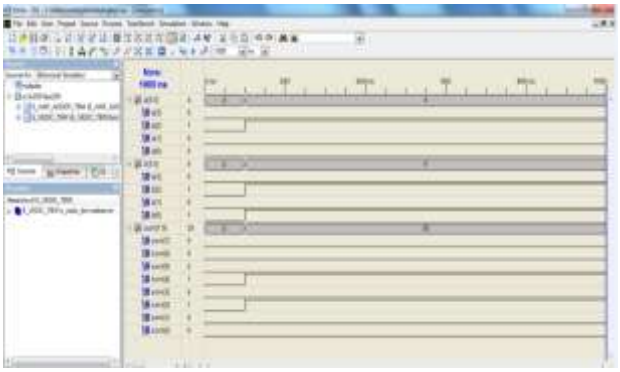


Figure4. Simulate Result of 4BitVedic Multiplier

V. CONCLUSION

The main aim of this paper is to introduce an easiest method for design of multiplier and divider algorithm for high speed convolution and deconvolution algorithm by using Vedic mathematics. It required less area, less power consumption and less execution time and it also reduce the path and time delay. In future this paper can be implemented for signed numbers.

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