Dynamic Priority Based Matrix Arbiter for NoC Router

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***Abstract*–**Network-on-chip((NoC) is a general purpose on chip means Network on Chip is a new method for communication to solve a problem that new challenges faced on system on chip. In router, Arbiter is used in network on chip when number of input are requested for same output port, the arbiter has generate the grant signal on the basis of that number of input port getting a priority and the input port transmit a packet to output port. Dynamic priority of a packet is given according to the traffic load of previous router. In certain router, if many packets request the same output channel, the router need to choose one of these packet, and deliver it to next router. In the dynamic priority based round robin arbiter gives low power consumption, reduced in delay & along with area gate count. In this paper we studied dynamic priority based round robin arbiter with help of scheduler algorithm. The scheduler algorithm states that if we send request to first signal it will enable first output request and remaining request get disable according to their priority.

Keywords*-Network on Chip (NoC),Dynamic Priority (Dp)*

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I. INTRODUCTION

In recent years, many researches of the NoC design make on effort to improve the performance by using routing algorithm or chaining router architecture Network-On-Chip (NoC) consists of routers, links, and network interfaces. Routers direct researches of the NoC design make on effort to improve the performance data over several links (hops).[1]

The NoC architecture has two parts: router and data link. The router can store and forward data, and the data link can transmit signals from one router to its neighbor. The input buffer stores the input data temporarily, The arbiter receives requests from input buffers and allocates virtual channels to requests and then gives grant signals to request initiators. The crossbar switches granted input requests and forwards the request data to data link, and then the request data is transmitted to the next hop router through data Link. In the NoC it consist of an NoC architecture andNoC router architecture which design a router it consist of three parts arbiter, buffer, crossbar In the Dynamic Priority the different channels are requested for different locations then the dynamic priority arranged that signal then dynamic priority arranged in equilibrium. Dynamic priority of a packet is given according to the traffic load of previous router. In certain router, if many packets request the same output channel, the router need to choose one of these packet, and deliver it to next router. Dynamic priority based Round Robin Arbiter will operates on the principle that a request that was just served should have the highest priority and next round of arbitration. In this paper we will design dynamic priority based matrix arbiter which will reduced time and improve the speed to make better transmission of signal.

II. LITERATURE REVIEW

A. NoCArchitecture

In the NoC architecture the Network-On-Chip (NoC) consists of links, routers and network interfaces. Routers direct data over several links (hops). Topology defines their logical lay-out (connections). Network-on-Chip (NoC) is an alternative for communication in SoCs with ability of providing high throughput, low atency and scalability..NoC architectures are based on packet-switched networks and circuit-switched networks. A typical NoC consists of computational processing elements (PEs), network interfaces (NIs), and routers.. The NoC architecture has two parts router and data link. The router can store and forward data and the data link can transmit signals from one router to its neighbor.[2]

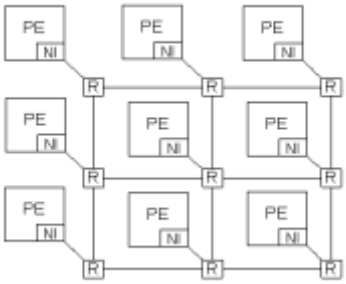


Fig:- Block Diagram of NoCArchitecture

This paper proposes the power efficiency of NoC (network on chip) is becoming a new research direction. They had proposed an innovative power-efficient architecture of input buffer of NoC, which makes use of the mentioned characteristics, it can improve the power efficiency of the NoC of tiled CMP significantly. As an important part of a tiled CMP, the NoC

architecture is composed with two parts: router and data link. The router is a module which can store and forward data, and the data link can transmit signals from one router to its neighbor. Since the energy consumption of an operation depends on the data of current cycle as well as its continuously previous cycle, They used the data transition as the independent variable for precision. The digital signals transmitted on NoC are occurred by cache coherence protocol . [1]

B.NoCRouter architecture

The NoC router architecture consist of three bolck Arbiter, buffer, crossbar. The input buffer stores the input data temporarily, The arbiter receives requests from input buffers and allocates virtual channels to requests and then gives grant signals to request initiators. The crossbar switches granted input requests and forwards the request data to data link, and then the request data is transmitted to the next hop router through data link .In this paper, A NoC Router if more than one input is request for

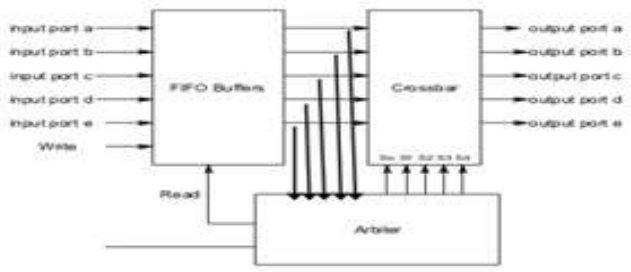


Fig:- Block Diagram ofNoC Router

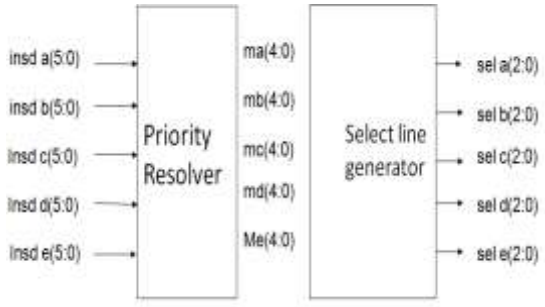
the same output the arbiter is used. Here we are explaining the behavior of Round Robin Arbiter in NoC Architecture. The Round Robin Arbiteroperates on the principle that a request which was just served should have a lowest priority on the next round of arbitration. It keeps the updated status of all the ports and knows which ports are free and which ports are communicating with each other. Packets with the same priority and destined for the same output port are scheduled with a Round-Robin Arbiter. In the Round Robin Arbitration scheme, which may be granted that all input request are treated fairly. Hence they had proposed arbiter is suitable for NoC design.[2]

C. Arbitration Techniques

A NOC, which is capable of supporting different classes of service levels such as best effort and guaranteed traffic, needs to support an arbitration mechanism. This arbitration mechanism schedules a flit for transmission on the output path. There are various arbitration mechanisms such as RR (Round Robin),Matrix Arbiter. In this NoC router fixed priority arbitration techniques is used.They are two techniques of arbitration one is fixed priority & another is Dynamic priority .In the fixed priority the priority of input port is fixed & it will assign the signal having highest priority that is fixed .The next signal have different priority.[5]

D. Matrix Arbiter

In Matrix arbitration scheme when all input port are requesting for same output port then Matrix arbiter first trap source and destination address from buffer and forms the Matrix . The Matrix arbiter uses same algorithm as that of Round Robin Arbitration Algorithm. In case Matrix Arbiter Priorities of input packet to transfer the packet from source to destination are arranged in rotation among source address in the Matrix form. Hence Matrix arbiter is basically based on rotation priority to avoid the drawback of fixed priority based Round Robin Arbiter.



In this paper,they have focused Design Matrix Arbiter for NoC architecture . In the matrix arbitration when all input packet have the same priority request for same output port then matrix arbiter generate the matrix depending upon input and this case the destination address is not same so every input port getting a priority so they have to transfer data from source to destination. When all input port are request for same output port in this situation matrix arbiter first form a matrix 5*5. After that matrix arbiter assign the Priority to all input request and generate the grant signal. In this paper they are analyze the Area, power. In the matrix arbiter the input request is granted according to priority matrix. the round robin arbiter use less resources as compared to matrix arbiter & the matrix arbiter consume more resources because of that it uses maximum clock frequency. The matrix arbiter has higher throughput and more computational speed. As the number of input increase power consumption increases.

III. WORK ON DSIGN DYNAMIC PRIORITY DYNAMIC PRIORITY BASED MATRIX ARBITER

Dynamic priority based Matrix Arbiter: It operates on the principle that input ports are request for output ports are send request it check source as well as destination address it will make all input request equilibrium then it.

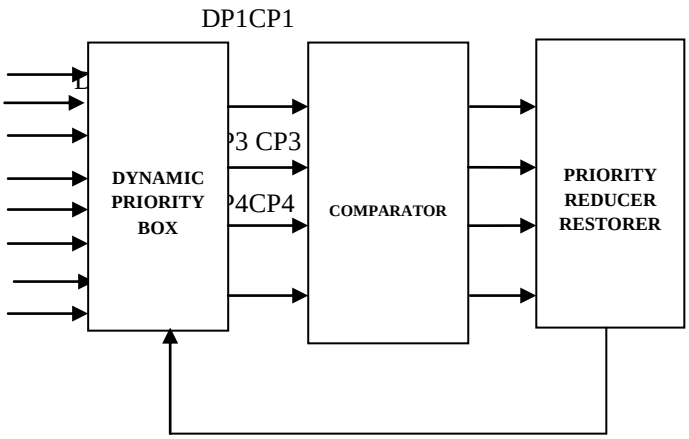


Fig:-1.The Block Diagram proposed arbiter architecture for dynamic priority based Matrix arbiter

In the dynamic priority based matrix arbiter the block diagram shows that first block that is dynamic priority box provides dynamic priority it will transfer three signals first is request second is priority and third is grant signal .In the dynamic priority based matrix arbiter sends requests to all 4 priority then it will check the highest priority if the 3 position priority is high then it will show the grant signal as a 0010 and then it will done up to last position. The second block is comparator compares request signal and priority signal it provides CP1 ,CP2, CP3,CP4 it will goes to the next block priority reducer router which gives the results of both Priority signal & Request signal .In this way it shows that if we are sending request the matrix arbiter shows the it will form matrix traps the source and destination address for providing the input to the router. In the dynamic based matrix arbiter it will proves that if apply the 4 request it will generate the same clock pulse for it.

IV .SIMULATION TOOLS

Xilinx ISE 13.2i

The language used for the coding of arbiter is VHDL in which behavioral and structural style of modeling is used. For simulation and synthesis purpose Xilinx ISE 13.2i version is used. RTL view & synthesis report can be easily obtained in this software. In addition, power calculations can be done using XPower menu in this tool. for the number of gates counts are calculated with help of summery report which is generated after simulation .In this ISE 13.2i the report are generated for different parameter .For calculating delay check the synthesis report which gives the time period of transmitted port.

V. SIMULATION RESULT

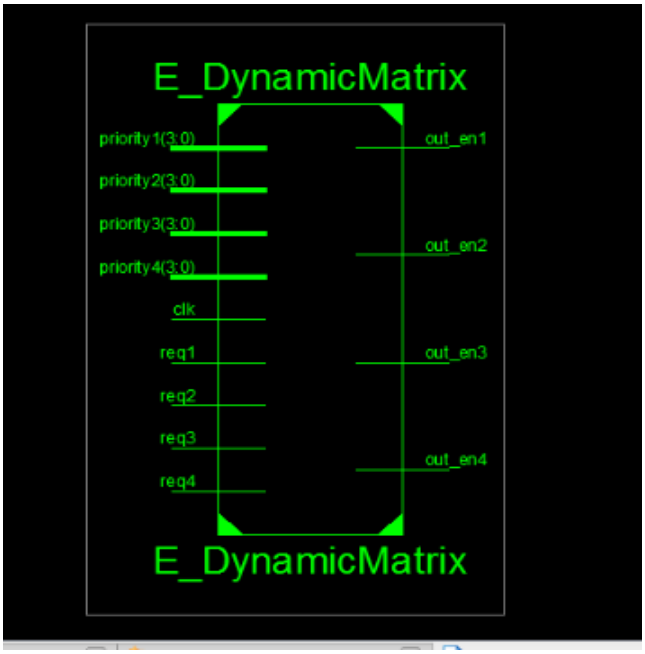


Fig.2:- Schematic Diagram

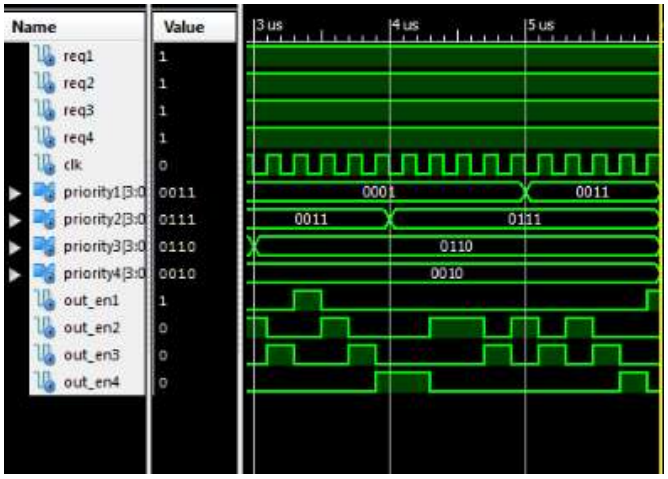


Fig:-3. Output waveform of dynamic priority based Matrix arbiter

TABLE:-1
SIMULATION PARAMETER TABLE

Parameter	Result
Power Consumption	0.10mwatt
Delay	4.04ns

The dynamic priority based Matrix arbiter gives power consumption of about 0.10mwatt also the delay of 4.04ns along with area gate count.

IV.CONCLUSION

In this paper we studied dynamic priority based matrix arbiter in this arbiter it forms the matrix which consist of request signal, grant signal, and priority signal. Which gives output in rotation form. In the dynamic priority based NoC router gives low Power consumption along with the gate counts and also reduced in delay.

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