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Test length Optimization of 3D Stacked ICS Using Multi-Visit TAMS

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***Abstract* :** 2.5-D stacked ICs (2.5D-SICs) consist of multiple active dies (or 3D towers of active dies), which are placed side-by -side on top of and interconnected through a passive silicon interposer base which contains through silicon vias (TSVs). A known presented post-bond test and design for-test (DFT) strategy for such 2.5D-SICs put a Test Access mechanism (TAM) for interposer and micro–bump testing. It gives heterogeneous integration higher performance, bandwidth and lower power consumption. However, testing of 2.5D SOC is considered as one of the important dare and hence logical test techniques are needed. The objective of this paper is to design efficient test access mechanism (TAM) and test scheduling architecture of different dies of the SOC with different condition like power and TSV such that the overall test time of that SOC is reduced, here in this paper we extend that begin with the concept of Multi- visit TAMs, that's mean parallel TAM which allow to visit the same die more than once, for minimal additional hardware cost. The multi – visit TAMS also help in identifying a valid parallel TAM and achieve significantly lower test lengths. In this work, we have proposed heuristic approaches. Experimental results are presented for several ITC02 benchmark SOCs which show promising results for different TAM width.

IndexTerms*–*TAM(Test Acces Mechanism),DFT(Design for Testability) ,active Dies

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I. INTRODUCTION

1.1 2.5 D system -on -chip (2.5-D SOC

Recent advancement in semiconductor technology enables the manufacturing of integrated circuits with TSV is a conducting nail, made up of copper or tungsten that provides electrical connection. Mainly TSVs are used to create vertical inter die connection through the substrate of a thinned–down silicon wafer to its back side that provide higher density and performance at lower power dissipation. TSVs typically made of copper or tungsten. There is electrical path from front-side to back side of thinned-down silicon wafer inter-connection of vertically stacked dies [9]. Typical TSVs have a depth of 50 micro meters, diameter 5 micro meter height: 50 micro meters min. pitch: 10 micro meter. It give following advantage over wire bond such as high density, low capacitance, which results improved band-width, performance, power dissipation. It gives the opportunity of die stacking.

Compared to the 2D design, the 3D SOCs poses great challenges in testing[13]. Extremely limited test resources in such as pin count, TSVs density and routing area are shared among more and more in three dimensional planer specially, the pins are only located at the bottom tier and the test access to the upper tiers. TSVs are used for three –dimensional integration so – it is called 3D stacked ICs (3D-SICs), these are vertical die stacks that offer a small foot –print and form-factor[16], it is mainly useful for hand held and portable application. TSVs are also used in so-called "2.5D-SICs", in which multiple active dies are placed side-by-side on top of an interconnected through a passive silicon interposer base which contains TSVs. 2.5D-SICs not reduce the footprint, but offer better cooling options for high – performance and communication application[18].

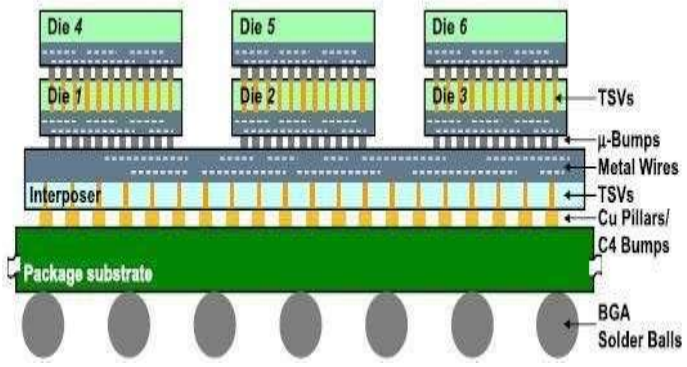

Fig1: 3D- IC containing passive silicon interposer base

Fig1 depicts a typical 2.5D-SICs, in which multiple active dies are stacked face–down on top of an interposer base, connected through fine pith micro bumps. The testing times are optimal only for the TAM given TAM widths. Lower the testing times can be achieved if an optimal TAM width partition is chosen which evolve into 3D towers of die stacking. The goal of this project work is to reduce the test length by using multi-visit TAM, the objective of multi visit TAM concept are, for given interposer designs, to achieve a higher success rate by finding a valid TAM architecture and to reduce the resulting test length by using wider TAMs. Compared to the 2D designs, the 2.5D-SOC poses great challenges in testing[15]. Extremely limited test resources such as pin count, TSVs density, and routing area shared among more and more cores in three dimensional placements. Specially, the pins are only located

at the bottom tier, and the test access to the upper tiers are through the TSVs. Thermal management becomes even more critical due to the increased power density and the non-uniform distribution of power density in 3D. It's a key design issue to prevent chip-wide overheating during the test mode. The spatial and temporal non-uniform thermal behaviour of the cores during testing should be properly modelled and utilized during concurrent test scheduling. As the cores are deeply embedded and spread among multiple tiers, the three dimensional test access architecture faces a more complex and comprehensive configuration environment [17]. A very limited work has been carried out on the above mentioned problems of 3D SOCs. This motivates our work for designing an efficient test infrastructure considering various constraints.

1.2 Objective

Here we generalize the concept of one-visit TAMs to multi-visit TAMs, which allow TAMs to visit to visit the same dies multiple times. One of these visits is used to test that die itself; The other visits are merely transit-only visits, which are used to enable connections to other dies that otherwise would remain unreachable through existing functional interposer connections**.** The objectives of the multi- visit TAMs concept are, for given interposer design, to achieve a higher success rate for finding a valid TAMs architecture and to reduce the resulting test length by being able to identify wider TAMs. Here multi-visit TAMs architecture is a generalization of the hybrid TAMs architecture. Hence there are a number of TAMs which all start and end at port 0, and each TAMs contains a number of active dies such that each dies is included in exactly one TAMs. This implies that for a multi–visit the TAMs containing k dies .Each die can be visited at most k times. Due to this missing interposer connection, the distribution, daisy-chain, Cannot succeed in constructing valid TAMs, the multi-visit TAM architecture in the novel multi- TAMs scheme are indicated. In case, consist of a single TAMs Which starts at port 0. The objective of this work is to design an efficient test scheduling architecture to reduce the overall test time of SOC considering the maximum available TAMs width. In this work, heuristic approaches has been for test architecture design and test time optimization problem of 2.5D SOC. Experimental results show the effectiveness of the proposed methods compared to already proposed 2.5D test architecture and scheduling optimization methods.

II. LITERATURE SURVEY

Diagrams of the test difficulties of 3D-SICs were displayed in [1–3]: they relate to test streams, test substance, and test access. Test cost models should be defined that improve test streams for greatest viability and least cost [4,5]. New blame models and comparing tests are required for 3D-particular deformities, particularly for the ones identified with the TSVs-based entomb interfaces [2, 3, 6]. Pre-bond wafer testing is a noteworthy test because of the various little, fine-pitched, and harm delicate smaller scale knocks, TSV tips, and cushions [7,8]. Essentially, there are likewise challenges identified with testing and treatment of non-planar bite the dust to-wafer stacks [19]. The outlines of DFT designs that traverse over different kicks the bucket require consideration [1,11]. To the best of our insight, no papers have tended to the particular issue of testing 2.5D-SICs or 3D-SICs containing an aloof silicon interposer base. Marinissen et al. [10, 11] proposed a test access engineering that backings both pre-bond and post-bond testing of 3D-SICs. The design comprises of pass on level wrappers which give test controllability and watch capacity on all practical I/O of the pass on. The wrapper has both a solitary piece ('serial') TAMs for test guidelines and low-transfer speed test information and in addition adaptable, multi-bit ('parallel') TAMs for high-transmission capacity test information. Amid pre-bond testing, the kick the bucket is examined on its TAMs small scale knocks, or (if pore innovation can't deal with the fine-pitch miniaturized scale knock) devoted test cushions. Amid post-security testing, test access is on the base pass on, while the wrappers of the different bites the dust in the stack coordinate to lift test guidelines and information up to the circuit-under-test and withdraw. As [24] portrayed, the pass on wrapper.

1500 both with some specific 3D extensions. In either case the external I/Os are at the bottom die equipped with an IEEE 1149.1 interface to support board-level interconnect testing. In order to incur as few extra test pins as possible, the stack's serial TAMs is multiplexed onto the IEEE1149.1 pins, whereas, the parallel TAM is multiplexed onto functional I/Os. [10, 11] assumed the 3D- SIC only contains a single "tower", i.e., each stack level contains exactly one die. Chi et al. extended this DFT architecture to support multiple "towers" on a single base die. We will use the 3D test access architecture from [10, 11, and 14] also in this paper. However, the approach from [14] requires active DFT circuitry (flip-flops, multiplexers, and logic gates) at each tier, which in the case of passive silicon interposer is impossible Chi et al propose a post–DFT architecture for 2.5D-SICs.This architecture contains DFT elements both in the active dies as well as in the passive interposer[21]. The active dies stacked on top of the passive interposer base are equipped with 3D –enhanced die–level test wrappers, which can be based on either IEEE STD 1149.1or IEEE STD 1500. These die –level wrappers implement both a single – bit („serial") TAMs for test instruction and low bandwidth test data, as well as a scalable, multi –bit (parallel) TAMs for high – band-with test data. Specific 3D features include (1) test turns, (2) test elevators to transport test data up and down in the stack and optional pre-bond probe pads.

At the bottom side of each active die, the I/O to interposer port passes through a regular IEEE1149.1 wrap. The DFT in the passive interposer is by definition limited to additional interconnects only[20].All interposer ports are extended with a four –pin highlights the DFT or the ex 2.5D-SICs introduced. The serial TAMs is able to perform interconnect testing of micro –bumps and interposer, as well as basic low –band width die testing. Core wrapper design, TAMs design and test scheduling have been very active areas of planar SOC testing research. Goal et Al presented a genetic algorithms based heuristic for optimal wire allocation and core assignment with test –rail/test- bus based TAMs. A wrapper/ TAM co-optimization, method was described in

for efficient test planning. A graph theoretical approach for power constrained test scheduling was also discussed [5].
YU et. Al proposed a TAM/wrapper co-design methodology that targets both test time minimization and prevention of hot spots. These are very limited work on 3D SOC testing. The first work on TAMs design for 3D-SOC was presented in an integer linear programming (ILP) model was designed to divide the total TAMs wires into several test buses with fixed width and to assign modular cores to test buses so as to minimize the overall test time under the constraints of TSV count utilized by TAMs. A number of test –access architecture and TAMs optimization methods have been proposed in the literatures wue et al. have proposed several 3Dchain design techniques [10], a recently developed TAMs optimization technique does not impose any limits on the number of TSVs used for theTAM but consider pre-bond test consideration and wire lengths limits. Recently a test–access mechanism (TAM) optimization technique was proposed in to minimize the testing time of 3D SOCs, under limits on the number of TSVs utilized by TAMs. The same TAMs that traverse multiple layers in post– bond testing are fully reused for pre-bond tests. Consequently, TAMs can be divided into multiple parts and distributed among the different silicon layers[22]. As all the TAMs segments in a particular silicon layer need to be probed during pre-bond testing, a required for that Silicon dies that contains many TAM segments[23].

1 Parallel TAM Optimization

et al. [14] proposed a post-bond DFT architecture for 2.5D-SICs, which we also adopt in this paper. This architecture contains DFT elements both in the active dies as well as in the passive interposer. Chi et al. also proposed search algorithms that attempt to enhance the basis DFT architect reduce the overall test length for the active dies by identifying functional interposer interconnects that can be reused as parallel TAMs. Here three TAMs configuration distinguishes. The distribution, daisy-chain and hybrid architecture. In the distribution architecture, Each active dies (or 3D tower) has its own private TAM. This architecture can only be constructed if w0i > 0and wi0 > 0for all ports.$1 \leq i \leq k$. The various TAMs can operate in parallel and the overall test length is deter-mind by the die with the longest test length. In the daisy-chain architecture has TAM, which moves from port 0, via all active dies(or 3D towers),and then back to port 0. The active dies can be daisy-chained in any order Which allow freedom in constructing the daisy-chain architecture out of functional interposer connections a daisy-chain TAM supports both sequential and parallel test schedules. In a sequential test schedule, one die is tested at a time, while other dies bypassed using the one bit bypass register of the die wrapper. But in parallel test schedule, all dies are tested simultaneously with their scan chains concatenated. In the hybrid architecture is a generalization of distribution and daisy-chain architecture .in the hybrid architecture, there are a number of daisy-chain TAMs. Each daisy-chain TAM contains a number of active dies such that each die is included in exactly one TAM. Different TAMs can operate in parallel, while each individual TAM supports both sequential and parallel test schedules; The search algorithms defined in try to identify a TAM configuration which best minimize the overall 2.5D –SICs test length. Their keys performance parameters are success and test length, the success and test length obviously depend on the functional interposer connection. The search algorithms defined in [14] try to identify a TAM configuration which best minimizes the overall 2.5D-SIC test length. Their key performance parameters are *success* and *test length*, where "success" is defined as achieving a TAM wider than one wire (as we already have the serial TAM provided by the IEEE1149.1 DFT). Success and test length obviously depend on the functional interposer connections.

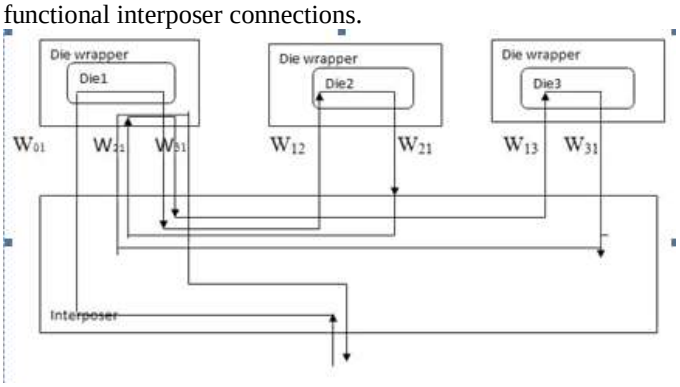

Fig2: The functional interposer model

Multi-visit Parallel TAM Optimization

An algorithm that identifies Multi-Visit TAM configuration that achieves the shortest test length. The inputs for the algorithm include a matrix containing the interconnect specification of the interposer in question and *a test-length lookup table* which provides the test lengths of each die for a range of TAM widths. The proposed algorithm consists of two steps. The first step generates all possible partitions for k dies.
In the second step, for each partition we identify the best possible (One- or Multi-Visit) Daisy-chain TAM for each group of dies in that partition. A better Daisy-chain TAM is defined as a TAM of wider width, or, in case of equal width, of less re-visits. A wider TAM implies equal or smaller test length, which is our main optimization criterion. Every re-visit implies more area in the wrapper of the re- visited die, which is our second optimization criterion. Step 1 can be accomplished by straightforward enumeration..

The tree for the One-Visit Daisy-chain TAM described above can be extended to represent the Multi- Visit Daisy-chain TAM. Part of the resulting tree is shown in Figure. This figure indicates that the complexity of the Multi-Visit tree is much higher than that of the One-Visit tree. Multi-Visit TAMs have different TAM lengths depending on the number of re-visits use.

III. Heuristic Approaches for Optimizing the Overall Test Time of 2.5-D SOC

The proposed algorithm consists of two steps. The first step generates all possible partition for k dies. In the second steps, for each partition we identify the best possible (one or multi-

visit) daisy-chain TAM for each group of dies in that partition. A better daisy-chain TAM is defined as a TAM of wider width. A wider TAM implies equal or smaller test length, which is our main optimization criterion.

3.1 Problem formulation

The objective of this work is to generate an efficient way of designing a test schedule with optimized testing time by considering the maximum available TAM width.

The problem can be formulated as follows:

Given a three dimensional SOC with

i).N number of dies,

ii).Total TAM width limit (TAM max),

iii).Inter connect specification of the interposer

iv).Test length lookup table which provides the test length of each die for a range of TAM width.

3.2 Proposed Algorithm

A method has been proposed regarding the above mentioned problem, algorithm based on heuristic approach, below is description of proposed algorithm.

Here algorithm tries to reduce the test time of dies for available TAM Width (Wmax). Here in this algorithm we explored the entire possible path for accessing the available dies. These paths are the different way of connection between the dies. If the no. of dies are more than available maximum TAM Width (Wmax) then same TAM Width (Wmax) is assigned along all the dies of the path and added serially in which the test time of all the dies for the give TAM Width (Wmax) is added, but if no. of dies is less than given TAM Width(Wmax) than randomly distributed the TAM Width among all the path of the dies and record the maximum test time along each path and from maximum test time the algorithm select the minimum test time. In this way the path corresponding to which the minimum test time is obtained, is the best test time for the given TAM Width

Algorithm.[Multi-visit OPTS (D, W, P; Test length look up table)]

1. Let D be the set of Dies,{d1,d2……dn};
2. Let W be the TAM width;
3. Let p be the set of all possible path of the N Dies (p1,p2,p3……Pn);
4. Initialize the maximum TAM width;
5. For each path Pi in p
6. {
7. Tj:=calculate test length (TAM width ,test length look up table);

/*Tj is the test time of the path*/

8. If Tw < N
9. Then assign equal TAM width to all the die;
10. Else
11. Then randomly distribute the TAM width to the entire path;
12. Record the maximum test time ;
13. Finally take out the minimum test time.
14. End

Fig 3:Algorithm for Multi-Visit Path

Table 1: Example

Dies	TAM width	Testing time
1	1	3023
2	2	3175
3	3	2507
4	4	2070
5	5	1774
6	6	1624
7	7	1405
8	8	1257
9	9	1182
10	10	1107

Here we assume 3 dies and also we have taken the maximum available TAM width (Wmax) is 16 and the test time of these dies with respect to different TAM width are shown in table1. At first we explore all the possible path with respect to available dies, here dies are 3 so possible path is 6.

So here 6 different path is explored. now on all available path TAM width is distributed randomly, for example, path[1] 1,2,3 path[2] 1,3,2 path [3] 3,2,1 path[4] 2,3,1 path[5] 2,1,3 path[6] 3,1,2. now on each path we distribute the TAM width 16 randomly. For example on path [1] random distribution of 16 is{8},{4},{4},test time is(3023),(3175),(5746) clock cycles on corresponding TAM width, obtained test time is [5746] clock cycle ,now for next path[2], TAM width distributed corresponding to this path is {4},{8},{4},test time is [116],[2507],[3175] clock cycle, obtained test time is [3175] clock cycle, now for path [3] distribution is {5},{9},{2},test time corresponding to this TAM width is [103],[1405],[2582] clock cycle, obtained test time is [2582] clock cycles, again now for path [4]{2},{3},{1} and test time is [3157]. and test time is [3175],[2507],[3023] clock cycles, obtained test time is {3175}. Now algorithm will assign TAM width 16 to next path randomly and the entire procedure will again be performed in previous manner. Now from all test time we will take minimum test time and minimum test time is {2582} clock cycle. In this way we obtained the optimal test time to corresponding TAM width (Wmax).

IV. EXPERIMENTAL RESULT

The proposed algorithms are implemented using C programming language with Core i7 processor and 4 GB RAM. To demonstrate the effectiveness of the proposed algorithms, we use SOCs from ITC‟02 benchmarks namely d695 p22810, p93791, p34392 .Experimental result are presented in Table2-Table5.Experimental result shows the test time of different SOC for different TAM width (W_{max}) Table 2 describes the detail experimental result of SOC D695 in which for different TAM Width test time is recorded. TAM width goes on increasing and the corresponding test time is recorded in clock cycle. Tables contain two columns .First column contain the different value of TAM Width (Wmax) for which test time is calculated. As the TAM width is increased test time of the corresponding SOC goes on decreasing. The result obtained is very efficient. Similarly the other Table contains the different

TAM Width and the corresponding testing time for the given TAM Width for SOCs D695, P22810, P34392, and P93791.Test time is calculated using the proposed algorithm. The result optioned is optimal and efficient.

Table2: Experimental Results of SOC D695 for different TAM Width

D695	
TAM Width	Testing time (Clock cycles)
n=16	45841
n=24	32891
n=32	24163
n=40	19757
n=48	14983
n=56	12192
n=64	10869

Table 3: Experimental Results of SOC P22810 for different TAM Width

P22810	
TAM Width	Testing time (Clock cycles)
n=16	654972
n=24	606656
n=32	575004
n=40	347411
n=48	243791
n=56	191978
n=64	162595

Table 4: Experimental Results of SOC p93791 for different TAM Width

p93791	
TAM Width	Testing time (Clock cycles
n=16	1443358
n=24	777193`
n=32	767139
n=40	320754
n=48	320757
n=56	320757
n=64	320757

Table 5: Experimental Results of SOC p34392 for different TAM Width

P34392	
TAM Width	Testing time (Clock cycles
n=16	1843266
n=24	1255931
n=32	1207789
n=40	954863
n=48	800513
n=56	556930
n=64	457648

V. CONCLUSION AND FUTURE SCOPE

The DFT architecture also uses 3D improves die wrappers that permit for parallel TAMs of user-defined width, multiplexed onto functional connections. Exclusively intended search algorithms try to recognise as–wide-as possible set of functional interposer interconnects that can be reused as parallel TAMs to the many dies .Here we presented Multi-visit TAMs,i.e. parallel TAMs which are allowed to visit the same die more than once. At the cost of a minimal adaption of the die wrapper hardware, multi–visit TAMs offer more workability in recognizing TAMs in available interposer designs and hence achieve significantly higher success rates and lower test lengths. Even, the TAM optimization algorithm typically has the very suitable calculated time of less than second.

In this work thermal concerned testing and TSV constraints is not considered. In future we work will work on it.

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