International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169
Volume: 4 Issue: 4 326 - 330

Design and Simulation of High Speed, less area 64-Bit ALU using Efficient Technique

Prof. Rajendra M. Rewatkar*, Apurva V Khode, Ashwini S. Kalinkar, Padmaja S. Bangde, Shreya D. Potey

Asst.Professor, Dept. of Electronics Engineering,DMIETR, Wardha, India*

B.E. Students,Dept. of Electronics Engineering,DMIETR,Wardha,India

Abstract:- In this paper, Authors has been designed high speed, less area 64-bit Arithmetic and Logic Unit by efficient techniques using VHDL language. The optimization of the proposed design will be done by using the different techniques. The parameters speed and area of the design will be improved by using Carry Look Ahead Technique. It also reduces the circuit complexity.ALU is a fundamental building block of central processing unit of a computer which is used in the simplest microprocessors for purpose of maintaining timers.Previously many efficient architecture have been introduced for the design of low complexity operation, but we have given the attention to the carry look ahead technique. The proposed design of ALU will performs the mathematical, logical, and shifting operations in a computer. In this work, the efficient modules of ALU aredesigned using Xilinx software and simulation results are verified on same platform using test benches.

Keyword: *ALU, VHDL, EDVAC,DSP.*

*****

I. INTRODUCTION

Now a days, increasing demands of gadgets like laptop, tablets, PCs forcing technologies to develop high speed processor. The speed of any processor is mainly depending upon computational time needs to finish the task in ALU. Adder and multiplier is main fundamental block inside ALU on which speed is depended. The system can be made chipper, more efficient and more flexible by reducing the number of adder and multiplier in the circuitry. It is a basic building block of any microprocessor along with DSP Processor that accomplishesmany arithmetic functions grounded upon the control input selection. Thedifferent functions of ALU are collocates with the help of set of fundamental units.All rest of the elements of computer system such as control unit, register, memory, I/O are mainly responsible to bring data into the ALU for process and then to take results back out.ALU is a combinational type of circuit. The ALU takes as input the operand and a code from the control unitwhich indicatesthe operation to be performed. The output is theresult of the computation which we are realizing. The VHDL software interface used in this design reduces the complexity and also provides a graphic presentation of the system.This software not only compiles the given VHDL code but also generates waveform results

II. DESIGN METHODOLOGY:

In the present work, Authors have designed the basic module for 64 bit ALU using simple full adder entity. This basic module performed various arithmetic and logical operations. Also, the simulation waveform is observed and the design is verified by using test benches. Similarly, the efficient module of the 64 bit ALU has been design using carry look ahead techniques. It provides efficient way for high speed, less area 64 bit ALU at the architectural level. The basic ALU consist of full adder techniques which uses more numbers of adders as well as gates results into increased delay and due to this there is occupation of more area which ultimately increasing the power dissipation.

To make proposed system efficient, we have use the technique consisting of relatively less number of adders which minimizes delay and occupied less area.So the system becomes more faster than the basic one.The requirement of adders is minimized, results into the minimization of gates. Hence, the system will occupy less area.

 ISSN: 2321-8169
326 - 330

The carry-look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits.Carry look ahead depends on two things, first is Calculation for each digit position whether that position is going to propagate a carry if one comes in from the right. Second is combining these calculated values to be able to deduce quickly for each group of digits, that group is going to propagate a carry that comes from the right. In this efficient design we have introduced adders using carry look ahead technique, we have done subtraction using adders and 2's complement. we have designed 64-bit shift register, 64-bit multiplier. 64-bit shift register is design to perform shifting operations which are generally used in multiplication,division which also function as the delay circuits and digital pulse extender. It is found in calculators, computers and data processing system.

Different operation controlled by respective mode select bit is depicted in the table1:

Mode Select S3	S2	S1	S0	Cin	Result	Operation
0	0	0	0	0	A+B	Addition
0	0	0	0	1	A+B+1	Addition with carry
0	0	0	1	0	A-B	Subtraction
0	0	0	1	1	A+B+1	Subtraction with borrow
0	0	1	0	0	A+1	Increment
0	0	1	0	1	A-1	Decrement
0	0	1	1	0	A/2	Right Shift
0	0	1	1	1	A*2	Left Shift
0	1	0	0	0	NOT A	Compliment
1	1	0	0	1	A.B	AND
1	1	0	1	0	A+B	OR
1	1	0	1	1	A XOR B	EX-OR
1	1	1	0	0	A XNOR B	EX-NOR
1	1	1	0	1	A NAND B	NAND
1	1	1	1	0	A NOR B	NOR
1	1	1	1	1	2's Compliment of A	2's Compliment

The figure 2 has shown the block schematic of 64 bit ALU. In this, total 4 select lines are connected to the design. Select input S_3 bit will decide the working of logical and arithmetic blocks. If it is 0 then arithmetic operations are performed and 1 then logical operation is performed.

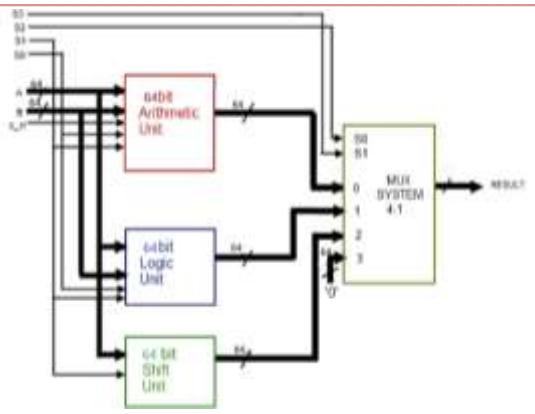


Figure 2: Block Schematic of 64-bit ALU

The circuit diagram of the 64 bit ALU is depicted as below,

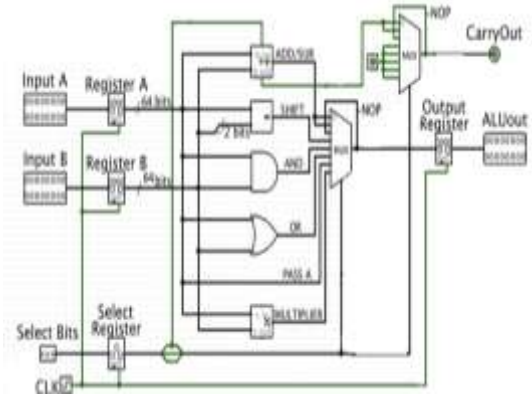


Figure 3 Circuit diagram of 64 bit ALU

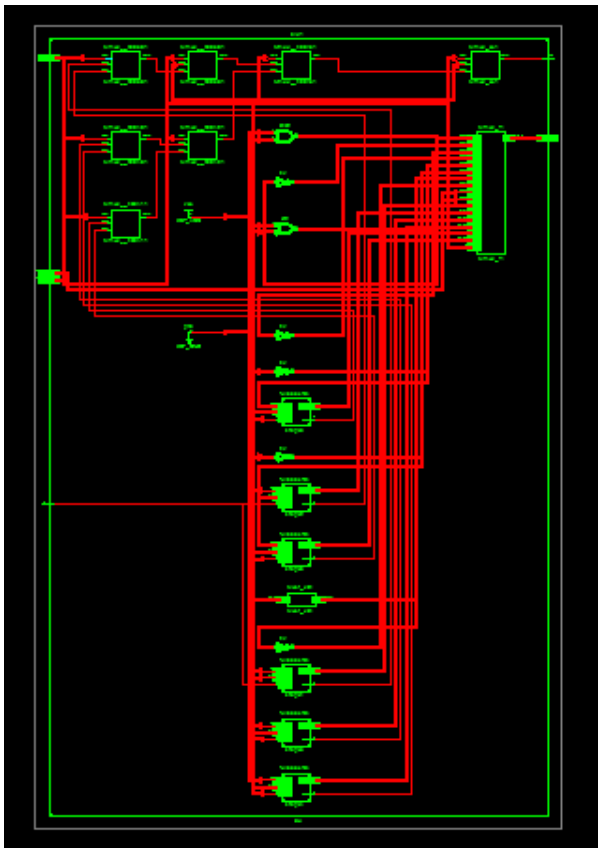
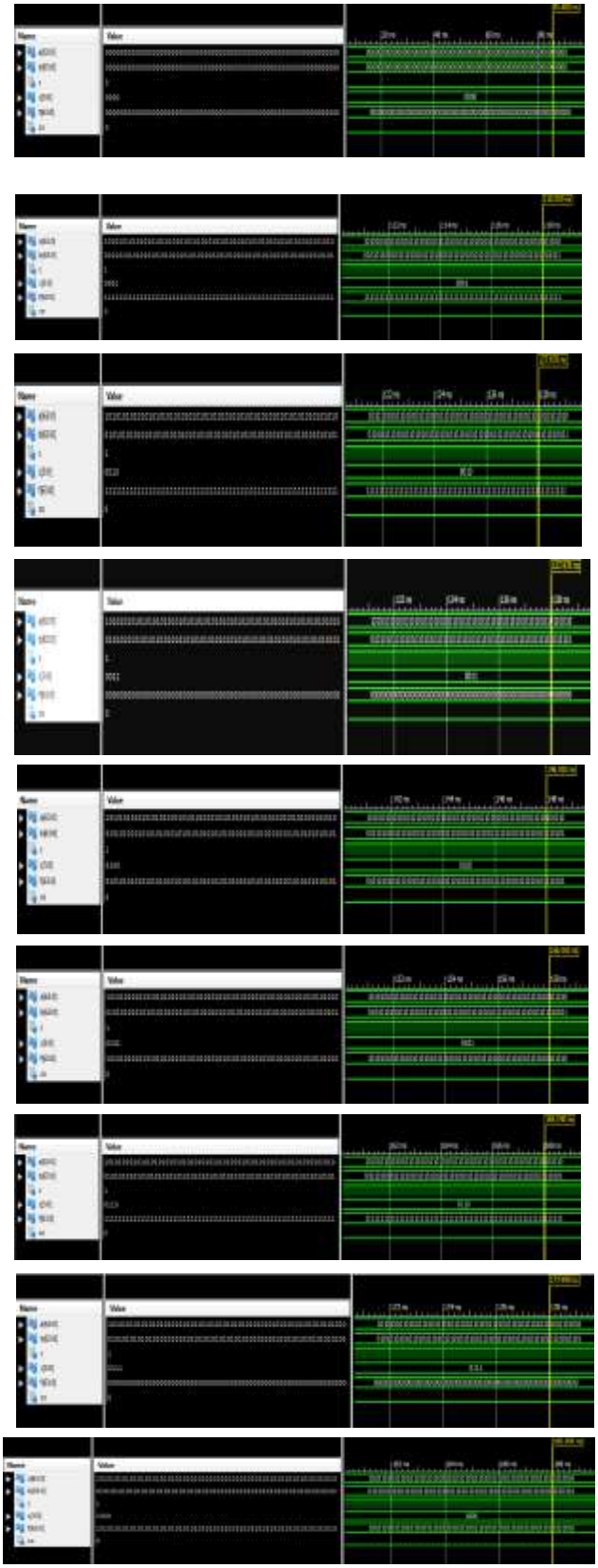


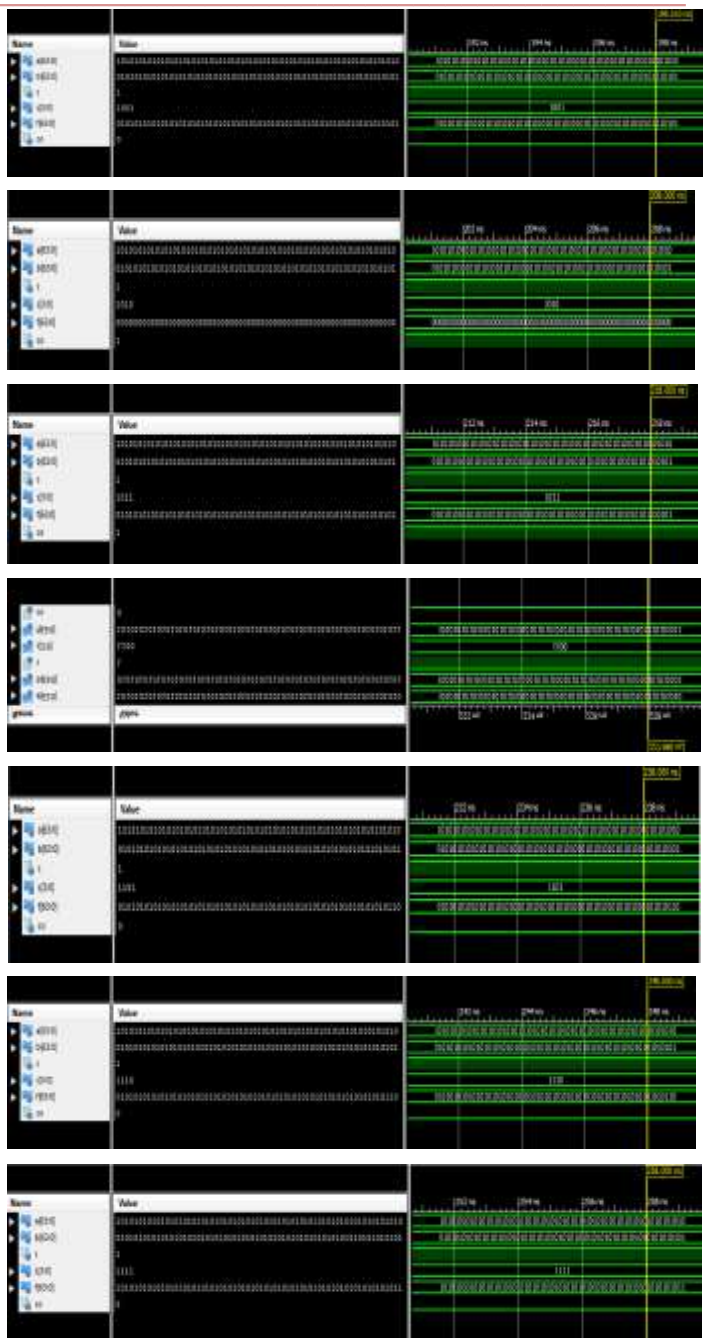
Figure 4: RTL view of 64-bit alu

ISSN: 2321-8169
326 - 330

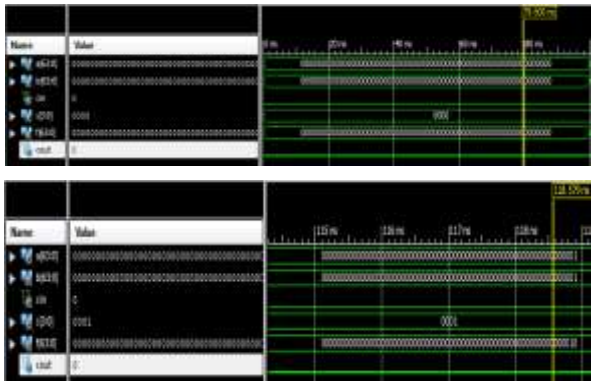
III. SIMULATION AND RESULTS

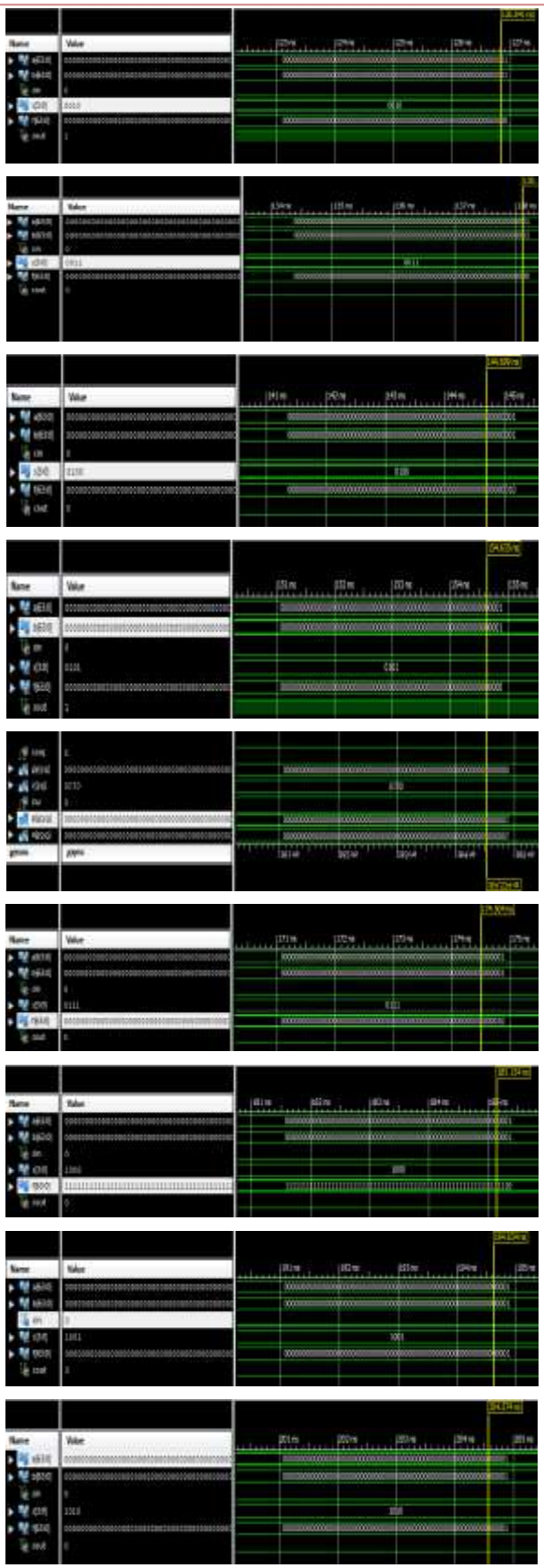
The design waveform of the Basic module of 64 bit ALU is depicted as below

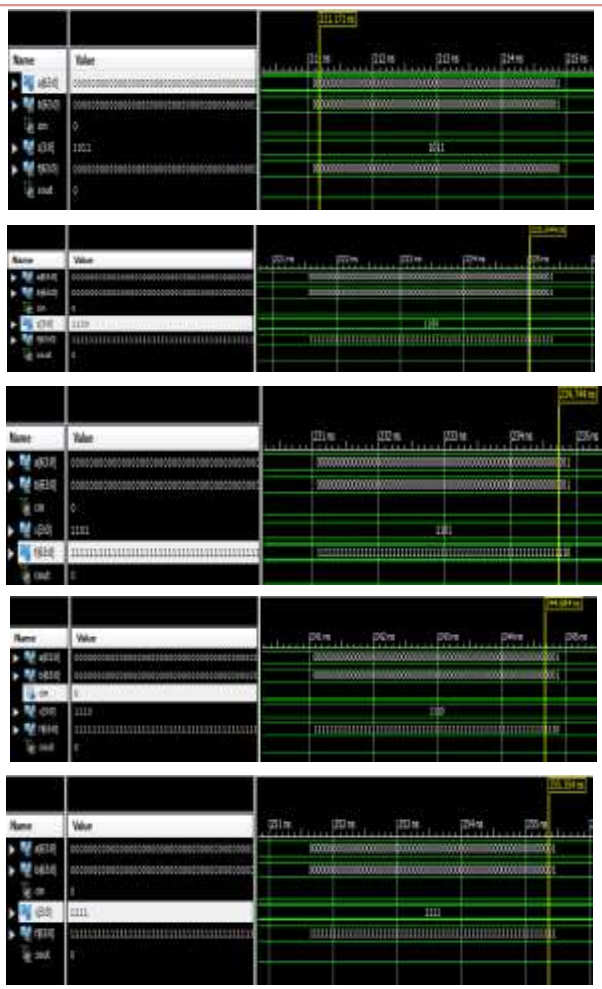




The design waveform of the 64 bit carry look ahead is depicted as below:







III. CONCLUSION:

The efficient module of the ALU has been presented. Initially, the basic module of the 64 bit ALU is designed and the simulation results are verified for the arithmetic and logical operations. Then, The64 bit ALU is designed using carry look ahead approach which increases the speed to a great extent but the hardware complexity increases. The proposed methodology provides a systematic way to derive high speed system with very less area. Also, Author efforts are directed towards implementation of 64 bit ALU design with different circuit topology and optimization.

REFERENCES:

[1] Suchita Kamble, Prof .N. N. Mahler "VHDL Implementation of 8-Bit ALU"IOSR Journal of Electronics and Communication Engineering ,ISSN : 2278-2834 Volume 1, Issue 1, May-June 2012.

[2] Ankit Mitra- "Design and implementation of low power 16 bit ALU with clock gating" International Journal of Advanced Research in Computer Engineering & Technology,Volume 2, Issue 6, June 2013 ISSN: 2278 – 1323

[3] Geetanjali, Nishant Tripathi "VHDL implementation of 32 bit arithmetic logic unit" International Journal of Computer Science and Communication Engineering, 2012.

[4] P Bhanusree, G Bhargav Sai, Y Ashwanth Kumar, K Sravan Kumar"VHDL Implementation Of 64-bit ALU"IOSR Journal of Electronics and Communication Engineering ISSN: 2278-2834, ISSN: 2278-8735. Volume 7, Issue 4, Sep. - Oct. 2013.

[5] Jagannath Samanta, Mousam Halder, Bishnu Prasad De "Performance Analysis of High Speed Low Power Carry Look-Ahead Adder Using Different Logic Styles" International Journal of Soft Computing and Engineering ISSN: 2231-2307, Volume-2, Issue-6, Jan-2013

[6] Daljit Kaur, Ana Monga- "Performance Analysis of 64-Bit Carry Look Ahead Adder" International Journal of Computer Science and Information Technologies ISSN: 0975-9646 Volume 5(1), 2014, 689-693.

[7] Pranali Thakre, Dr. Sanjay Dorle, Prof. Vipin Bhure:- "Low power 64 bit multiplier design by Vedic mathematics" International journal of application or innovation in Engineering and management ,Volume 3, Issue 4, April 2014 ISSN: 2319-4847.

[8] Rag had Z. Tawfiq:- "Xilinx FPGA implementation of arithmetic logic shift unit"- IJCCCE, Volume 6, No. 3, 2006.