Design and Implementation of Reconfigurable Bus Protocol Translator/Convertor using FPGA

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***Abstract*—**In systems involving multiple peripherals with diverse bus protocols it is desirable to have a versatile reconfigurable hardware platform to translate/convert a specific protocol to minimize the complexity of system design. Especially when the number of peripherals and devices are large, it is very much mandatory to have such a hardware to deal with diverse communication protocols. These requirements give rise to the need for an reconfigurable system which can act as a bridge between two devices following different communication protocols. Communication protocols such as I2C, SPI,USB and UART protocols are commonly used protocols in hardware design. In this work, such a versatile hardware solution is proposed which would translate a basic UART protocol to I2C,SPI or USB, depending upon the communication requirement. Such a system will eliminate the complexities of protocol management to the designer and it allows them to focus on application design and development. A customized hardware is designed using Altera Cyclone-II FPGA core and the protocol bridge is tested for multiple hardware engines.

Keywords- *UART, SPI, I2C,USB,VHDL and FPGA*

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I. INTRODUCTION

Protocol conversion is introduced to enable communication between two devices that follow different communication protocols by dynamically converting one protocol to another at runtime. For establishing communication between a host controller with a SPI or I2C device, first the UART protocol of the host has to be translated to SPI or I2C protocol since the host controller support only UART protocol [1]. Though commercially available protocol converts are available for this purpose, the proposed work would give a all-in-one solution for the same. To implement this protocol converter, a reconfigurable hardware like FPGA/CPLD are used. These are general purpose reprogrammable semiconductor devices, which can be used for implementing complex designs and functions [2].FPGA is composed of matrix of configurable logic block (CLB) connected through programmable interconnect, memory module and clock management. It is opposed to ASIC which is designed for particular application. FPGAs have SRAM based architecture so it can be reconfigurable multiple times. The main advantage of FPGA includes minimal development time and cost. Very High Speed Integrated Circuit Hardware Description Language (VHDL) is used for programming the FPGA. The commonly used serial protocols are UART, SPI,USB and I2C [3]. The main advantage of serial communication it can be performed with minimal pins. Peripherals such as ADC, DAC, EEPROM are uses serial communication to achieve small form factor. Design of a general purpose such a hardware will allow the designer to focus on the application instead of focusing g on protocol details of the peripheral.

Several serial protocols have been implemented on FPGA for the effective serial data communication. This section explains about existing work related to serial protocol. Design of I2C bus controller for interfacing FPGA with EEPROM is showcased in [7]. A serial data converter converts analog voltage from sensor to digital and then saves the digital data into EEPROM using I2C protocol. Designing I2C based system is represented in [8] where interfacing a microcontroller with DS1307 through I2C protocol is done. But the work does not show any protocol conversion. Implementing a new smart bus translator to convert standard protocol of one device to protocol of other device is shown in [9]. It reduces the complexity of the device when that device has multiple protocols and also reduces time to develop the firmware different protocol devices. Design and implementation of SPI protocol used for a SOC chip is done in [10]. The scope of this work is limited to communicate SOC chip with processor via SPI protocol. SPI implementation with BIST on FPGA is shown in [11] where an FPGA is used as a master and EEPROM as a slave for the SPI protocol. Most of the existing work is limited to achieve single protocol needed for application specific requirements. There is no solution available for a generic protocol conversion. In this work, a generic hardware is designed to address this problem. The sections of this work are organized as follows: Section III demonstrates the proposed design, Section IV depicts the hardware design, Section V explains the Simulation results, Section VI explains about Conclusion and Future scope.

II. PROPOSED DESIGN

The proposed protocol converter is designed with UART, SPI,USB and I2C protocol. This can convert UART into SPI, USB and I2C protocol. Figure 1 shows general block diagram of protocol converter implemented in this work which can convert UART into SPI, USB and I2C protocol. In the proposed work the FPGA is used for realizing serial protocol converter. The performance of the protocol converter is tested

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by using two different types of DACs and a USB compatible microcontroller.

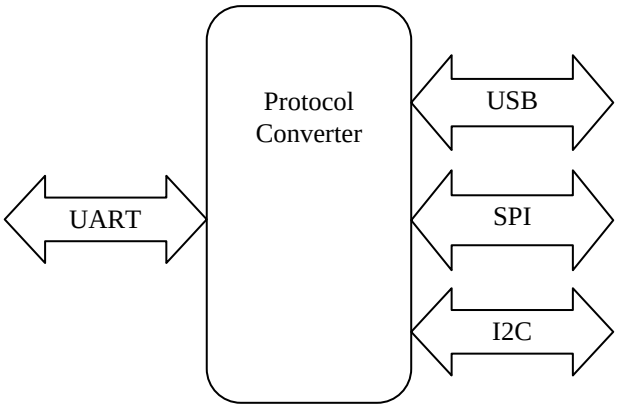

Figure 1. Proposed Design of Protocol Converter

The architecture block diagram for the proposed serial communication protocol converter is shown in figure 2.

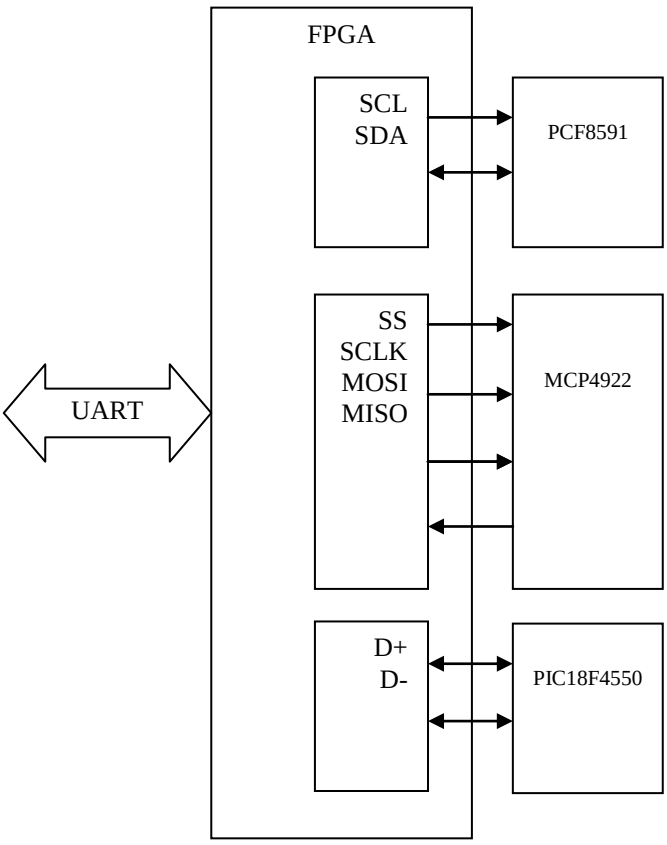

Figure 2. Architecture Block Diagram

This architecture block diagram shows that protocol converter is receiving data from host controller via UART and it converts into SPI, USB and I2C protocol. The proposed work uses SPI protocol compatible DAC (MCP4922), USB compatible 18F4550 microcontroller and I2C protocol compatible DAC (PCF8591) for testing protocol conversion. The protocol conversion technique is implemented on FPGA by using VHDL coding. The firmware development is done in modularized approach, respective modules are designed for I2C, SPI and USB conversion at low level and tested after final port mapping. The UART transceiver is designed to receive data at multiple baud rates from the host controller. Standard baud rate of 9600 is used for testing the design. The proposed architecture offers protocol conversion in parallel mode for all the three standard protocols. Provision is also given for the user to opt for the required protocol conversion and to selectively enable/disable the unused protocol block. The real time output of the protocol converter is tested and validated by interfacing the converter with commercially available data converters and microcontroller. The hardware prototype model of proposed protocol converter requires a host controller, SPI compatible DAC, I2C compatible DAC, USB compatible microcontroller for system validation. Input data for the protocol converter is received from UART receiver protocol and the protocol converter circuit in FPGA converts UART into SPI,USB and I2C protocol.

III. HARDWARE IMPLEMENTATION

Altera Cyclone-II FPGA is used for the proposed design to realize protocol bridge using EP2C5T144C8 from Altera Cyclone-II family. The FPGA configuration is done by using passive serial mode using parallel cable interface. The Altera EP2C5T144C8 Cyclone-II FPGA is capable of performing advanced RVI applications with 4068 logic elements, 26 numbers of 4K RAM blocks and 89 I/Os. The hardware is designed with 1.2V and 3.3V for the FPGA's core logic and I/O interface respectively, +5V for powering external instrumentation hardware. There are three discrete power supply voltages used in the design. VCCINT is the power supply voltage for internal logic and input buffers operating at 1.2V. VCCIO is the supply voltage for output buffers operating at 3.3V. Figure 3 shows the schematic for hardware kernel using Altera cyclone-II FPGA.

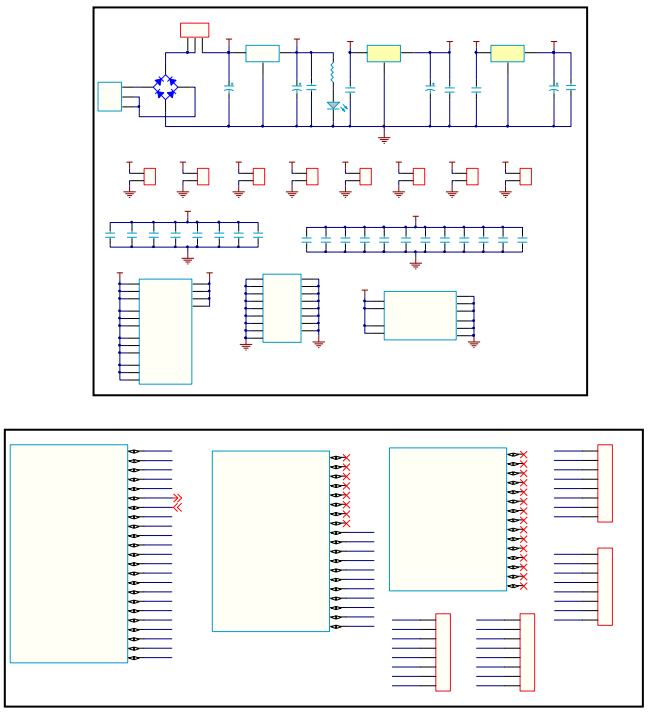

Figure 3. Schematic for hardware kernel

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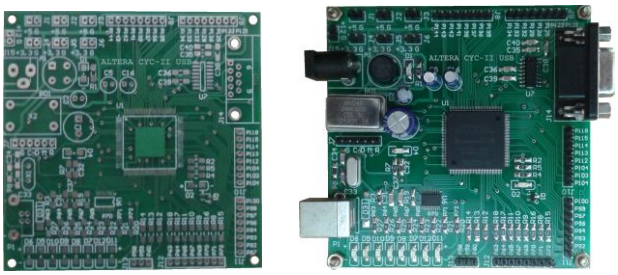

Figure 4. PCB and populated hardware for FPGA kernel

IV. SIMULATION RESULTS

The simulation of proposed work is done in Altera platform. The operating clock frequency used for this work is 24 MHz. The following figures show the simulation results and synthesis results of the proposed protocol converter.

Figure 5 shows the top level block for the proposed work, the input side of the top level block has clock input and UART receiver pin to obtain input data from host controller and output side of the top level block shows that output pins for SPI, USB and I2C protocols.

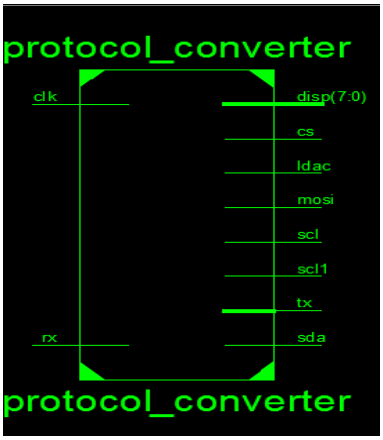

Figure 5. Top Level Block of Proposed Work

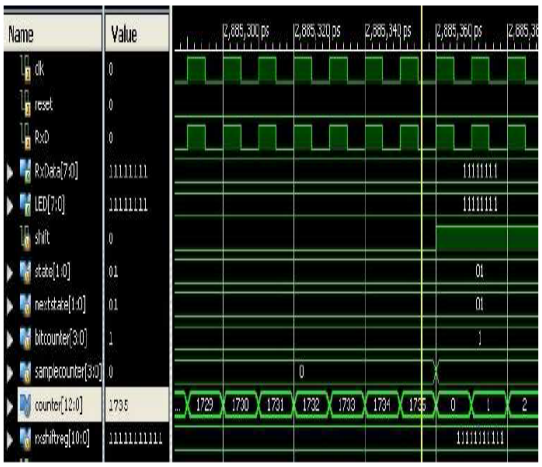

Figure 6. Simulation Output of UART Receiver

UART receiver receives data form host controller via rxd pin accumulates the bits in shift register then converts serial data to parallel. The output of UART receiver shown to figure 6.Finally UART receiver discards the start bit and stop bit and stores 8-bit data in a register. Figure 7 shows that simulation result of SPI protocol. In this work, SPI protocol is used to transmit the data which is received from the host controller through UART protocol to SPI compatible DAC. This figure explains that FPGA as a master and DAC as a slave for the serial communication.

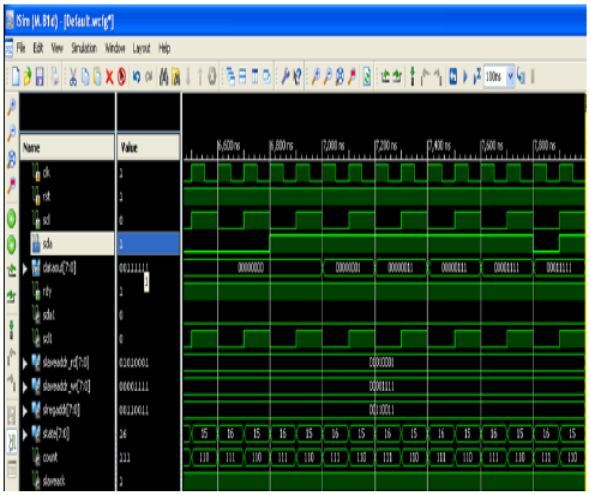

Figure 7. Simulation Output of SPI Protocol

The simulation result of I2C protocol is shown in figure 8. This shows that FPGA as a I2C master and DAC as a I2C slave both are connected through SCL and SDA lines. The FPGA master transmits data serially to slave via SDA line and supply the clock in DSL line.

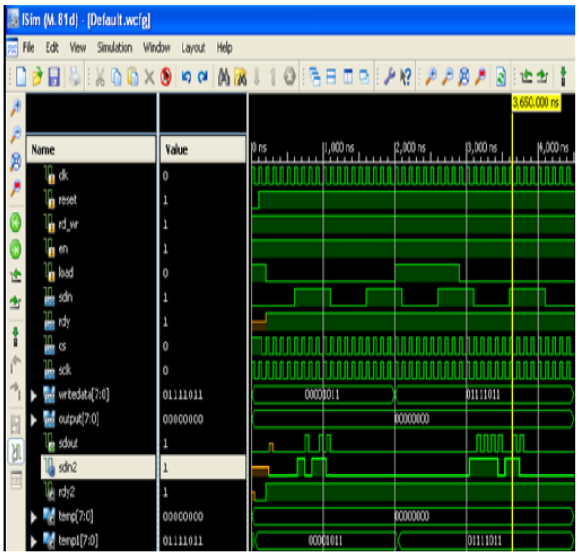

Figure 8. Simulation Output of I2C Protocol

Figure 9 shows the RTL schematic and technology schematic of proposed protocol converter

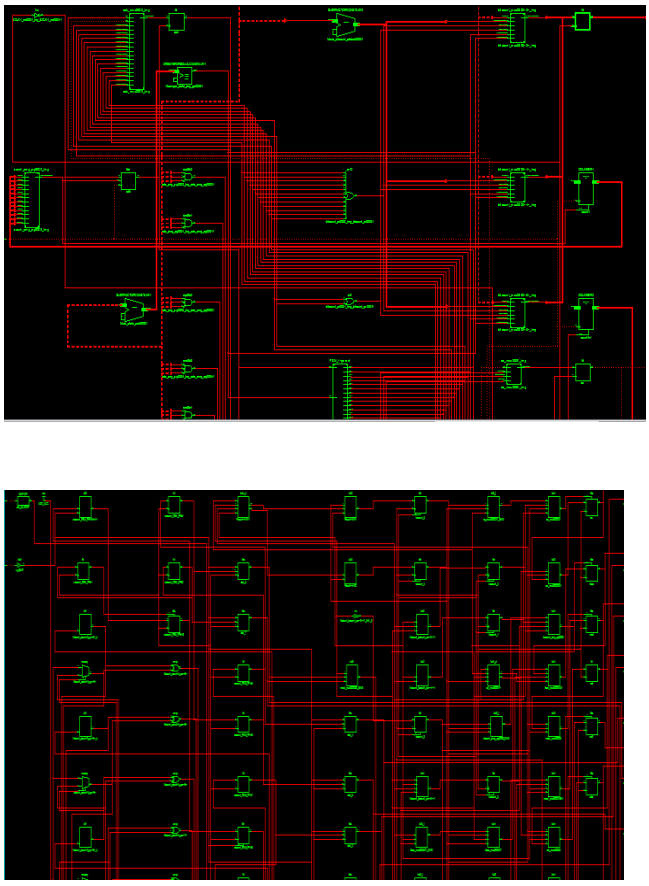

Figure 9. RTL Schematic Technology Schematic of Proposed Work

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	58	960	6%
Number of Slice Flip Flops	77	1920	4%
Number of 4 input LUTs	95	1920	4%
Number of bonded IOBs	17	66	25%
Number of GCLKs	2	24	8%

Figure 10. Utilization Summary of Proposed Work

The device utilization summary for the proposed design in FPGA is shown in Figure 10 .Result shows that slices occupation for proposed work is 6%, Flip-Flop is used 4%, 25% of bonded IOs and 4% of LUTs from overall FPGA resources.

V. CONCLUSION

In this work serial protocol translator/converter is designed and implemented on FPGA kernel to support multiprotocol devices. This work is used to minimize the design time to implement a system involving multiple devices with diverse communication protocols. Provision to choose and configure a specific protocol depending upon the requirement and adding multiple numbers of the same protocol are the added advantages of the proposed design. The design is implemented for UART, SPI, USB and I2C protocols in a single FPGA core and the results were tested against commercially available data converters and microcontrollers for data integrity. This work is designed in VHDL and simulations with real time performance are verified in Altera cyclone-II FPGA core.

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