Low Leakage and PDP Optimized FinFET based 8T SRAM Design

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Abstract—The paper proposes a Fin Field Effect Transistors (FinFETs) based SRAM design comprising of 8 transistors. The circuit utilizes channel length of 22 nanometers. The operation of this circuit is dependent upon the control switch CS that decides the operating mode and minimizes the leakage current flowing in the cell which in turn lowers the leakage power to a minimal value of 0.331pW. The read buffer available in the design provides a different path for read mode and also enhances the Read Static Noise Margin (RSNM), thus enhancing the readability of the circuit.This design is also able to operate at a minimal voltage of 70mV, thus efficiently utilizing the power available. It also optimizes the power delay product (PDP) for both read and write operations.

Keywords-*CMOS integrated circuits; FinFET; Low power; Nanotechnology; SRAM cells; Very large scale integration (VLSI)*

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I. INTRODUCTION

Ever increasing demand of all the eminent processes being performed by a single device has led to the scaling of Complementary Metal Oxide Semiconductor (CMOS) technology to lower technologies has led to enhanced integration density. But with the scaling of technology towards lower channel lengths, there arises enormous increase in the wastage of energy because the leakage current in the circuit rises. This in turn results in stand-by power consumption, i.e., the power loss when the circuit is not in operational mode or idle mode. Hence the fraction of leakage power rises in the total power budget [1]. Moreover, it is very important to operate in sub-threshold region so as to maximize energy efficiency but CMOS are very vulnerable to this region and suffer from Short Channel Effects (SCE). Moreover process variations also hinder the memory operation in the sub-threshold region. These kind of issues arise due to the poor channel controllability in the sub-threshold region that contribute to enhanced sensitivity occurring in the process variation [2, 3].

To suppress the SCE and to reduce the leakage power, many different types of solutions were presented, including: strained silicon, hetero-devices, Silicon-On-Insulator (SOI), Fin-shaped Field Effect Transistors (FinFETs), and Micro-Electro-Mechanical Systems (MEMS). Due to the most effective channel controllability, which in turn helps to suppress SCE along with lowering of the leakage current and providing a better ON current along with reduced random dopant fluctuations (RDF), FinFET devices are acted upon as an important candidate in lower nanometer technologies owing to their thin body and 3D structures.Still, new device solutions available possess a couple of challenges of conventional devices for their successful working in the sub-threshold region.Generally, it requires some more number of steps in the device abstraction process leading to greater sensitivity to process variations due to increased unpredictability in Nano-scale regime [4]-[6].

Despite the fact that the FinFETs have the ability to reduce threshold voltage (Vth) variation, many memory storage units are still considerably susceptible to the inconsistency owing to the fact that they possess a very small size resulting in dense integration, while not compromising upon its performance and reliability. One of the available solution is the Dynamic Random Access Memory or the so called DRAMs. They have an advantage over its alternatives that they does not require to refresh data regularly as the data is stored on a capacitance. But this reduced the speed as time is taken in refresh process and also enhances the total power required by the circuit. So a better alternative is Static Random Access Memory (SRAM) can hold the data because of internal positive feedback and are faster as there isn't any requirement of refreshing data [7]. Also, SRAM cells have stronger data stability and a higher write voltage margin at lower power supply voltages and thus are more in demand due to better effectiveness. It forms a part of almost every electronic device including portable electronics, micro-sensors, radio frequency identification, laptops, cell phones and cameras and many more, hence being the backbone of many different applications in very large scale integration (VLSI) area [8,9].

The traditional SRAM cell comprising of 6 transistors has good area density and performance in 90nm, 65nm, and 45nm technologies, however the aforementioned results are only applicable for supply voltages above 0.8V. Hence the traditional circuit cannot work efficiently in the sub-threshold region, resulting in the deterioration in the quality of hold stability, read stability, and write ability [10]. Moreover, there

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is also a need to minimize energy utilization of memory, so we need to decrease the minimum operating voltage. Also SRAM cell spends the majority of its time in the standby mode as they need to retain their data for some definite amount of time, which leads to increase in leakage power and leakage current that needs to be minimized [11]. Cell stability has the ability to determine the sensitivity of the memory to process tolerances and operating conditions and therefore is mostly given in the terms of Static Noise Margin (SNM), which is the maximum value of DC noise voltage that can be tolerated by the SRAM cell without changing the stored bit. This factor needs improvement especially in the read mode when the data is being read from, i.e., read static noise margin (RSNM).There needs to be a design which can provide the best tradeoff among these parameters without disturbing its proper functionality [12]-[15].The structure of the paper is as follows. In Section II, existing challenges related to SRAM cells are discussed. Section III explains the various characteristics of proposed design. In Section IV, design simulation is presented. Finally, Section V involves results and comparison analysis while Section VI finally concludes the paper.

II. Existing Challenges

The circuit formerly introduced as the SRAM storage unit had many vulnerabilities and thus it was a difficult task to store data when there was a scaling of technology from micrometers to nanometers. This design was not able to function properly at lower supply voltages, making it difficult to reduce the power consumption of circuit. Also, it has poor write ability as there exists access transistor sizing which doesn't allow the weak access transistors to interrupt the feedback loop to write data. Moreover, if the conditions of process variations are considered, the impact is much more severe, leading to low Read Static Noise Margin (RSNM) and small Write Noise Margin (WNM), which may cause read and write failures [17].So due to failure of the traditional SRAM design in many aspects, further research was conducted to find a design which could solve its drawbacks [18].Another design that was considered as an alternative to 6T was the conventional 8T SRAM. The main conception of this design was to provide different paths for read and write operation while also isolating the read buffer of memory from its storage nodes. During a read operation, storage node changes semi output node without causing any variation in the voltage [19].But still there were some issues that continued to take place in this design, namely high amount of power consumed by the circuit along with larger delays than expected used to occur. So there was a need to further research upon and find better solutions to the existing problems [20].

As the time proceeded, there were many more attempts to solve the prevailing issues which led to many more researchers suggesting different designs. Some worked upon to optimize the read buffers while some improved its write noise margin while others improved delay and power characteristics [21]. Many new concepts were proposed in order to enhance the read and write ability of the memory by using either sleep transistors or power gated circuits or even by utilizing the basic concepts of pass transistors and transmission gates. Some researchers' designs led to increased cell heights, thus increasing the amount of power consumption [22]. Some increased the number of transistors in the circuit to combat power issues but compromised area involved [23]. Some tried to lower down the supply voltage to reduce leakage power. Though the dynamic voltage scaling is helpful in reducing power loss but it comes at the cost of data stability and write ability resulting in functional failures including read, hold and write failure resulting into yield loss [24]. Some reduced the amount of leakage in the circuit by removing idle gates from the circuit. There is another solution to save power and that is to reduce the device dimensions but it again leads to degradation the data stability and write ability of SRAM cells [25].The concept of stack transistors was an innovative idea but this increased the resistance between supply voltage and ground, thus increasing the amount of leakage current [26]. But still there is a need to improve overall cell stability of the circuit without compromising its power, delay and PDP.

III. Proposed SRAM Cell

Most of the work done in the field of VLSI considers area and speed as the ruling parameters which define the effectivity of the device. But recently the modern gadgets require energy efficient construction because of many aspects, namely increasing leakage currents, power loss and reliability. Fig. 1 shows the FET model symbol for BSIM-CMG model that can be used as both PMOS and NMOS depending upon a certain parameter. Also fig. 2 depicts the schematic representation of the proposed design of the SRAM cell.In this circuit, read and write operations have different paths for its operation, so that they do not interfere with each other's working. There also exists an extra transistor in the internal latch which is controlled by Control Switch. This switch is used to minimize the leakage current and leakage power in the idle state as well as maximize readability of the cell.

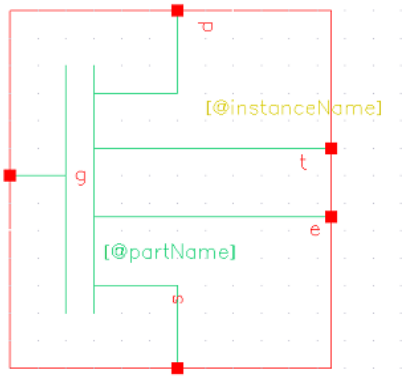

Figure 1. FinFET Symbol

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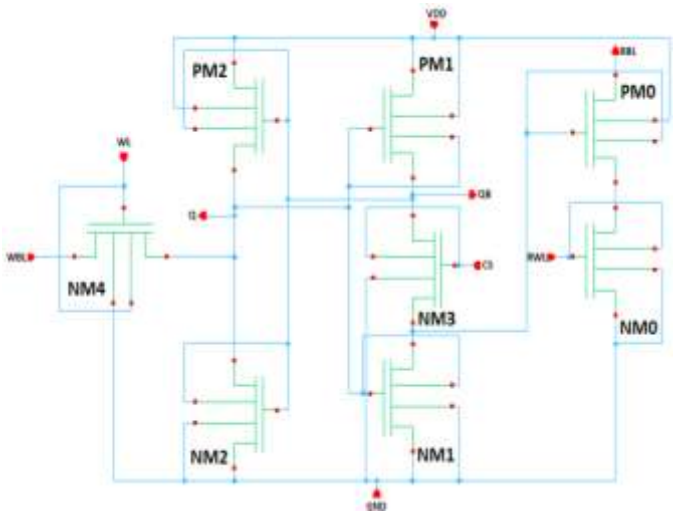

Figure 2. Proposed 8T SRAMSchematic

The proposed 8T SRAM Cell symbol is shown in fig. 3. This symbol is utilized for the verification of the SRAM design for proper functioning. It can also be used to form the SRAM cell Array to store much more amount of data and thus avoiding the complexity that can occur in arranging the overall architecture.

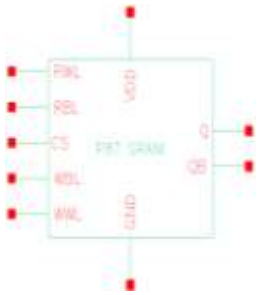
Figure 3. Proposed 8T SRAM Symbol

There are three different operating modes available for the SRAM cell, i.e., read, write and hold mode. During the read mode,circuit is managed with the help of read buffer, comprising of PM0 and NM0. The pmos of buffer is connected to the internal latch of the memory cell, while the nmos is connected to the read bit line which controls the data to be written upon the cell.This internal latch comprises of an extra nmos NM3, controlled by a Control Switch CS. This switch is turned on and act as a closed switch during read mode, thus resulting in higher RSNM.The write operation is performed with the help of word bit line WBL along with the access transistor NM4. The extra bitline that was used in the conventional designs has been removed so as to avoid excess leakage of power within the circuit, without compromising its functionality, i.e., there does not occur any write failure when the data is being written into SRAM cell.Hold mode is very essential for effective working of the circuit. In this state the cell is supposed to retain its previous data without letting out the flow of power. This design tries to minimize the leakage power as well as leakage current with the help of NM3 available in the latch circuitry. This nmos is responsible for the extra resistance path that can be effectively utilized by switching CS to logic 0. It hence creates a barrier to the flow of leakage current due to high impedance.

IV. Design Simulation

SRAM cells are considered as the most important part of almost every electronic gadget. Designing of these memory cells requires utmost care when considering their transistor parameters. Table 1 shows the parameters along with their values for FinFETs based SRAM cell for the 22nm technology.

TABLE I. FinFET Parameters involved

Parameters	Definition	Value
L	Gate Length	22e-09m
TFIN	Body (Fin) thickness	15e-09m
FPITCH	Fin Pitch	80e-09m
COVS	Constant gate to source overlap capacitance	0
COVD	Constant gate to drain overlap capacitance	COVS
VDD	Default supply voltage	1V
NBODY	Channel Doping Concentration	$1e22m^{-3}$
Vth	Threshold Voltage	0.525(n), -0.506(p)

The proposed work regard the schematic design to study its behavior in Nano-scale technology node with the help of Cadence Virtuoso (Virtuoso V.6.1) and BSIMCMG 110.0.0 model for FinFETs using 22nm technology. Analog simulation of designed SRAM cell has been performed to ensure that there doesn't exist any read or write failures. Fig. 4 shows the power response for the proposed circuit using FinFET technology.

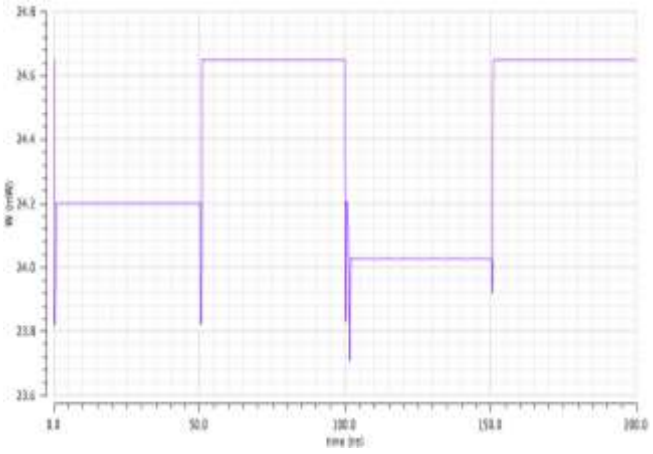
Figure 4. Proposed 8T SRAM Power Response

V. Result Analysis and Comparison

The proposeddesign is worked upon by updating the existing designs with the help of FinFETs. As power and delay are the most eminent parameters to ensure the efficient working of any device, thus they are analyzed as the fundamental

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metrics of evaluation and thus are taken care of. Moreover the improvement in these two parameters leads to optimization in terms of energy in both the active modes i.e., read and write mode. The incorporation of the designed SRAM cell will also be carried out for low power low delay design.

There are different parameters upon which the proposed work is compared with the existing designs.Due to the ultra-scaling of transistors, short channel devices have leakage occurring in the circuit.The current leakage components flowing in the circuit results in leakage of power. The standby leakage power is measured at minimum supply voltage where 6σ hold stability is assured. Also while measuring leakage component, bit lines are activated while the wordlines are deactivated. Table 2 shows the comparison of the proposed design in terms of leakage power flowing in the circuit. The reduction in the amount of leakage power of the projected design as compared to the existing works is shown in fig. 5.

TABLE II. LEAKAGE POWERCOMPARISON ANALYSIS

Parameter	Conv. 8T	Ref [16]	Ref [17]	Ref [18]	Ref [19]	Ref [20]	Proposed Work
Leakage Power	2.1 µW	2.2 µW	2.5 µW	2.7 µW	1.8 µW	2.1 µW	0.331 pW

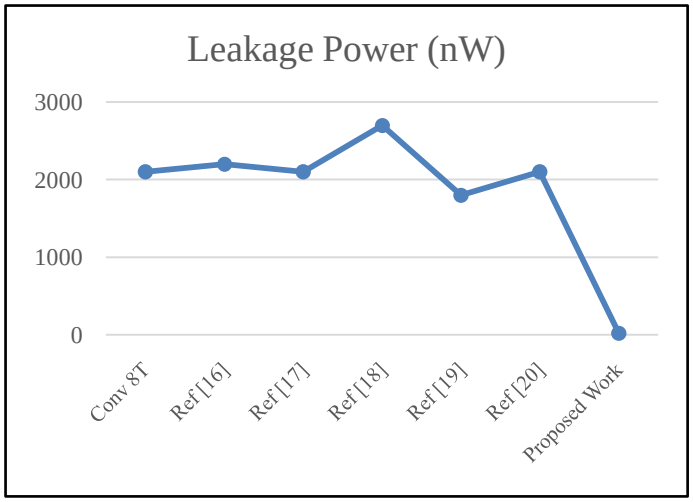

Figure 5. Leakage Power Comparison (nW)

Another important parameter for the successful operation of SRAM circuits is the minimum supply voltage at which the SRAM does not compromise its operability. This is known as V_{min} of the circuit.Table 3 shows the comparison of the suggested design with the existing literature in terms of minimum operating voltage required for desired. Fig. 6 shows the pictorial comparison of minimum supply voltage and read delay respectively.

TABLE III. VMINCOMPARISON ANALYSIS

Parameter	Conv. 8T	Ref [21]	Ref [22]	Ref [23]	Proposed Work
Minimum Voltage (V)	0.15	0.15	0.11	0.10	0.07

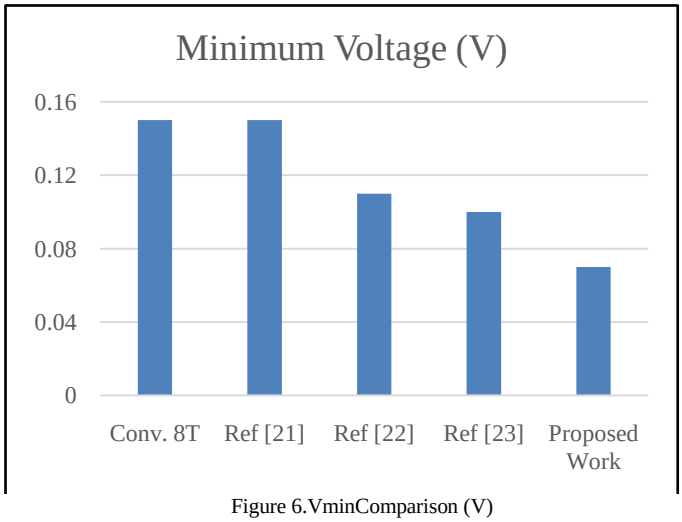

Figure 6.VminComparison (V)

Moreover the circuit is ruled with the power and delay as the prime factors for absolute energy of SoC but it is the PDP that characterizes the efficient working of device, so lowering this parameter is critical in real time applications. It decides the practicality of any circuit and decides its effectiveness to be implemented into chips. Table 4 shows that the proposed design is much more optimized in terms of read, write and average PDP.Fig.7 shows the pictorial representation of this comparative analysis of energies with the existing works.

TABLE IV. PDPCOMPARISON

Parameter	Ref [24]	Ref [25]	Ref [26]	Proposed Work
Read PDP (pJ)	0.56	0.71	0.39	0.0011
Write PDP (pJ)	1.57	0.97	0.80	0.0013
Average PDP (pJ)	1.065	0.84	0.595	0.0012

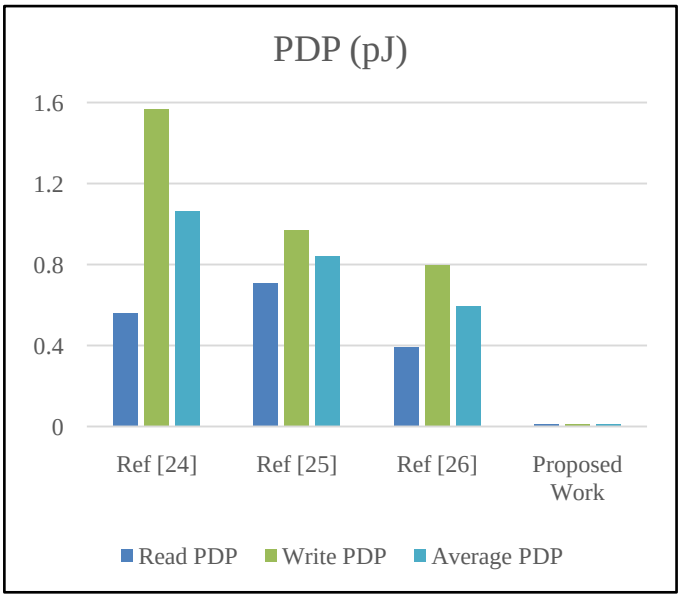

Figure 7.PDP Comparison (pJ)

VI. CONCLUSION

The proposed design of SRAM cell comprises of 8 FinFET transistors. FinFET transistors are utilized as they are well

known as a replacement for the conventional planar CMOS technology because of enhanced channel controllability. Even with the technology scaling down of technology, does not have much of an impact on the functionality of the device. Thisdesign is able to work properly even in the deep sub-threshold areas, much below the supply and threshold voltages. It is also possible to reduce the amount of the supply voltage to a minimal level, which means it requires a very small amount of voltage to run its operations. Performance analysis of the suggested design with the existing ones shows that this circuit is PDP efficient in all the active modes i.e., read and write modes.

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