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Energy Efficient CNTFET Based Full Adder Using Hybrid Logic

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Abstract—Full Adder is the basic element for arithmetic operations used in Very Large Scale Integrated (VLSI) circuits, therefore, optimization of 1-bit full adder cell improves the overall performance of electronic devices. Due to unique mechanical and electrical characteristics, carbon nanotube field effect transistors (CNTFET) are found to be the most suitable alternative for metal oxide field effect transistor (MOSFET). CNTFET transistor utilizes carbon nanotube (CNT) in the channel region. In this paper, high speed, low power and reduced transistor count full adder cell using CNTFET 32nm technology is presented. Two input full swing XOR gate is designed using 4 transistors which is further used to generate Sum and Carry output signals with the help of Gate-Diffusion-Input (GDI) Technique thus reducing the number of transistors involved. Proposed design simulated in Cadence Virtuoso with 32nm CNTFET technology and results is better design as compared to existing circuits in terms of Power, Delay, Power-Delay-Product (PDP), Energy Consumption and Energy-Delay-Product (EDP).

Keywords-*Carbon Nanotube Field-Effect Transistor (CNTFET); Nanotechnology; Full Adder; Low Power; High Speed; Power Delay Product.*

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I. Introduction

With the arrival of new technology,Moore's predicted that the transistor count on every integrated circuit (IC) will double about every 18 months. To meet the demand of compact designs, it became essential to continuously scale down the channel length in Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) and produce vast numbers of transistors on a single piece of the chip as predicted by Moore's law [1]. After 2006, the channel length of a MOSFET device has come down in the deep submicron/Nano range. The feature size started decreasing rapidly from 250nm to 180 nm, 135nm, 90nm, 65nm, 45nm and so on. Today statistics says that 32nm technology is among the realistic channel length being used and as per International Technology Road map for Semiconductors (ITRS) suggestion by coming years channel length of MOSFET will be reached around10 nm. Since, the physical gate length of device decrease lower, there is an abrupt rise in device parameters and leakage current becomes the most valuable factor in device optimization and hence, V-I characteristics of predictable MOSFET are extensively affected [2, 3].

In modern time, MOSFET technology needs to be replaced by alternate technologies, the conventional MOSFET have to be interchanged by quantum effect, molecular electronic device and single electron solid state device. Among the given types, molecular electronics device is one of the most capable candidate [3]. The aforementioned limitation of MOSFET force the researcher to involve new circuit and specific field of research i.e. Nano devices such as silicon nanowire transistors, Single Electron Transistor (SET), Resonant Tunneling Diode (RTD), Spin Transistor (SPINFET).Quantum-dot Cellular Automata (QCA), Graphene Nanoribbon Transistor (GNRT) and Carbon Nanotube Field Effect Transistor (CNTFET) have begin to replace the conventional bulk-CMOS technology in the near future [4]. Among the introduced novel technologies, CNTFET seems to be more successor for CMOS due to the presence of both n-type and p-type CNTFET, intrinsic relationship of both technologies and remarkable properties of CNTFET. Due to exclusive characteristics of CNTFET device, the existing logic style even with the higher advantage will be able to accommodate with the new technology [5].

Full adder is the basic element of any circuit design that perform arithmetic operations just like multipliers, comparator, compressor, parity checkers and address generation in memory. So reducing the amount of power consumption in full adder, it will help to decrease the total power consumption of the complete circuit [6].Over years various designed are developed for Full adder. In terms of power consumption and speed of circuit each design have its own merits and demerits.It can be observed from past designs that most of the work in Full Adder design using CNTFET has been done either to optimize the power, delay or PDP (Power Delay Product).CNTFETs have been used previously in many circuits as they require less amount of power when compared to the CMOS based designs. But it is also important to consider the propagation delay, which defines the speed of any device [7]. While the power is improved in some of the previous works, the delay parameter got neglected, as well as the area involved in terms of the number of transistors utilized. There is a further need to optimize the circuit in order to find the best combination of transistor logic so as to optimize power and delay simultaneously, while utilizing an optimal number of transistors and by using different logic styles like binary, ternary and hybrid techniques to optimize the design [8, 9].

The rest of this paper is organized as follows. In section II proved a brief description of CNTFET. In Section III, schematic design and simulations are presented. Section IV analyzed and compare results. Finally, Section V concludes the paper with the future work.

II. Carbon Nanotube Field Effect Transistors

Carbon Nanotube (CNT) is Nano-scale tube made up from a rolled sheet of graphite which is rolled up along a wrapping vector. A CNT could be single-wall (SWCNT) or multi-wall (MWCNT). Single-wall CNT is made from one layer of graphite that composed one cylinder and multi-wall CNT is made by more than one layer of graphite, then it is rolled up and resulting in a common centre for all cylinders centres is same [10]. Carbon nanotubes are represented by a vector, called chirality vector that defines the arrangement of carbon atoms along the tube. A chirality vector of a CNT is described by chiral number, i.e. denoted as (n, m). In Fig. 1, chirality vector is given by Cn and is derived from : $\bar{C}_n=n_1.\bar{a}_1+n_2.\bar{a}_2$ where lattice unit vectors are $\bar{a}_1$, $\bar{a}_2$ and n_1& n_2 are positive integers which specify the tube's structure. These indices determine the arrangement of atoms along the nanotube. We have three different kinds of nanotubes: armchair, chiral and zigzag and the SWCNT have different manners such that if $n1-n_2=3K$ ($k\epsilon Z$) then SWCNT is conducting, otherwise SWCNT is semiconducting. Conductive CNT applied as nanowires and semi-conductive CNT is used as transistor channel [11, 12].

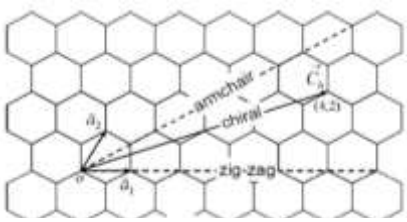


Figure 1. Representation of a SWCNT of a chiral vector [17].

Identical to the MOSFET, the CNTFET has four terminals. Given in Fig. 2, undoped semiconductor Nano tubes were founded under channel region and for low series resistance in the ON-state the heavily doped Carbon Nano Tube sandwiched between the source/drain and the gate. Depending on the gate voltages, the device gets turned ON or OFF with the help of the gate. The V-I characteristic of CNTFET is alike to a MOSFET. In Fig. 2(a), structure of CNTFET device is given and top view of the structure is in Fig. 2(b). The distance between centres of two adjoining SWCNT nanotubes under the same gate of CNTFET is called pitch, which affect the contacts of the transistor and the width of the gate [13, 14]. The width of the CNTFET gate is based on the following equation

$$W_{Gate} \approx \text{Min}\,(W_{min}, N*\text{pitch}) \quad (1)$$

Where N is the number of nanotube in the channel and W_{min} is the minimum width of the gate. Analogous to the MOSFET, a CNTFET device also possesses voltage that can electronically turn on the transistor via gate, known as the threshold voltage (V_{th}) [15].

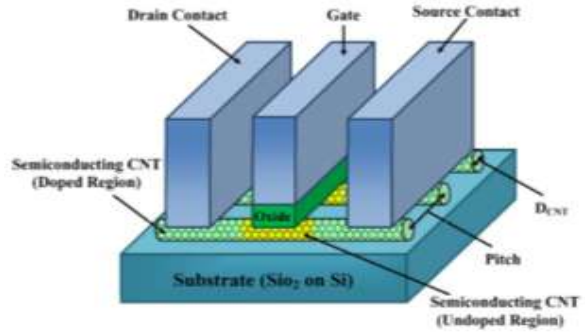


Figure 2. Schematic of CNTFET [21].

The threshold voltage of a CNTFET is approximately founded to be half the bandgap and can be calculated based on the following equation:

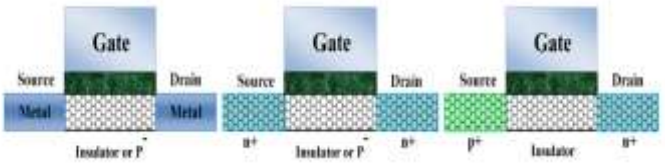
$$V_{th} \approx \frac{E_g}{2q} = \frac{av_\pi}{\sqrt{3}\,q D_{CNT}} \quad (2)$$

Where parameter a (≈2. 49Å) is the carbon to carbon atom distance.$V_\pi$is carbon π-π bond energy in the tight binding model.D_{cnt} is the diameter of the CNT, q (=1.6 e^{-19} C) is the electron charge and$E_g$is an energy gap [16].

Therefore, by varying the diameter of CNT with different turn on voltages, different transistors can be implemented. From (2), it is clear that threshold voltage is the inverse of the diameter of CNT which is calculated by following equation:

$$D_{CNT} = \frac{\sqrt{3}a_0+\sqrt{(n^2+m^2+mn)}}{\pi} \quad (3)$$

Where a_0 = 0.142 nm is called interatomic distance, which is the distance between the carbon and neighbouring atom [17]. Three main types of CNTFET exist that rely upon the type of source, drain and gate and type of connections between source and drain with CNT channel. In the first type CNT directly connects contacts to metal source and is known as schottky barrier CNFET (SB-CNFET).It is also known as tunnelling transistor as the source/drain channel junction performs the principal of direct tunnelling via a schottky barrier (SB). [18, 19].



(a) (b) (c)

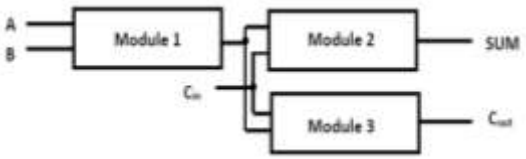
Figure 3. (a) SB-CNFET (b) MOSFET-like CNFET (c) T-CNFET [24].

In the On state, the energy barrier limits the Trans conductance and decreases the drain current (I_d), thus ION/IOFF ratio becomes relatively low. SB-CNFETs have ambipolar attribute and is reliable for medium to high-performance applications. The second type of CNFET, known as band-to-band tunnelling CNFET (T-CNFET) shown in Fig. 3(c). T-CNFET has low ON current and super cutoff attribute [20]. These conditions make it suitable for sub-threshold and ultra-low power application, but it is not much suitable for very high speed operations. The third type of CNFET, known

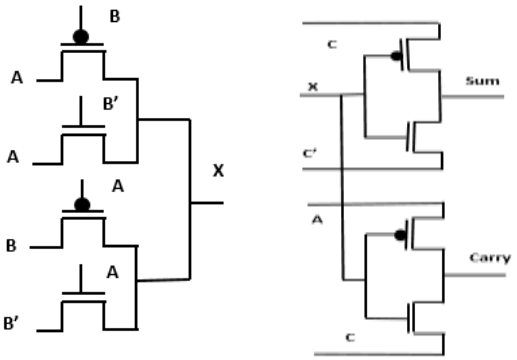
as MOSFET-like CNFETs shown in Fig. 3(b). In this CNTFET source-channel junction is not schottky barrier and between source-drain and channel semiconductor-semiconductor junction is formed because positive impurities are doped in source and drain. MOSFET-like CNTFET is appropriate for high performance operations because it has high ON/OFF ratio, high ON current and scalability. In this paper, use MOSFET-like CNTFETs for all proposed designs [21, 22].

III. Proposed Full Adder

In this paper the proposed full adder design is generated by using three blocks and presented in Fig. 4(a). Module 1 and Module 2 comprises of XOR gates, by using these gates sum signal (SUM) is generated at the output. And with Module 3 Carry signal (C_{out}) is generated at the output. Each module is designed carefully to optimized entire full adder in terms of power, delay and PDP. Details of each module is discussed below:



(a)



(b) (c)

Figure 4. a) Schematic structure of proposed full adder. (b) XNOR module. (c) Sum and Carry generation module.

A. *Modified XOR Module:*

In most of the full adder circuits XOR module is responsible for the maximum power consumption. In this section a new XOR module is proposed to design low power full adder. Fig. 4 (b) shows the XOR module, which reduces the power consumption by eliminating the power consuming XNOR gate and avoiding the possibility of voltage degradation. XOR module used in this design is full swing, without feedback transistors in order to reduce delay and power consumption. Module of XOR gate uses 6 Transistors and have the benefit of full swing output. Inverter between input chain and Sum output act as buffer and decreases the propagation delay. Multiplexers are implemented by using only two transistors with pass transistor logic. Full swing XOR module neglect the double V_T threshold problem and high leakage power consumption at the output. The result of module 1 is represented in(4):

$$X=A\oplus B \quad (4)$$

B. *Sum and Carry Generation Module*

In the proposed circuit, the output Sum and Carry signal are implemented by using GDI (Gate-Diffusion-Input) logic, which allows reduction in propagation delay, power consumption and area involved of the circuit. Sum and Carry Modules are shown in Fig. 4(c).A basic GDI cell consists of four terminals: G (common gate input of PCNTFET and NCNTFET), D (common diffusion node of both transistors), P (the outer diffusion node of PCNTFET) and N (the outer diffusion node of NCNTFET). The main characteristics of circuits are: (1) GDI has three inputs- G (gate input to NCNTFET / PCNTFET), P (input to source of PCNTFET) and N (input tosource of NCNTFET). (2) Bulks of both NCNTFET andPCNTFET connect to N or P (respectively), so it can bebehave as CMOS inverter. GDI technique can implement various logic functions by using only two transistors. This approach is sufficient for a design which is fast and low power with less number of transistors. Sum and carry signal outputs are represented in (5) and (6):

$$Sum = (A\oplus B)\oplus C_{in} \quad (5)$$

$$Carry = AB+BC+AC \quad (6)$$

IV. Design Specifiaction and Simulation

The full adder design has been simulated in cadence virtuoso simulator. For simulating this circuit, compact SPICE model and 32nm CNTFET technology has been used. This SPICE model is developed for unipolar, MOSFET-like CNTFET devices,also known as the standard model of CNTFET. In this model, each CNTFET transistor has one and more than one CNTs under the gate as per requirement. This model further involves Schottky Barrier Effect, including CNT, Parasitics, Gate and Source/Drain capacitance and resistance, and CNT Charge Screening Effects. Table 1 shows, brief description of CNTFET model Parameters and along with their values. All of the simulation has been done at room temperature with voltage0.9V and design is optimized in terms of Power, Delay, PDP, Energy and EDP.

TABLE 1. CNTFET MODEL PARAMETER

Parameters	Description	Value
L_{ch}	Physical channel length	32nm
L_{geff}	The mean free path in the intrinsic CNT channel	200nm
L_{ss}	The length of doped CNT source-side extension region	32nm
L_{dd}	The length of doped CNT drain-side extension region	32nm
K_{gate}	The dielectric constant of high-K top gate dielectric material (planner gate)	16

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T_{ox}	The Thickness of high-K top gate dielectric material (planner gate)	4nm
C_{sub}	The coupling capacitance between the channel region and the substrate (backgate effect).	40pF/m
E_{fi}	The Fermi level of the Doped S/D tube	0.6ev
Pitch	The distance between the centers of two adjacent CNTs within the same device.	20.0nm
W_{gate}	The width of metal gate.	6.4nm
(n1, n2)	The chirality of tube.	(19,0)
Tubes	The number of tubes in the device.	1

The schematic of 1-bit full adder is shown in Fig. 5, which is constructed with PCNTFET (p carbon nanotube field effect transistor) and NCNTFET (n- carbon nanotube field effect transistor) transistors.

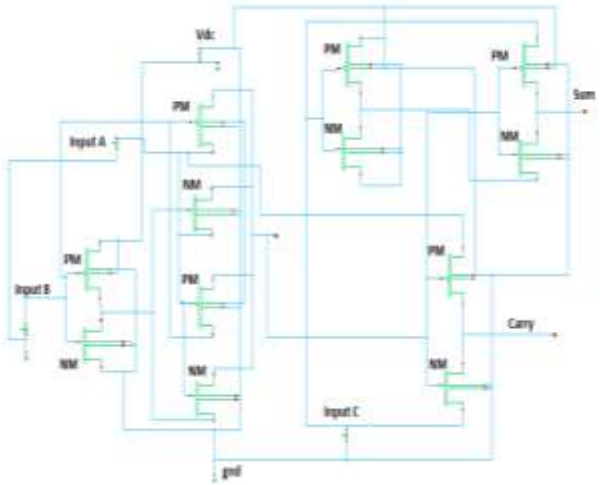

Figure 5. Schematic of Full Adder

For logic verification analog Simulation of full adder design has been performed. The transient and DC response of the proposed design of full adder is shown in Fig. 6 and Fig. 7.

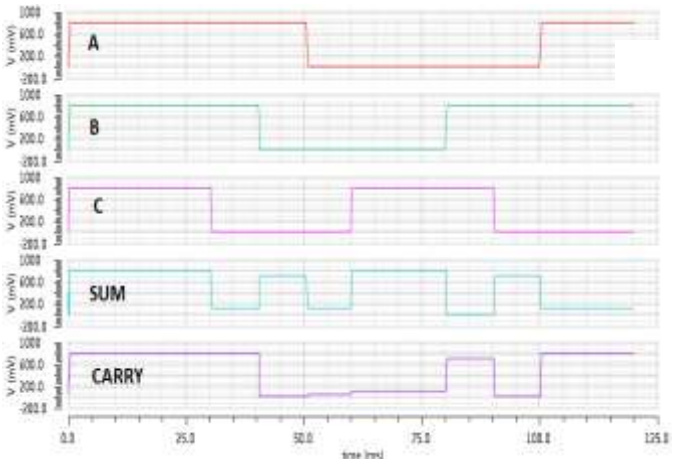

Figure 6. Transient response of Full Adder

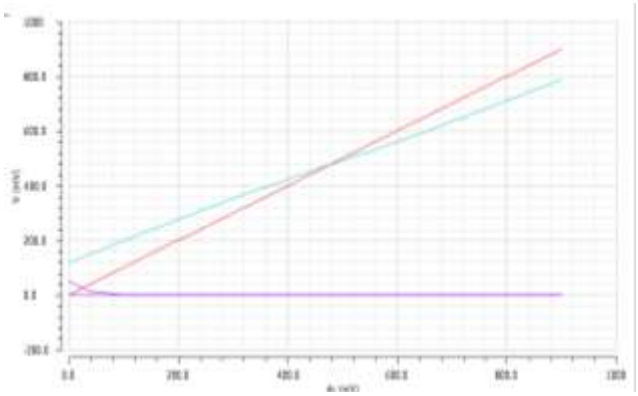

Figure 7. DC response of Full Adder

The power waveform of proposed full adder is shown in Fig. 8. The power parameter is calculated by taking the average of this waveform. Reduction in power consumption by using hybrid technique which reduce the number of transitors.

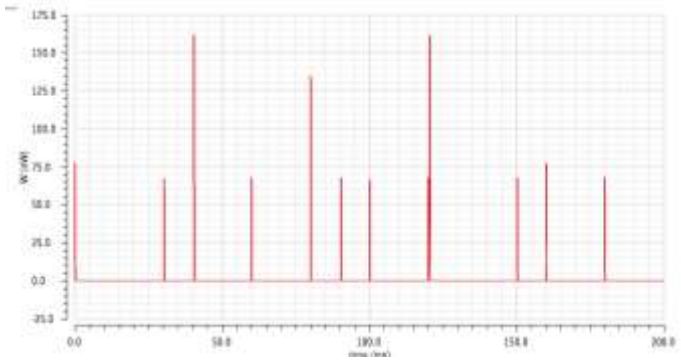

Figure 8. Power Waveform of Full Adder

V. Results Analysis

As reported in ITRS standard voltage for 32nm CNTFET technology is 0.9V. The schematic designs have been simulated for supply voltage0.9V. Power, Delay and power-Delay –Product (PDP) are taken into consideration for design evaluation. All the transistor at input in schematic design are verified and delay parameter has been calculated for each input supply voltage. The Delay has been measured at different points in the circuit and maximum value of measurement is considered as the delay of the circuit. The parameter value of power consumption is calculated from the average power consumption over the maximum period of time. Finally the PDP is calculated from power and delay, for constructing tradeoffs between power and speed.

Table 2 shows that power, delay and PDP of proposed design has improved than all the compared designs. And table 3 shows the Delay, Power, Energy Consumption and EDP analysis and comparison with existing designs.

TABLE 2. PERFORMANCE ANALYSIS

Reference	Ref [19]	Ref [20]	Ref [21]	Proposed
Power(μW)	0.6512	0.2630	0.3021	0.000809
Delay (ps)	27.376	25.393	15.204	2.477
PDP (aJ)	17.828	6.6792	4.5927	0.00200

TABLE 3. PERFORMANCE ANALYSIS

Reference	Ref [22]	Ref [23]	Ref [24]	Ref [25]	Proposed
Delay (e^{-12}s)	42.62	27.3	39.1	6.39	2.477
Power (e^{-6}W)	2.05	0.896	1.041	0.733	0.000809
Energy (e^{-15}J)	20.5	8.96	10.4	7.33	0.00809
EDP (e^{-24J}.s)	0.873	0.24	0.41	0.044	0.00002

The parameter comparison state the proposed full adder works more efficiently. Fig.9 shows the power, delay and PDP comparison of the proposed design at 0.9v with existing circuits of table 2.

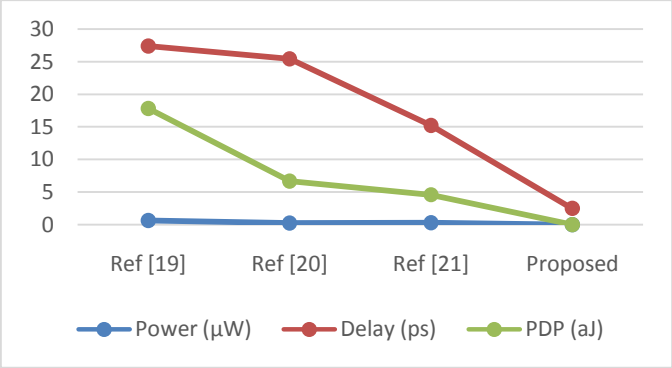

Figure 9. Comparison of Power, Delay and PDP

Fig.10 shows the Power, Delay, Energy consumption and EDP comparison of the proposed design at 0.9v with existing circuits of table 3.

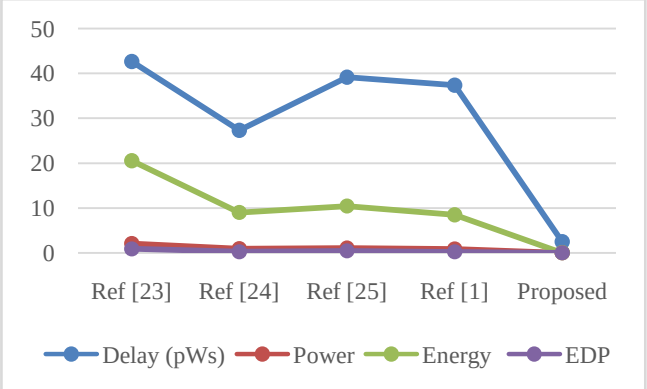

Figure 10. Comparison of Delay, Power, Energy and EDP

VI. Conclusion

In modern time,MOSFET technology required to be changed with alternate technologies and CNTFET emerges as the most suitable candidate. CNTFET have unique features such as low OFF-current and ballistic transport, which gives low power consumption and high speed designed circuit. The work proposed has resulted in high speed, low power consumption and reduced transistors CNTFET based full adder. In proposed design, number of transistors gets reduced by using GDI technique for sum and carry modules. Designing and simulation analysis is done using 32nm CNTFET technology in Cadence Virtuoso. The results conclude that there is an improvement in terms of power consumption, propagation delay, Power-Delay-Product (PDP), Energy Consumption, Energy-Delay-Product (EDP)as compared to the existing designs.

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