

Design of Fast Integer Pipelined Multipliers for CMOS 64-bit Synchronous and Asynchronous Logic with Adaptable Latency

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Abstract—Adaptive latency multiplier architecture suited for implementation of multiplier. The architecture combines a second-order carry save and carry select with skipping of the row and split carry using pipelined architecture. The architecture and logic design of CMOS 32-bit synchronous implementation is 2.5 ns. The proposed architecture and VLSI design demonstrates that an adaptive latency multiplier, in either synchronous or asynchronous implementations. This architecture can be used in fast performance multipliers.

Index Terms—Arithmetic units, asynchronous systems, multipliers, VLSI design, Throughput.

I. INTRODUCTION

For the high speed multipliers which is used in DSP processors and advanced microcontrollers, the CMOS architectures are used in order to obtain such an accurate arithmetic manipulations. In micro architectures with CMOS implementation 2ns has proved. [15]. In full custom CMOS multiplier design < 3ns is possible [14]. Pipelined multipliers are impact on various factors like registers, propagation delay and it is limited by certain times and leads to slow down the performance of multiplier process.

In order to increase the throughput of pipelined arithmetic adaptive latency logic has been proposed [18]. The interfacing is the basic problem between the synchronous and asynchronous unit because of signal handoff. High speed VLSI adder has been proposed in previous work [16][13]. But still there is an issue on adaptive latency between synchronous and asynchronous interfacing. Asynchronous (i.e., unclocked) design but not adaptive latency [7], [11] to reduce power consumption was addressed earlier but not for high speed.

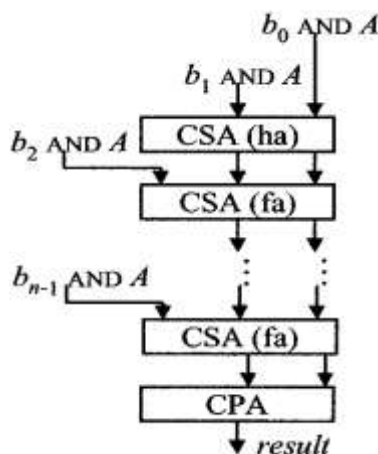


Fig.1 Simple blocks of Array Multiplier

The aim of the paper is to produce fastest multiplier design with accuracy. The proposed design deals with pipelined multiplier architecture, which combines various algorithm and design VLSI implementation for synchronous adaptive latency multiplier.

II. ARCHITECTURE AND LOGIC DESIGN OF THE PROPOSED MULTIPLIERS

$$\text{Delay} = \text{Denc} + \text{Dsel} + \text{DHA} + (n/4 - 2) \text{DFA} + \text{D} \text{ 4:2} + \text{Depa}$$

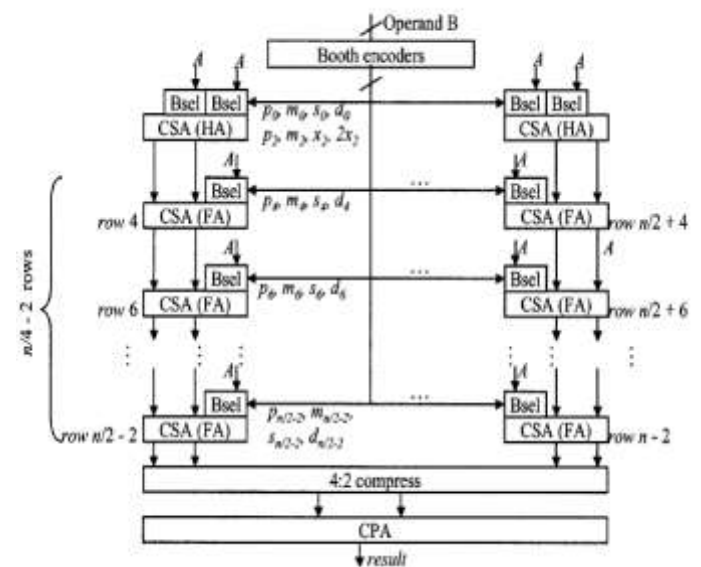


Fig. 2 Architecture split-array multiplier

where the delay contributions are Denc: Booth encoding logic producing the encoding bits p,m,s,d; Dsel logic that selects the operation of each CSA row according to the encoding bits DHA : half-adder (CSA row); DFA: full-adder (CSA row), : 4 : 2 compressor; Depa : final CPA.

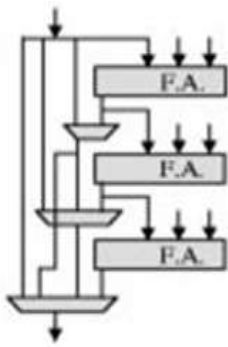


Fig. 3 Model – Dummy Path

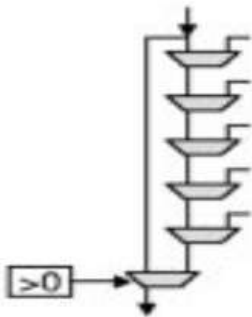


Fig. 4 Model - Delay Selector

III. SYNCHRONOUS VARIABLE-LATENCY DESIGN IMPLEMENTATION

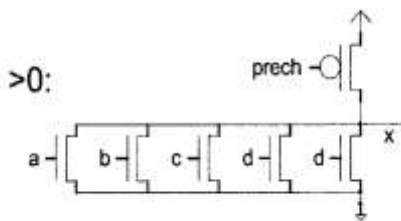


Fig.5 VLSI design of the logic producing the “onecycle” signal [>0]

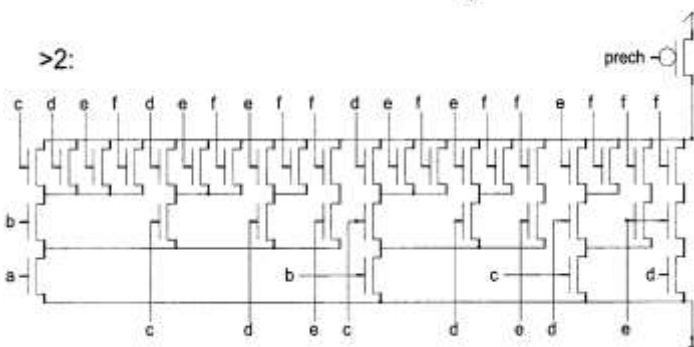


Fig.6 VLSI design of the logic producing the “onecycle” signal [>2]

$$Donecycle = Denc + Dsel + DHA + 2(DFA+DMUX) + 2 DMUX + DMUX + D4:2 + 7 DFA + Ddet$$

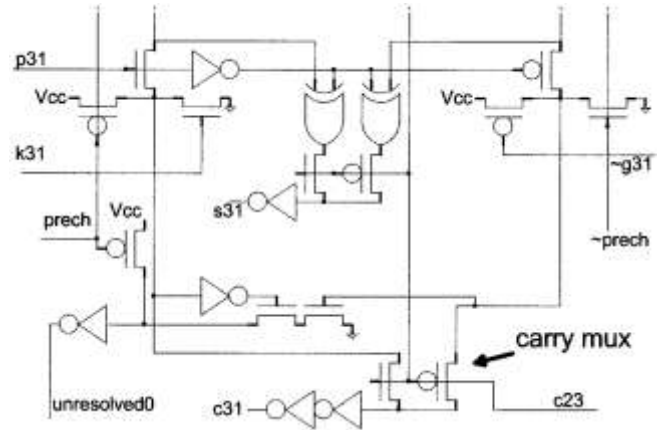


Fig.7 Full custom VLSI design of a carry select block unresolved carry detection circuitry.

$$Dsinglecycle = Db-enc + Db-sel + Dha + 2(fa + Dmux) + 2 Dmux + Dmux + D4:2 + 7 Dfa + Dmux$$

$$Donecycle = Dboothenc + Dboothsel + 2 (Dfa + Dmux) + 2Dmux + D4:2 + 7 Dfa + Ddetect$$

IV. VLSI DESIGN OF ADAPTIVE LATENCY IMPLEMENTATION

IMPLEMENTATION

The adaptive latency asynchronous multiplier is based on the micropipeline architecture [17]. The multiplier is designed as two-stage micro pipelines interfaced with the external request/acknowledge 2-phase signals at the input and another pair at the output of the multiplier. Double edge triggered memory elements in order to reduce the micro pipeline interconnections and switching activity.

V. PERFORMANCE RESULTS

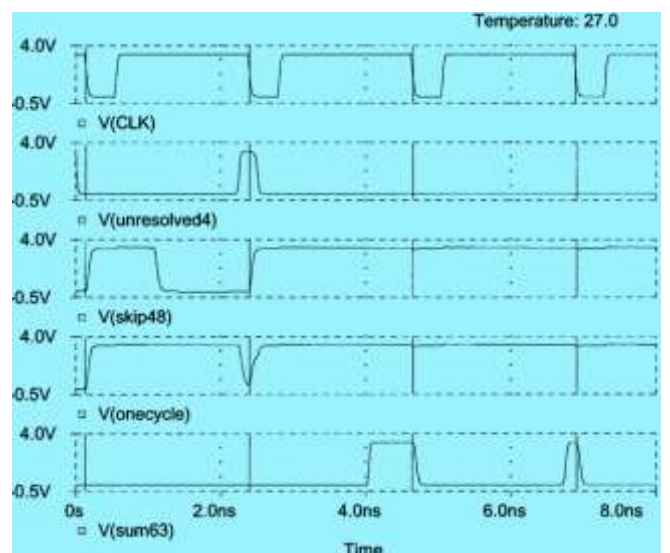


Fig.8 HSpice Simulation Results

HSpice simulation of the synchronous multiplier with 0.35 m CMOS process. Long metal line parasitic capacitances were manually coded into Spice netlists, based on a hypothetical layout of the circuits. The capacitance of

the internal nodes that may cause charge redistribution effects are actually small, compared to the load capacitance and the parasitic capacitance of the output nodes. Data values are sampled by the registers on the falling edge of the clock. Register delay is overlapped with the subsequent precharge phase of the dynamic combinational circuits.

VI. SELF-TIMED IMPLEMENTATION

In table.1 self timed implementation results are listed. While the average delays of the two micro pipeline stages referring to SPEC95 execution are

$$\text{Delay}_{avg1} = D_{bootenc} + D_{bootsel} + D_{ha} + \text{app. } (D_{fa} + D_{mux}) + 2 D_{mux}$$

$$\text{Delay}_{avg2} = D_{4:2} + E \{D_{epa}\} \sim D_{4:2} + 7D_{fa} + \text{pncp. } D_{mux} + (1 - \text{pncp.}) . 5D_{mux}$$

Table.1 Delay Characteristics Comparison

Parameters	Synchronous	Self-Timed
Delay I	1.65	1.65
Delay II	1.23	1.23
Pipe register	0.29	0.32
Pre charged hold time	0.40	0.40
Delay single cycle	1.83	0.76

VII. CONCLUSION

In this paper the architecture, logic design, and circuit implementation of variable latency multiplier architecture, which can be exploited in a synchronous design scheme as well as in an asynchronous one.

The proposed architecture and VLSI design demonstrate that a variable latency multiplier, in either synchronous or asynchronous implementations, can overcome the performance offered by fast fixed-latency multipliers. The proposed design explained the use of edge-triggered registers, to reduce the complexity of the register-overriding logic design in the synchronous implementation and of the interconnection routing in the self-timed implementation.

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