A Network Structure for Diagnosis of Four Types of Faults in Reed-Muller Canonical Circuits

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Abstract—In this paper, a new network structure and its associated universal test set, independent of the circuit function, and dependent only on the number of function variables, with good fault diagnosing capabilities have been proposed for single stuck-at, double stuck-at, AND-bridging and OR-bridging faults in Exclusive-OR Sum of Products (ESOP) Reed-Muller Canonical (RMC) circuits.

Keywords—Reed-Muller canonical; ESOP; stuck-at faults; bridging faults

I. INTRODUCTION

Logic networks are usually designed by using ‘AND’ and ‘OR’ gates. However, the networks using AND-EXOR gates have some advantages over the conventional AND-OR networks. In general, any arbitrary logic function can be expressed in Exclusive-OR Sum of Products (ESOP) Reed-Muller Canonical (RMC) form as, $F = a_0 \oplus a_1 x_1^* \oplus a_2 x_2^* \oplus \ldots \oplus a_n x_n^* \oplus a_{n+1} x_1^* x_2^* \oplus \ldots \oplus a_n x_1^* x_2^* \ldots x_n^*$ where, $x_n^*$ can be $x_n$ or its complement, $a_i$ is either 0 or 1 and $m = 2^n-1$. However, there can be variations in such forms. The different types are Fixed Polarity RMC (FPRM), Positive Polarity RMC (PPRM), Generalised RMC (GRM) and Exclusive-OR Sum-of-Products RMC (ESOP). The FPRM has a restriction that the variables in any of the product terms have to be of the same type namely complementary or non-complementary. For PPRM, the complementary form of variables is not allowed. The GRM may contain both complementary and non-complementary types but the combination of the variables should be unique. The ESOP form does not have any such restriction. Such networks often require fewer gates and interconnections than those designed using AND and OR gates. Second, they can be made easily testable. The ESOP form has the least number of product terms and hence needs the least number of AND gates and is very much suitable for hardware implementation. Examples of such networks include arithmetic, telecommunication and error correcting circuits.

II. LITERATURE SURVEY

A PPRM network for detection of stuck-at faults with a universal test set of size $n+4$, $n$ being the number of data inputs, was proposed in [1]. Though quite good for self-testing, the method is economical only for the specified form, which obviously has more number of product terms than the other forms in most cases. Multiple stuck-at fault detection for ESOP circuits was carried out in [2]. However, since the cardinality is $2n+6+\sum_{i=0}^{j} c_i$, where, $c_i = 0$ to $j$, the order of ESOP expression, the test set is not universal and also is too large to be practical for large input functions. Stuck-at and bridging faults with a universal test set for PPRM network has been reported in [3]. Multiple fault detecting GRM realizations was proposed in [4]. Reference [5] described an ESOP implementation with a universal test set of size $n+6$ for single stuck-at faults only. In [6] it was demonstrated that single stuck-at fault detection can be achieved with only $n+5$ test vectors. It was shown in [7] that $2n+s+3$ test vectors are required for single stuck-at fault detections in GRM / ESOP circuits while $2n+s$ vectors are required for detection of AND/OR-bridging faults in such circuits, where $s$ is the number of product terms in the logic function. Here too, the test set is not universal as it depends on $s$, the number of product terms of the function. References [8], [9] proved that a test sequence of length $2n+8$ vectors is sufficient to detect all single stuck-at and bridging faults. Two new methods, each with a small modification in this scheme with ESOP RMC circuits had been proposed for analysis and diagnosis of single stuck-at faults [10], [11]. In [12],[13],[14], it was demonstrated how the RMC forms help in the detection of various digital faults and how to determine the best polarity among them. It was proved that test vectors for multiple fault detection and diagnosis in digital circuits could be generated using Neural Network with different training algorithms [15]. Reference [16] proposed a new test pattern generation algorithm using Neural Network which requires additional gates. The analysis and diagnosis of OR-bridging faults in any of the pairs of data and control lines and OR-bridging faults including intermediate gate outputs of the ESOP RMC circuits was proposed in [17], [18].
In [19], a modification regarding auxiliary outputs of the network given by [6] was proposed for four types of faults namely single stuck-at, double stuck-at, AND-bridging and OR-bridging. The network structure and test set proposed by [6] was extended for double stuck-at, AND-bridging and OR-bridging types of faults [20]. It was proved by the authors that the same network structure with limited test set can be used for the other three types of faults also. The two auxiliary outputs of the structure in [20] were replaced by a single auxiliary output in [21] by the same authors. The simulation results were found to be much better than in [20].

The literature survey shows that research is being carried out for the past 45 years in the field of fault detection in digital circuits, especially with the network structure of Reed-Muller canonical form. Test vectors for determining various types of faults such as the basic single stuck-at, multiple stuck-at, bridging and stuck-open categories had been tried out with various modifications of the basic ESOP networks. The cardinality of the test vectors proposed by many authors become prohibitively excessive for a large number of input variables.

III. MATERIALS AND METHODS

A. Network Structure

The proposed network structure is shown in Figure 1. The complementary variables \( x_1', x_2' \ldots \) are represented as \( z_1, z_2, \ldots \) and serve as additional inputs. An AND block, an XOR function tree block which implements the required logic function \( F \) and also an additional output \( O \) obtained through a separate XOR gate are also present. The actual data inputs to the system are \( x_1, x_2 \ldots x_n \). Additionally, the scheme requires three control inputs \( c_1 \) to \( c_3 \) from which one of them is connected to each AND gate of the AND block as per the logic mentioned in a succeeding section. Finally, all the data inputs, complementary variable inputs present in the function and the control inputs are applied to a separate XOR gate producing the auxiliary output \( O \) to aid in the detection of faults which cannot be differentiated by the main function output \( F \) alone.

B. Test Vectors

The generalized test set for the proposed structure is shown in Table I. The test set has \((n+5)\) vectors; each of the vectors is \((n+nz+3)\) long, ‘n’ being the number of data inputs and ‘nz’ being the number of complementary variables.

The first three columns of the matrix represent the three control inputs \( c_1 \) to \( c_3 \), the next ‘n’ columns that of the data inputs \( x_1 \) to \( x_n \) followed by \( nz \) columns corresponding to the number of complementary inputs available in the function.

The test vectors are applied as the logic values of the input, complimentary and control variables; the resulting outputs \( F \) and \( O \) are converted to decimal values and tabulated for convenience and easy comparison.

![Generalized Proposed Network](http://www.ijritcc.org)

**Figure 1.** Generalized Proposed Network.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>GENERALIZED TEST SET</th>
</tr>
</thead>
<tbody>
<tr>
<td>( c_1 )</td>
<td>( c_2 )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
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<tr>
<td>1</td>
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<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
C. Control Signal Assignment

The assignment of control signals for the network is represented in Figure 2.

![Control Signal Assignment](image)

Figure 2. Control Signal Assignment

The algorithm for assigning the control lines is as follows:

**Step 1:** Draw the circuit for the required function.

**Step 2:** Assign the numerals 1, 2 and 3 respectively to the two inputs and the output of the final XOR gate producing the function output F.

**Step 3:** Consider each XOR gate connected to the inputs of the final XOR gate considered in **Step 2**. Assign the outputs of these XOR gates with the same numerals as the inputs of the final XOR gate of **Step 2**.

**Step 4:** If the output of the XOR gate considered is 1, then assign 2 and 3 to its inputs; else if the output is numbered 2, assign 3 and 1 to its inputs.

**Step 5:** Consider the next earlier input stage and assign the same numerals as the output points connected from the previous steps.

**Step 6:** Assign cyclic numerals as discussed in previous steps.

**Step 7:** Repeat until the basic input stage of the XOR gate tree is reached.

The numerals indexing this input stage incremented by 1 indicates the cardinality of the control line to be connected to the AND gate block.

D. Algorithm for Fault Diagnosis

**Step 1:** Set up the circuit as in Figure 1.

**Step 2:** Connect the control lines c₁ to c₃ as explained in the preceding section.

**Step 3:** Apply the test vectors as given in the Table 1, one by one.

**Step 4:** For each test vector applied, determine the three fault-free outputs F and O.

**Step 5:** Simulate the single stuck-at type of fault and determine the corresponding outputs F and O.

**Step 6:** Compare the sets of outputs with the predetermined fault-free outputs.

If the two output sets match exactly, it implies that a fault, if present, is not identifiable or detectable; else, the fault is a detectable one.

**Step 7:** Repeat **Steps 4 to 6** for all inputs and outputs of all gated except those auxiliary outputs, which is assumed to be fault-free.

**Step 8:** Repeat **Steps 4 to 7** for Double stuck-at, OR-bridging and AND-bridging faults for other possible combination pairs of control inputs, data inputs and intermediate gate outputs in the network.

E. Identifiability and Distinguishability Factors

For all the faults, the identifiability factor and distinguishability factor are calculated as explained below.

**Step 1:** The set of Boolean outputs (Main and auxiliary) for each test vector is determined for the given circuit assuming it to be fault free.

**Step 2:** The output Boolean vectors are each considered separately and their decimal equivalents are determined by standard binary to decimal conversion process.

**Step 3:** The above two **Steps** are repeated for single stuck-at faults at various locations of the circuit.

**Step 4:** The total number of faults for which the decimal equivalents of the outputs sets are identical to the output set of the fault-free operation is counted.

**Step 5:** The total number of possible faults is determined from a knowledge of input and output points including intermediate gates of the circuit.

**Step 6:** The ratio in percentage of the total number of faults obtained in **Step 4** to the total number of possible faults as known in **Step 5** gives a measure of the unidentifiable faults, from which the identifiability factor can be determined.

**Step 7:** The number of total faults for which the decimal equivalents of the output sets F and O are different from the fault-free output sets are counted.

**Step 8:** The ratio of the number counted in **Step 7** to the total number of possible faults is the indistinguishability index.

**Step 9:** The distinguishability factor is determined by subtracting the percentage indistinguishability from 100%.

IV. FUNCTIONS CONSIDERED FOR SIMULATION

The following ten random functions F₁ to F₁₀ have been considered and simulated for two reference structures and the proposed structure using MATLAB coding for Single-stuck-at, Double-stuck-at, AND-bridging and OR-bridging faults:

\[
\begin{align*}
F₁ &= x₁ \oplus x₂x₃ \oplus x₁'x₂x₃ \\
F₂ &= x₁x₄ \oplus x₂x₄ \oplus x₃x₄ \oplus x₁x₂x₃ \\
F₃ &= x₁' \oplus x₂x₃'x₄ \oplus x₃x₄' \oplus x₂'x₃ \oplus x₁x₂x₃ \\
F₄ &= x₁x₂' \oplus x₂x₃x₄' \oplus x₃x₄ \oplus x₂x₃ \oplus x₂'x₃' \oplus x₃'x₂x₄ \oplus x₄x₆ \\
\end{align*}
\]
\[ F_5 = x_1 \oplus x_2 x_3 \oplus x_4 x_5 x_6 \oplus x_4 ' x_3 x_7 x_8 \]
\[ F_6 = x_1 x_2 x_3' \oplus x_4 ' x_6 x_7' \oplus x_8 x_9 \oplus x_1' x_3 x_4' x_5 x_6' \]
\[ F_7 = x_1 x_2 x_3' \oplus x_4 x_5 x_6' \oplus x_7 x_8 x_9 x_1' x_3 x_4' \oplus x_2 x_3' \oplus x_3 x_5 \]
\[ F_8 = x_1 x_3 x_5' \oplus x_4' x_5 x_6' x_7 x_8' \oplus x_10 x_6 x_7' x_8 x_{10} \]
\[ F_9 = x_1' x_2' x_3' x_5' \oplus x_5' x_6 x_7' \oplus x_8 x_{10} x_{11} \oplus x_1' x_2 x_3 x_9 \]

\[ F_{10} = x_1 x_2 x_4 x_5 x_6 x_7 x_8 x_{10} x_{11} \oplus x_1 x_2 x_3' \oplus x_4 x_7 \]

Table II shows some of the features of the reference and proposed network structures.

<table>
<thead>
<tr>
<th>Network Structures</th>
<th>No. of Control lines</th>
<th>No. of Outputs</th>
<th>No. of Inputs for Auxiliary output(s)</th>
<th>No. of Test Vectors</th>
<th>Length of Test Vectors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference Structure 1 [6]</td>
<td>4</td>
<td>1</td>
<td>2</td>
<td>n+nzl</td>
<td>n+5</td>
</tr>
<tr>
<td>Reference Structure 2 [21]</td>
<td>3</td>
<td>1</td>
<td>1</td>
<td>n+nzl</td>
<td>n+5</td>
</tr>
<tr>
<td>Proposed Structure</td>
<td>3</td>
<td>1</td>
<td>1</td>
<td>n+nzl+3</td>
<td>n+5</td>
</tr>
</tbody>
</table>

where \( n \) is the number of data inputs
\( nzl \) is the number of complementary inputs

V. NUMERICAL ILLUSTRATION

The function \( F_1 = x_1 \oplus x_2 x_3 \oplus x_1' x_2 x_3 \) having three variables is taken as an example for numerical illustration.

In addition to the given data and control inputs, there is an additional data input \( z_1 \), which differs from the data input \( x_1 \) only in the last test vector.

The main function output expression is given by
\[ F = c_2 x_1 \oplus c_3 x_1 x_3 \oplus c_2 x_1' x_3 x_5. \]

There is one auxiliary output \( O \) having the logic expression
\[ x_1 \oplus x_2 \oplus x_3 \oplus c_1 \oplus c_2 \oplus c_3 \oplus z_1. \]

A. Single Stuck-at Faults

The total number of possible single stuck-at faults is,
\[ 2^{n+nc+nzl+nza+nzx} = (3+3+1+3+2) = 2^{12} = 24. \]

where, \( n \) is the number of data inputs = 3
\( nc \) is the number of control inputs = 3
\( nzl \) is the number of complementary inputs = 1
\( nza \) is the number of AND gate outputs = 3
\( nzx \) is the number of XOR gate outputs = 2

B. Double Stuck-at Faults

Double stuck-at faults can occur easily due to the shorting of any two of the lines, especially the adjacent lines of the circuit.

The network structure and test vectors are the same as those for the single stuck-at fault. However, in the test procedure, two lines at a time have been considered and made as stuck-at-0 or stuck-at-1 and simulated. Since two lines are involved, four possible combinations, viz. (0,0), (0,1), (1,0) and (1,1) for each pair of lines including the data lines, the control lines, the intermediate gates and the output.

The total number of fault location pair combinations is \( 4^* (n+nc+nzl+nza+nzx) C_2 = 4^*12C_2 = 264. \)

C. AND-Bridging Faults

The bridging faults are considered as a special case of multiple faults. In an AND-bridging fault, all the lines involved in the fault have the same post-fault values as the logical ANDing of their pre-fault values. In the present research, only two lines are assumed to be faulted at a time and of non-feedback type. Unlike the double fault, this type has only one combination of logical ANDing of pre-fault values. Hence, the number of fault possibilities is \( 1/4 \) of the double fault case = (\( n+nc+nzl+nza+nzx \)) \( C_2 / 4 = 66. \)

D. OR-Bridging Faults

In an OR-bridging fault, all the lines involved in the fault have the same post-fault values as the logical ORing of their pre-fault values. In the present research, only two lines are assumed to be faulted at a time and of non-feedback type. The total number of fault possibilities is \( (n+nc+nzl+nza+nzx)C_2 / 4 = 66. \)

The fault-free outputs and the total number of fault possibilities in the proposed network structure for the four types of faults mentioned above is shown in Table III.
Inference: The identifiability as well as the distinguishability for all the ten random functions considered are 100%. Hence single stuck-at fault in any of the input lines, control lines, output lines or the intermediate gate lines is completely identifiable by the proposed method.

VI. SIMULATION RESULTS

Adopting the algorithms outlined in previous sections, the percentage identifiability and distinguishability are determined for the four types of faults in the circuits for ten functions mentioned above, the simulation results are shown in Tables IV to VII as also the respective inferences.

TABLE IV. CONSOLIDATED IDENTIFIABILITY AND DISTINGUISHABILITY FACTORS FOR SINGLE STUCK-AT FAULTS IN THE REFERENCE AND PROPOSED STRUCTURES

<table>
<thead>
<tr>
<th>F</th>
<th>O</th>
<th>% Identifiability</th>
<th>% Distinguishability</th>
</tr>
</thead>
<tbody>
<tr>
<td>F1</td>
<td>84.62</td>
<td>83.33</td>
<td>100</td>
</tr>
<tr>
<td>F2</td>
<td>97.06</td>
<td>96.88</td>
<td>100</td>
</tr>
<tr>
<td>F3</td>
<td>95.45</td>
<td>95.24</td>
<td>100</td>
</tr>
<tr>
<td>F4</td>
<td>96.30</td>
<td>96.15</td>
<td>100</td>
</tr>
<tr>
<td>F5</td>
<td>97.62</td>
<td>97.50</td>
<td>100</td>
</tr>
<tr>
<td>F6</td>
<td>96.34</td>
<td>96.25</td>
<td>100</td>
</tr>
<tr>
<td>F7</td>
<td>98.39</td>
<td>98.33</td>
<td>100</td>
</tr>
<tr>
<td>F8</td>
<td>98.44</td>
<td>98.39</td>
<td>100</td>
</tr>
<tr>
<td>F9</td>
<td>98.39</td>
<td>98.33</td>
<td>100</td>
</tr>
<tr>
<td>F10</td>
<td>98.44</td>
<td>98.39</td>
<td>100</td>
</tr>
<tr>
<td>Averag e</td>
<td>96.11</td>
<td>95.88</td>
<td>100</td>
</tr>
</tbody>
</table>

Inference: The fault detection is very close to 100% on an average, for the functions considered. The proposed method also has shown an improvement in distinguishability by about 94% compared to the Structure[6] and by about 11% over the Structure[21].
TABLE VII. CONSOLIDATED IDENTIFIABILITY AND DISTINGUISHABILITY FACTORS FOR OR-BRIDGING FAULTS IN THE REFERENCE AND PROPOSED STRUCTURES

<table>
<thead>
<tr>
<th>Fn.</th>
<th>% Identifiability</th>
<th>% Distinguishability</th>
</tr>
</thead>
<tbody>
<tr>
<td>F1</td>
<td>84.62</td>
<td>84.85</td>
</tr>
<tr>
<td>F2</td>
<td>98.53</td>
<td>100</td>
</tr>
<tr>
<td>F3</td>
<td>96.54</td>
<td>98.10</td>
</tr>
<tr>
<td>F4</td>
<td>96.58</td>
<td>99.08</td>
</tr>
<tr>
<td>F5</td>
<td>98.57</td>
<td>100</td>
</tr>
<tr>
<td>F6</td>
<td>98.29</td>
<td>99.62</td>
</tr>
<tr>
<td>F7</td>
<td>98.28</td>
<td>100</td>
</tr>
<tr>
<td>F8</td>
<td>98.59</td>
<td>100</td>
</tr>
<tr>
<td>F9</td>
<td>98.71</td>
<td>99.77</td>
</tr>
<tr>
<td>F10</td>
<td>98.79</td>
<td>100</td>
</tr>
<tr>
<td>Averag e</td>
<td>96.75</td>
<td>98.14</td>
</tr>
</tbody>
</table>

Inference: The fault detection is closer to 100% than the other two network structures compared, on an average. The proposed method also has shown an improvement in distinguishability by about 17% compared to the Structure[6] and by about 12% over the Structure[21] for the functions considered.

Summary: From the simulation results presented above, it can be seen that the proposed structure outperforms the other two structures in both the identifiability as well as distinguishability for all the four types of faults considered. The role of the control function in a network aiding in the identification and distinguishing the fault is highlighted from the test results. Here, all the lines viz. input lines, output lines and intermediate gate output lines are considered in fault simulations.

VII. CONCLUSION
In this paper, a new network structure and its associated universal test set, independent of the circuit function, and dependent only on the number of function variables, with good fault diagnosing capabilities have been proposed for single stuck-at, double stuck-at, AND-bridging and OR-bridging faults in ESOP RMC circuits.

For stuck-at faults, a line has been assumed to be either stuck-at-0 or stuck-at-1 at a time. For double stuck-at faults, only two lines have been assumed to be involved at a time. However, the two lines can be any pair of lines involved. The bridging faults have been assumed to be of single (involving only one pair of lines at a time) and of non-feedback type. Tree type EXOR function block has been assumed for the reduction of propagation delay. The gates of auxiliary output are assumed to be fault-free.

All the primary input lines, primary output line and all the inputs and outputs of the various gates of the circuit have been considered for the simulation of the various types of faults considered.

The analysis and diagnosis of the various types of faults have been performed through the use of two quantification indices. Ten random ESOP RMC functions from three to twelve variables have been simulated in MATLAB and compared for fault detection capability. A result compaction technique has been used for the ease of tabulation and comparison of the results.

The identifiability factor, is almost 100% for all the functions considered randomly and the distinguishability factor also has improved very much compared to the reference structures. The tabulated distinguishability factor is an overall value. Though the overall factor may be poor in some cases, its value for an individual output set is much higher. Further, the detection capability is not affected by this factor. It is also easy to identify the actual faulty line from the set of outputs measured.

REFERENCES


[16] Zhao Ying and Li Yanjuan, “A Multiple Faults Test Generation Algorithm Based on Neural Networks and Chaotic Searching For Digital Circuits”, International Conference on Computational Intelligence and Software Engineering (CISE), December 2010.


