International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169
Volume: 4 Issue: 6 212 - 213

Low Voltage and High Performance Constant Current Source using 90nm CMOStechnology

Menka Zankyani
Electronics and Telecommunication
SSTC/SSGI, Bhilai(C.G.),India
Email Id: menka.zankyani18@gmail.com

***Abstract*—** This paper proposed a self-biasing constantcurrent source circuit which is suitable for analog integrated and mixed mode circuits.A low input resistance, high output resistance and high gain current source is proposed. This current source circuit is designed by using five n-type and two p-type MOSFETs. Simulation is performed with 90nm digital CMOS technology.Accuracy and gainare the most important parameters to observe the performance of the Current Source. This current source is operated at 0.8V supply voltage.

***Keywords*—** *Constant Current Source; CMOS; Low voltage*

*****

I. INTRODUCTION

As the need for portable and wireless devices is increasing the designers are now more focused towards circuits with low power consumption and enhanced bandwidth. We require low voltage current source for low voltage applications. Area minimization is also an important task to perform in order to achieve reduction in the size of silicon chip. Recently supply voltage and threshold voltage requirements are diminishing very speedily. Low voltage application refers to the low input and output voltage as well as low supply voltage requirements. Constant current can be used to generate a constant current which is independent of the voltage across it. It is necessary to create chips of small size, using low power and lesser area consumptionto move with the rapid developments.Constant current source can be used to generate a constant current which is independent of the voltage across it. The preceding sections include contents are as follows: literature review, proposed current source, result of the proposed circuit and conclusion respectively.

II. LITERATURE REVIEW

Some current mirror circuits have been reported in [1-5]. Kuo-Hsing Cheng [1] proposed a current mirror whose performance better than a regulated cascade current mirror. It uses a reference current of 160µA. Manish Tikyani [2] has proposed a current mirror using four p-type and five n-type MOSFET. This circuit is designed with supply voltage of 1.3V. Houda bdiri gabbouj [3] has been proposed a low voltage current mirror which provides low input impedance high output impedance with high performance. A. Torralba [4]

has proposed a low voltage high performance current mirror using CMOS technology which provides bandwidth in the range of hundreds MHz. J. Ramirez-Angulo [5] has proposed a Low supply voltage high performance CMOS current mirror with low input and output voltage requirements" which is designed with 0.15V input and output voltage requirements, 40MHz bandwidth, 100Ω input resistance and 200MΩ output resistance.

III. PROPOSED CURRENT SOURCE

Constant current source is a source of power which provides a constant current for a load even if the load resistance value is changed. For low voltage application it is mandatory to use the

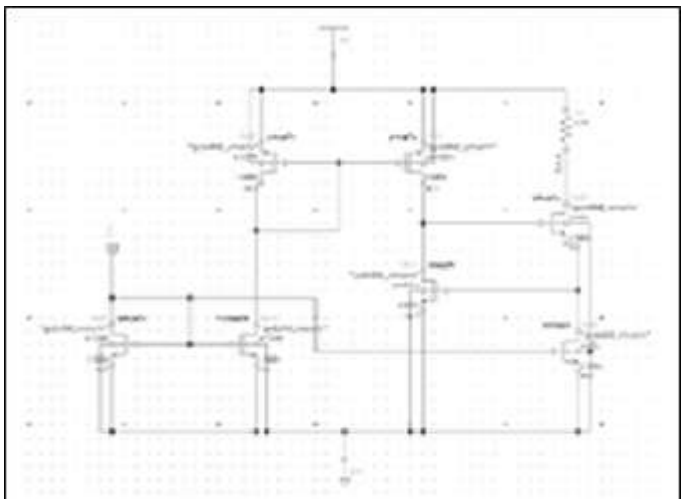

Fig.1. Low voltage constant current source

low voltage current source. Current source can be used in biasing and loading of a circuit. Most of the applications of a current source are found in the field of biasing. When we use a constant current source for the purpose of loading then the circuit would be insensitive to temperature. At output stage cascading of transistors is performed to achieve enhanced output impedance. Higher output impedance is achieved by using regulated cascode current mirror as compared to Wilson current mirror. This circuit is advantageous because it doesn't require any bias current at the input side. A stable current is achieved at the output of this circuit. In the proposed circuit negative feedback is provided used to stabilize the output current. Transistor MN2 is biased by the transistors MN0 and MN4. For biasing of PM0 we use transistor PM1. Thus we can say that the circuit is self-biased i.e. no external biasing voltage or current is applied to the current source. Self-biasing is done because if input current is too large then the device may get short circuited. Negative feedback is applied through

the transistors MN1 and MN2 to achieve stabilized current in the circuit. Input impedance of this circuit is given as

$$R_{in} = r_0 \quad (1)$$

Output impedance of the circuit is given by

$$R_{out} = \frac{g_m{}^2 r_0{}^3}{2} (2)$$

An Amplifier circuit is used at the output to enhance the gain of the current source. Settling time of a current source proves significant parameter to enhance the performance of the current source circuit. For high speed applications the settling time of the circuit should be as low as possible. The proposed circuit should also be able to operate at the high frequencies.

IV. Transistor Sizes

The aspect ratio of transistor used for designing the constant current source is given in TABLE I.

TABLE I. Transistor Sizes

Transistor	W/L ratio
MN0	180n/100n
MN1	4.5u/100n
MN2	6u/100n
MN3	5u/100n
MN4	120n/100n
MN5	120n/100n
MN6	450n/100n
PM0	120n/100n
PM1	120n/100n

V. Result and Discussion

The simulated result of proposed constant current source is given below. A low voltage current source circuit has been designed and simulated using Cadence EDA tool. This circuit is simulated with 90nm digital CMOS technology. Threshold voltages for PMOS and NMOS are 0.135V and 0.169V respectively. A load resistor of 1kΩ with the supply voltage of 0.8v is used for simulation. Transistor sizes of the proposed current source are reduced for reduction in silicon chip area of the circuit. A dc sweep of the input current is performed for a range of 0u to 100u. Power consumption of the circuit is reduced. All the results are obtained at the room temperature i.e. 27˚C.For AC analysis sinusoidal input is taken with frequency 1kHz.This circuit satisfied all the constraints i.e. area, speed, power of the analog integrated and mixed mode circuits.

TABLE II. Simulated Results

Parameter	Value
Supply voltage	0.8 V
Input current	50 µA
Bandwidth	9MHz
Gain	32dB

The dc sweep plot of this work is shown below.

Fig.3. dc sweep plot

VI. Conclusion

A low voltage high performance constant current source has been designed using CMOS 90nm technology. Cadence virtuoso EDA tool is used for simulation of the proposed current source. This proposed current source circuit is very efficient in terms of area, power consumption and speed.

Acknowledgment

With a deep sense of gratitude I am thankful of Ms. Jayashree for sharing his best of knowledge with me and providing a great approach to perform my task in a better way.

References

[1] Kuo-Hsing Cheng, Tsung-Shen Chen, and Ching-Wen Kuo "High accuracy current mirror with low settling time" 0-7803-8294-3/04

[2] Manish Tikyani and Rishikesh pandey "A new low voltage current mirror circuit with enhanced bandwidth" DOI 10.1109/CICN.2011.9

[3] Houda BDIRI GABBOUJ, Nejib HASSEN, Kamel BESBES "Low supply voltage high speed CMOS current mirror for analog design" IEEE ICM-December 2007

[4] A. Torralba, R.G. Carvajal, F. Munoz and J. Ramirez-Angulo"New output stage for low supply voltage, high performance CMOS current mirror"0- 7803-7761-3/03 IEEE 2007

[5] J. Ramirez-Angulo, R.G. Carvajal, A. Toralba"Low supply voltage high performance CMOS current mirror with low input and output voltage requirements" IEEE Transactions on circuits and systems-II Express Briefs, Vol. 51, No.3,March 2004.

[6] P. E. Allen and Holberg, *CMOS Analog Ckt. Design*, Oxford University, second edition, 2007.

[7] B.Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw Hill Companies,2002.