

Design of High Performance CMOS Comparator using 90nm Technology

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Abstract— In many digital circuits the parameters gain and offset voltage are calculated. In our design of CMOS comparator with high performance using GPDK 90nm technology we optimize these parameters. The gain is calculated in AC analysis and also we measure area, delay, power dissipation, slew rate, rise time, fall time. The circuit is built by using PMOS and NMOS transistor with a body effect and we also measure mobility variation and channel length modulation based on the second order channel effects. A plot of gain and offset voltage also discussed in the paper. Finally a test schematic is built and transient analysis for a input voltage of 1.2V is measured using Cadence virtuoso.

Keywords- CMOS Comparator, Offset voltage, Gain, cadence virtuoso, slew rate

INTRODUCTION

In ADCs, the comparator plays a main role on the overall performance. An accurate and fast comparator is a key element in any high-resolution and high speed data converter. As compared to other ADCs, pipelined ADC has merit of high speed, good precision and low power dissipation. Depending on the algorithm use, encoding process can often be pipelined with the comparator function. Since the encoding process is faster than the comparator function, the maximum conversion rate for the ADC is limited by the response time of its comparators. Therefore, the design and optimization of the comparators is critically important. The comparator is basically excluded from application to the high speed A/D converters with high resolution owing to its large offset voltage which significantly affects the resolution. As a consequence, the preamplifier-latch comparator topology in which an amplifier is added before a latched comparator, aiming at achieving small offset voltage and high speed, has been developed. The preamplifier latch comparator, which combines an amplifier and a latch comparator can obtain high speed and low power dissipation. Thus, by considering factors of speed and power dissipation, preamplifier latch comparator is the choice for a pipeline ADC.

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. The comparator is widely used in the process of converting analog signal to digital signals. In the analog to digital conversion process, it is necessary to first sample the input, this sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. If the positive input voltage of the comparator is at a greater potential than the negative input voltage the output of the comparator is a logic 1, where as if the input positive voltage is at a potential less than the negative input voltage, the output of the comparator is at logic 0. In pipeline A/D converter, internal comparator must amplify small voltage into logic levels, basic comparator circuit shown in figure 1.

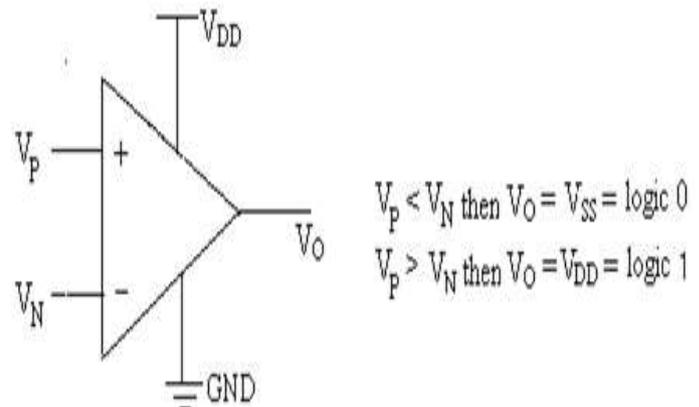


Fig 1- Basic Comparator Circuit

In the proposed design pre-amplifier circuit that amplifies very weak signal it is considered to be the input stage of the proposed comparator. Latch stage is used to determine which of the input signal is larger and amplifies their difference. Clock is used to indicate output level; whether its differential input signal is positive or negative. In order to provide maximum offset voltage we provide reference voltage to the circuit. Output buffer stage is used to convert the output of the latch stage circuit into a logic signal.

RELATED WORK

Behzad Razavi and Bruce.A.Wooley Described precision techniques for the design of comparator used in high performance Analog-Digital converters employing parallel conversion stage. Here introduced a number of comparator techniques for use in parallel Analog-Digital converters that are implemented in BiCMOS and CMOS VLSI technologies [1].

Lauri sumanen, Mikko Walteri, Kari halonen Described and proposed a new fully differential CMOS dynamic comparator topology suitable for pipeline A/D converters with low stage resolution .Here proposed topology, based on switchable

current sources, has a small power and area dissipation. The main benefits of the pipeline A/D converter architecture are its capability to a high resolution and very high bandwidth with low power consumption in a small area [2].

R.Lotfi, M.Taherzadev-sami, M.Yaser Azizi and O.Shoeai, Describe a 1-V fully differential low power MOSFET only comparator with rail-to-rail input swing is presented which can be suitably used in very low voltage, low power pipelined A/D converters. This comparator utilizes a resistive divider configuration with a MOSFET only clock booster to supply a higher voltage for the dynamic latch in the intervals that a comparison is to be made [3].

M.B.Gnermaz,L.Bouzerara.A.Slimane,M.T.Belaroussi, B.Lehoudj and R.Zirmi describes and analyzes a low power and high speed differential comparator. This comparator is based on the switched capacitor network using a two phase nano overlapping clock. The offset voltage of the designed comparator has been reduced by means of an positive feedback. Here presented clocked comparator circuit which consist of a pre amplification stage followed by a positive feedback stage forming the latch [6].

Riyan Wang , Kaichang Li, Jianquin Zhang, Bin Nie presented a high speed and high resolution comparator intended to be implemented in a 12 bit 100MHz pipeline analog to digital converter for frequency wireless local area network application. Here the designed comparator presents a rail-rail input range pre amplifier without any capacitance required [5].

Anand Mohan, Aladin Zayegh , Alex Stojceski, and Ronny Veljanovski , Presented the design and implementation of a high speed, low power CMOS comparator as part of an ultra fast reconfigurable flash analog to digital converter for a direct sequence, spread spectrum based ultra wide band radio receiver. Here Ultra means of communication has been around for decades [7].

DESIGN AND ANALYSIS

In the pre-amplifier stage input voltage $V_{in}=1.2$ V we get an amplified output also we include transconductance g_m in the circuit. In the preamplifier stage $I_{dc}=10\mu A$ because of drain saturation current the preamplifier works in saturation region, where $V_{ds}= \beta/2 (V_{gs}-V_t)$. By using a clock and providing offset voltage from the clock the output of the preamplifier stage compares both input voltages V_{in+} and V_{in-} and produce an output same as $V_{in+} - V_{in-}$. The substrate terminal of PMOS connected to V_{dd} and substrate terminal of NMOS are connected to the ground. $V_{in+} =1.2$ V provides an input voltage to the NMOS transistor and result in an output voltage which is the difference between V_{in-} . The preamplifier circuit also acts as a current mirror circuit two PMOS and 2 NMOS transistor we use a clock circuit to provide a dc offset voltage.

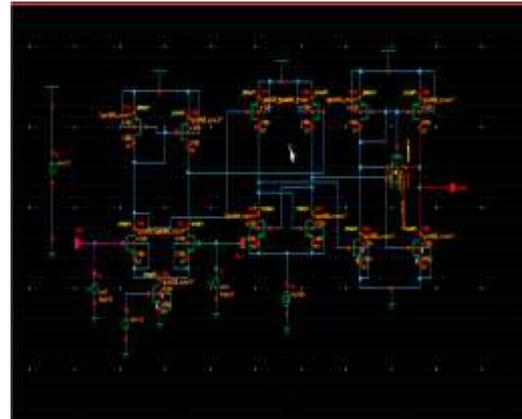


Fig 2 Schematic diagram of CMOS comparator

In the latch circuit the PMOS and NMOS circuits are connected in antiparallel which found a common source stage usually in the latch circuit the output of the preamplifier is taken as the input for two PMOS transistor when clock is high the comparator starts to work during this operation the common source stage produces the transconductance g_m which approximately equal to $1/\beta$. The gate of the NMOS transistor are connected to the drain of the PMOS transistor which reduces the second order effects such as channel length modulation, body effect, and mobility variation also in this stage the feedback is given to the preamplifier stage which reduces the noise from the signal.

In the output buffer stage we supply clock frequency of 100MHz which reduces the offset voltage in terms of mill volts. The power dissipation which include static and dynamic power dissipation are calculated from the output buffer stage. Finally an amplified output is obtained from the output buffer stage which is free of noise variations.

We also calculate slew rate, area, power dissipation, delay, rise time, fall time, offset voltage and gain of the comparator.

RESULT AND DISCUSSIONS

From the proposed design of high speed CMOS comparator, designed using cadence virtuso with GPDK 90nm technology is discussed below.

The transient analysis for CMOS comparator is obtained and the input voltage $V_{in}=1.2V$ is given below

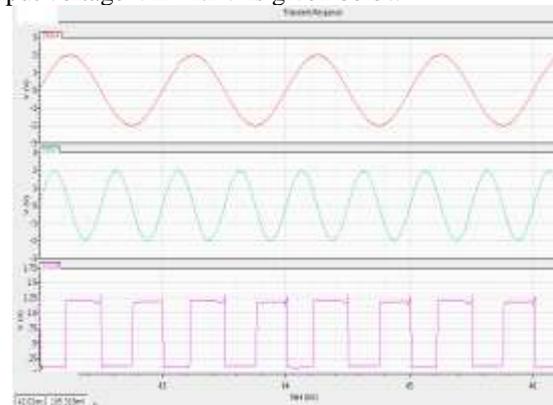


Fig 3: Transient Analysis of CMOS comparator

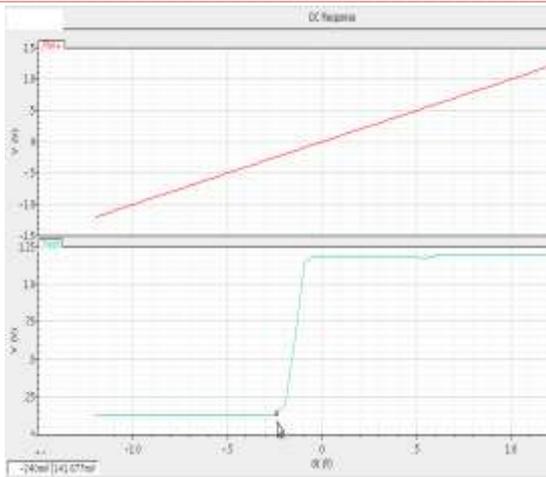


Fig 4: Offset voltage of a comparator

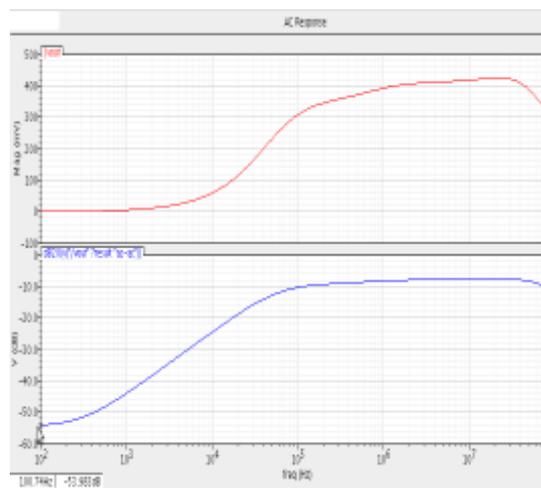


Fig 5 : Gain of the comparator

Next we consider the design of slew rate, rise time, fall time, power dissipation, delay, gain, offset voltage, and area calculations in the below table 1

Parameter	Value
Power supply	1.2 V
Power dissipation	360 μ W
Offset voltage	292.3 μ sec
Delay	2.272 μ sec
Rise time	2.727 μ sec
Fall time	363.7 kV/sec
Area	180fsqm
Technology	90nm
Gain	53.98db

CONCLUSION

In this work we proposed a high performance CMOS comparator with low offset voltage with high gain. The CMOS comparator will work in 90nm technology and results are discussed. The proposed CMOS comparator will operate at a power supply of 1.2V with offset voltage 192mV and power dissipation 1.2mW also we have carried out an output buffer stage for CMOS comparator in this stage the glitches present in the circuit are reduced. The objective has been achieved that

is the proposed design of CMOS comparator as produced a low offset voltage and low power dissipation.

FUTURE SCOPE

The main scope of future work in CMOS comparator is that we have to reduce the circuit area which is one of the important constraints in any VLSI design. The comparator converts analog signal to digital signal with a high sampling frequency. In future both area and time should be reduced so that an external circuit can be built which should reduce the both constraints.

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