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Review on FM0/Manchester encoder-decoder used in DSRC based Applications

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Abstract:-DSRC is an emerging technique that plays an important role in sensor networking for intelligent transportation and many other a system applications. The DSRC standards generally adopt FM0 and Manchester codes to reach dc-balance, enhancing the signal reliability In this review, the theoretical backgrounds of FM0/Manchester and how it can be used for DSRC will be discussed.

Keywords: *DSRC, FM0 code, Manchester code.*

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I. INTRODUCTION

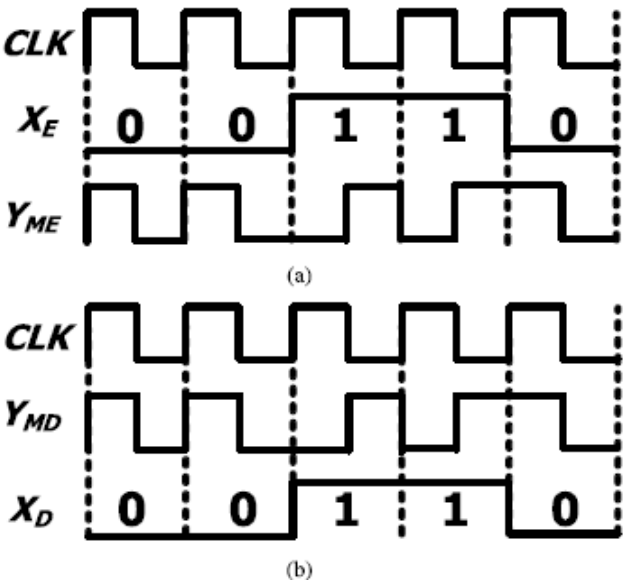
Dedicated short-range communication for one- or two- way communication .DSRC is basically wireless communication. It is basically designed for automotive
Sensor techniques play an vital role in intelligent transportation systems especially for urban traffic scenario. There are lots of urban traffic issues such as driver safety, traffic management, smart cities, traffic Optimization and parking applications. All above issues are associated with wireless sensor network. There is a requirement to provide links among infrastructures, vehicles and sensor nodes in wireless manner. DSRC can provide this links. DSRC builds up links among vehicles to exchange the information from in-car sensors and provides collision warning and autonomous system for inter-vehicle communication. DSRC transmit the information of local navigation sensors for relative positioning enhancement. Along with sensor informationDSRC can be utilize for developing map free intersection collision warning system. DSRC along with WSN and VANETs is widely used in ITS application.

DSRC basically consist of two basic units : on-board unit and roadside unit, OBU basically consist of sensor node and the RSU act as a data collection centre to collect information. DSRC forms a wireless communication between the two units. DSRC supports half duplex communication for OBU. This indicates OBU activates either transmitting or receiving function one at a time. If transmission and receiving function both can be operated through single hardware. The hardware efficiency of the circuit can be used greatly.

DSRC system consist of three parts : 1) microprocessor 2) Baseband processing and 3) Radio frequency. The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end. The baseband processing is responsible for modulation, error correction, clock synchronization, and encoding. The RF frontend transmits and receives the wireless signal through the antenna. Data coding is the part of base band processing. Data coding consists of NRZI,FM0 and Manchester. Data coding is classified into two parts : full cycle based coding and half cycle based coding. Full cycle based coding can be defined has 1-bit data that has steady signal in a cycle with no transition. NRZI is the example of a steady state signal or full cycle based signal. Full cycle based coding is processed cycle by cycle. Half cycle based coding can be defined has 1-bit data signal that has transition in a cycle. FM0 and Manchester is the example of a half cycle based coding signal. The 1-bit data is processed half cycle by half cycle. Full-cycle-based coding can be handled by general digital systems, where every digital data is also processed cycle by cycle .Half-cycle based coding with half-cycle processing is totally different from general digital systems.FM0 and Manchester provides dc balance and it enhances the signal reliability.

1. FM0/MANCHESTER ENCODING AND DECODING CONCEPT

1.1 MANCHESTER CONCEPT



(a) Manchester encoding (b) Manchester decoding

Manchester Encoding

Manchester encoding is also called phase encoding. Logic "1" represents the transition from HIGH to LOW. Logic "0" represents the transition from LOW to HIGH.

Manchester encoding is given by equation :

$$Y_{ME} = X_E \oplus CLK$$

According to above equation, YME must have a signal-transition in every cycle, whether XE is logic-1 or logic- 0.Due to this signal-transition, ac components are embedded into the YME, which can facilitate the synchronization in receiver. Manchester encoding is shown in figure (a).

Manchester Decoding

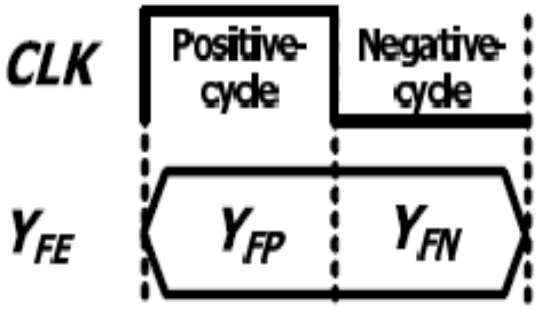
Manchester decoding is given by equation :

$$X_D = Y_{MD} \oplus CLK$$

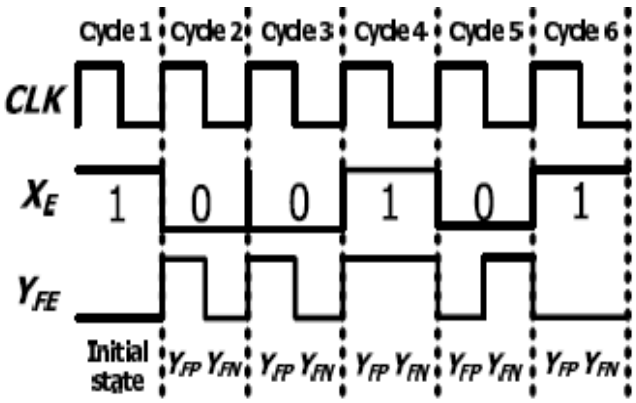
where XD stands for the decoded binary data, and the YMD denotes a Manchester codeword to be decoded. Manchester Decoding shown in figure (b).

1.2. FM0 CONCEPT

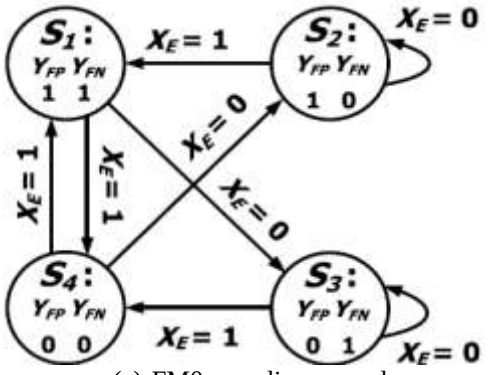
FM0 Encoding



(a) Structure of FM0 code



(b) Example of FM0 encoding



(c) FM0 encoding procedure

Previous state		Current sate			
		$X_E = 0$		$X_E = 1$	
$Y_{FP}(t-1)$	$Y_{FN}(t-1)$	$Y_{FP}(t)$	$Y_{FN}(t)$	$Y_{FP}(t)$	$Y_{FN}(t)$
0	0	1	0	1	1
0	1	0	1	0	0
1	0	1	0	1	1
1	1	0	1	0	0

(d) State transition table

FM0 is known as Bi-phase space encoding.FM0 code YFE is divided into two parts: YFP and YFN which represents FM0 code at positive-cycle and negative- cycle, respectively. The encoding procedure of FM0 code is given has follow:

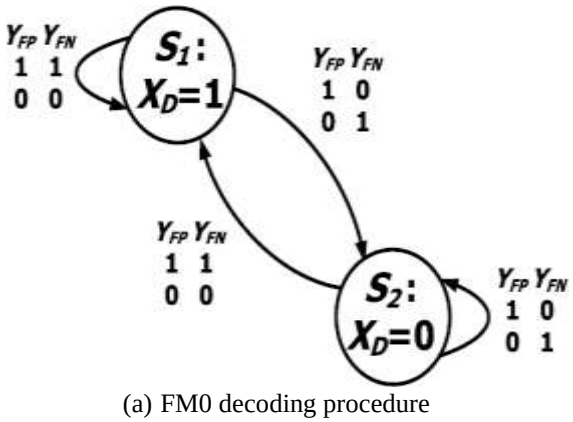
1) For the XE of logic-0, a signal transition is allocated between YFP and YFN.
2) For the XE of logic-1, no signal transition is allocated between YFP and YFN
3) A signal-transition exists among every YFE.

As shown in Table both YFP(t) and YFN(t) are three- variable Boolean functions of YFP(t − 1) YFN(t − 1), and XE With Boolean simplification, the YFE = {YFP(t), YFN (t)} is given as

$$Y_{FP}(t) = Y_{FN}(t-1)$$

$$Y_{FN}(t) = X_E \oplus Y_{FN}(t-1)$$

FM0 Decoding



(a) FM0 decoding procedure

Y_{FD}		X_D
$Y_{FP}(t)$	$Y_{FN}(t)$	
0	0	1
0	1	0
1	0	0
1	1	1

(b) Transition table of FM0 decoding

The FM0 codeword to be decoded is represented by Y_{FD}, which consists of Y_{FP} and Y_{FN}. The procedure of FM0 code is given as follows

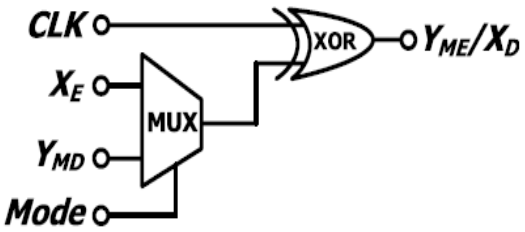
1) If a signal-transition exists between Y_{FP} and Y_{FN}, X_D is interpreted as logic-0.
2) If no signal-transition exists between Y_{FP} and Y_{FN}, X_D is interpreted as logic-1.
The logic value of X_D only depends on whether there is a signal-transition between Y_{FP} and Y_{FN}

As shown in Table, the state-transition table of FM0 decoding can be also conducted from the FSM of FM0 decoding The X_D is a Boolean function of $Y_{FD} = \{Y_{FP}(t), Y_{FN}(t)\}$ as

$$X_D = Y_{FP}(t) \odot Y_{FN}(t)$$

2. Hardware Architecture of Manchester Encoding/Decoding

Manchester Codec



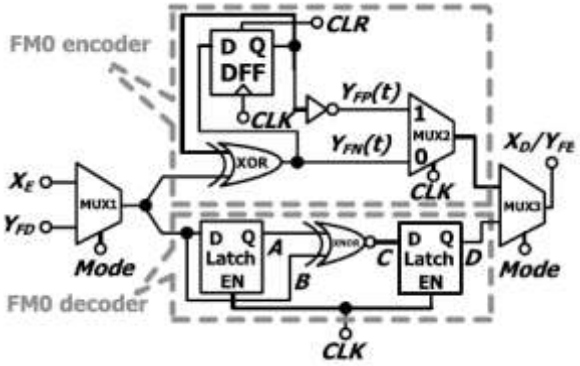
(a) Architecture of Manchester codec

The Hardware architecture of Manchester codec is as shown in figure. As shown in figure the Manchester Codec consist of two input XOR gate. One input is CLK and other is output from MUX. The Mode switches between the data paths of Manchester encoding and Manchester decoding by MUX. If Manchester encoding is adopted, X_E is passed through MUX to XOR, and the output of XOR represents Y_{ME}. If Manchester decoding is adopted, Y_{MD} is passed through MUX to XOR, and the output of XOR denotes X_D.

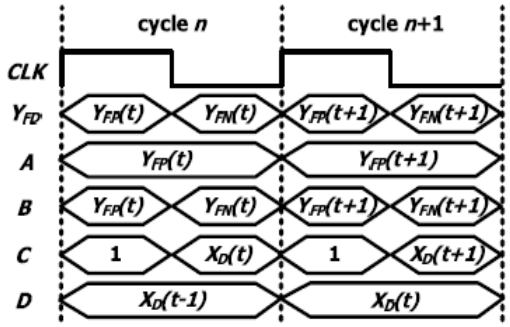
3. Hardware Architecture of FM0 Codec

FM0 Encoding

The Hardware architecture of FM0 codec is as shown in figure. This hardware architecture primarily consists of two parts: FM0 encoder and FM0 decoder. The CLR is active-low to reset the stored data in DFF to logic- 0.The EN is active-high enable signal of the latch, which is connected to CLK. The latch is non-transparent with the positive-edge of CLK but is transparent with the positive-level of CLK. The Mode indicates which part is activated and controls their input data paths and output data paths by MUX1 and MUX3, respectively. The MUX1 switches between XE and YFD for the input of FM0 encoder and that of FM0 decoder. The MUX3 switches between the output of FM0 encoder to YFE and that of FM0 decoder to XD. For FM0 encoding, the Boolean functions of YFP(t) and YFN(t) can be derived from (3) and (4), where, YFN(t −1) in (3) is stored in a flip-flop DFF. If CLK is at positive-cycle, YFP(t) is presented on the output of MUX2. If CLK is at negative-cycle, YFN(t) is presented on the output of MUX2. Then, a complete FM0 codeword is obtained from the output of MUX2.



(a) Hardware architecture of FM0 codec



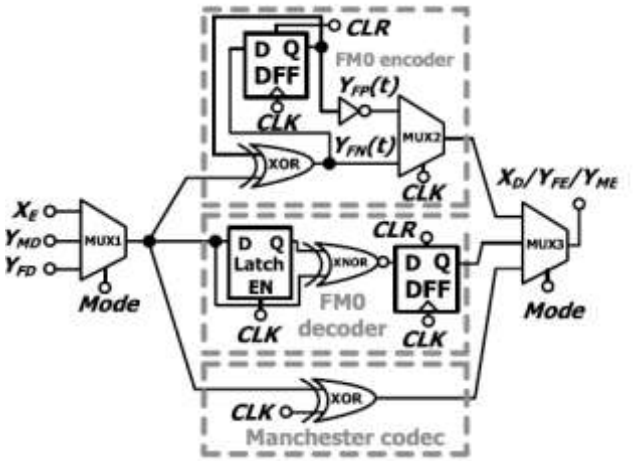
(b) Synchronization of FM0 decoder

FM0 Decoding

The FM0 decoder is responsible to convert YFD to XD. According to (5), XD can be derived from YFP(t) and YFN(t). However, YFP(t) and YFN(t) sequentially arrive with a half cycle latency between each other. This half cycle latency causes non synchronized input to XNOR gate causing logical fault on FM0 decoding. To solve this synchronization problem, a latch, which Is positive-level active, is allocated in FM0 decoder. Two inputs and the output of XNOR gate are marked as A, B, and C in Figure. The timing diagram of FM0 decoder is shown in figure. At cycle n, YFD sequentially presents YFP(t) and YFN(t) with a half-cycle latency through MUX1 to FM0 decoder. At the positive cycle n, YFP(t) is passed through the latch to A and also presented on B concurrently. Both inputs of XNOR are identical, and thereby the C is logic-1.At the negative-cycle n, YFP(t) is kept by the latch on A, and

YFN(t) is presented on B. Both YFP(t) and YFN(t) are synchronized on A and B at the negative-cycle n. XD(t) is presented on C; however, it is available only for a half- cycle. In order to hold this XD(t) for an entire cycle, a DFF is allocated after XNOR gate, and its output is referred to as D. The XD(t) of cycle n can be hold on D for an entire cycle n + 1. This FM0 decoder can convert YFD to XD with one-cycle latency

1. FM0/MANCHESTER ENCODING AND DECODING COMBINED HARDWARE



The hardware architectures are integrated into a FM0/Manchester codec, as illustrated in Fig..The Mode indicates which coding mode is activated by controlling MUX1 and MUX3. Nevertheless, this hardware architecture suffers from a serious limitation on hardware utilization. This hardware architecture is classified into three parts, including FM0 encoder, FM0 decoder, and Manchester codec. The OBU of half-duplex only activates one of three parts each time, and then the other two parts are idle. Suppose this hardware architecture is realized into a VLSI architecture with transmission gate (TG) circuit topology. This architecture consists of six kinds of logic components, including the XOR gate of 8 transistors, the XNOR gate of 8 transistors, the multiplexer of 6 transistors, the inverter of 2 transistors, the DFF of 22 transistors, and the latch of 10 transistors. This FM0/Manchester codec requires a total of 86 transistors, where FM0 encoder, FM0 decoder, and Manchester codec occupy 38 transistors, 40 transistors, and 8 transistors. Hence a technique is required that can optimize the circuit and allow to use the entire circuit at same instance of time.

II. Conclusions

DSRC can provide a wireless link for sensor networking in ITS applications and FMO/Manchester technique is used for t he DSRC application .It is half duplex communication. Use of FMO/Manchester provides DC-Stability and signal reliability in DSRC

References

[1] M. A. Kafi, Y. Challal, D. Djenouri, M. Doudou, A. Bouabdallah, and N. Badache, "A study of wireless sensor networks for urban traffic monitoring: Applications and architectures," in Proc. 4th Int. Conf. Ambient Syst., Netw., Technol., Jun. 2013, pp. 617–626.

[2] C.-L. Chen, C. W. Hsu, and C.-M. Wu, "A DSRC-based collision warning and autonomous system for inter-vehicle communication," in Proc. Cross Strait Quad-Regional Radio Sci. Wireless Technol. Conf., Jul. 2011, pp. 816–821.

[3] M. Fanaei, A. Tahmasbi-Sarvestani, Y. P. Fallah, G. Bansal, M. C. Valenti, and J. B. Kenney, "Adaptive content control for communication amongst cooperative automated vehicles," in Proc. IEEE 6th Int. Symp. Wireless Veh. Commun., Sep. 2014, pp. 1–7.

[4] N. Alam, A. Kealy, and A. G. Dempster, "An INS-aided tight integration approach for relative positioning enhancement in VANETs," IEEE Trans. Intell. Transp. Syst., vol. 14, no. 4,pp. 1992–1996, Dec. 2013.

[5] L. Tu and C.-M. Huang, "Forwards: A map-free intersection collisionwarning system for all road patterns," IEEE Trans. Veh. Technol., vol. 59, no. 7, pp. 3233–3248, Sep. 2010.

[6] S. Al-Sultan, A. H. Al-Bayatti, and H. Zedan, "Context-aware driverbehavior detection system in intelligent transportation systems," IEEETrans. Veh. Technol., vol. 62, no. 9, pp. 4264–4275, Nov. 2013.

[7] R. Uzcategui and G. Acosta-Marum, "Wave: A tutorial," IEEE Commun. Mag., vol. 47, no. 5, pp. 126–133, May 2009.

[8] Draft Amendment to Standard for Information Technology— Telecommunications and Information Exchange Between Systems— Local and Metropolitan Area Networks—Specific Requirements— Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications—Amendment 7: Wireless Access in VehicularEnvironment, IEEE Standard P802.11p/D3.0, 2007.

[9] Trial-Use Standard for Wireless Access in Vehicular Environments (WAVE)—Resource Manager, IEEE Standard P1609.1, 2006.

[10] Trial-Use Standard for Wireless Access in Vehicular Environments(WAVE)—Security Services for Applications and Management Messages, IEEE Standard P1609.2, 2006.