International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169
Volume: 4 Issue: 4 238 - 243

Low Power FinFET based SRAM Cell Design

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***Abstract*—**With the incessant developments occurring in VLSI circuits and systems arena and power dissipation becoming a major design constraint, the power component can be considerably reduced through efficient designing of the SRAM memory elements. Nowadays, multi-gate devices such as the FinFETs play a prominent role in reducing the power dissipation that what was found realizable by the conventional CMOS devices. Additionally, the FinFETs are found to be capable of overcoming some of the major drawbacks of the conventional CMOS devices, namely, the leakage current, the sub-threshold leakage, parasitic capacitance etc. This paper uses 32nm FinFET devices for the implementation of the 6T, 7T SRAM cell architectures and the resultant power is calculated for the read and write operations, to study the comparative benefits of the use of FinFETs in the memory cells than that of the CMOS counterpart circuits. Industry standard Cadence EDA tools have been employed for the simulations. The layout designs of 6T and 7T SRAM cells have been carried out using 180nm CMOS technology library for post layout simulations.

Keywords*—*FinFET; CMOS; 6T SRAM cell; 7T SRAM cell;

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I. INTRODUCTION

Memory array plays a vital role in the digital circuits, such as the system on chips (SoCs), microprocessors and microcontrollers, and the memory consumes a major chip area. Further, these arrays contribute to a large amount of power dissipation. Increased transistor leakage for the lower technology nodes has become an important challenge in sizing the SRAM cell. Several literature cater to various new architectures for the SRAM cell with the focus on reduction on the number of devices in the cell, reduced leakage power and good noise margin characteristics [1]. Moreover by comparing different SRAM cell structures such as the 4T, 5T, 6T, 7T, 8T and 9T, it has been proved that the 7T structures incurs improved write time margin, as well as the read static noise margin (SNM) without any considerable increase in chip area[1]. In this paper, the design of memory cells using FinFET devices have been carried out for comparison of their performance against the CMOS counterpart. The SRAM cells are compared using 6T and 7T SRAM structures and the results are analyzed. The FinFET has been chosen due to its advantageous structural characteristics. The FinFETs are made up of very thin and undoped body, which helps in suppressing major leakage paths, and hence in reducing the SCEs(Short Channel Effects) associated with the short channel devices. Because of the lightly doped body, the threshold voltage variation is eliminated due to its random fluctuation of dopants. The FinFET structure also provides enhanced carrier transport, thus resulting in higher current. Due to these characteristics, the power consumption in SRAM cell can be drastically reduced[2].

This paper is arranged as follows. Section II presents the FinFET device and its performance benefits. Operation of the 6T and the 7T CMOS based SRAM cells are described in section III. Section IV presents the FinFET based SRAM cell operation. The read and write simulations of the SRAM cells in Cadence environment are presented in Section V. Section VI analyses the results and the comparative performance analysis and observations. Section VII concludes the paper.

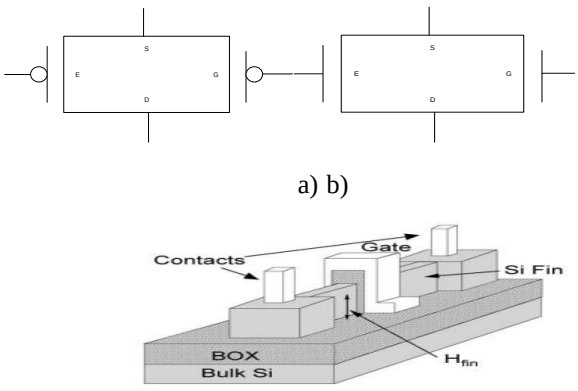
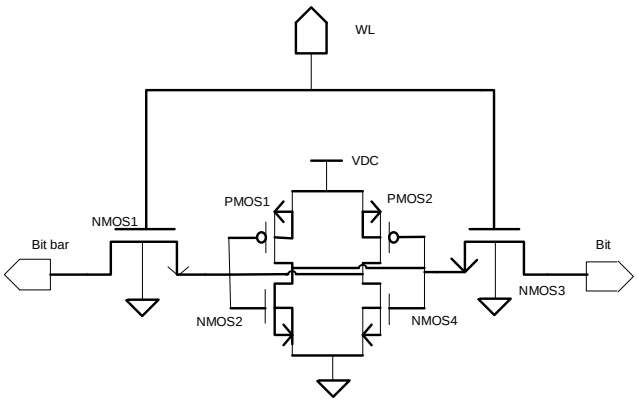


Figure 1: a) PFinFET Symbol b) NFinFET Symbol c) FinFET Structure.

II. FINFET DEVICES

CMOS devices incur high leakage current, high sub-threshold leakage and are composed of parasitic capacitances. These can be overcome by the FinFETs. As shown in Figure 1, the conducting channel of FinFET is wrapped by a thin silicon fin, which is the distinguishing feature when compared with other FETs. The effective channel length of the FET is proportional to the fin thickness. This fin wrap curtails the leakage by improving the effective electrical control over the channel. Furthermore, the FinFET provides better control over the short channel effects than the CMOS device. This reduced leakage current yields reduced power consumption in the circuits employing FinFETs. Hence, FinFET proves itself as a low power robust device and can prove to be an effective alternative for the CMOS transistor which is bulkier[3].

The FinFETs are used in different configurations normally. The 'Double Gate'(DG) configuration,is the one in which both the gates are shorted to realize switching of the FinFET, while these two gates remain isolated in the 'Back Gate'(BG) mode [4].



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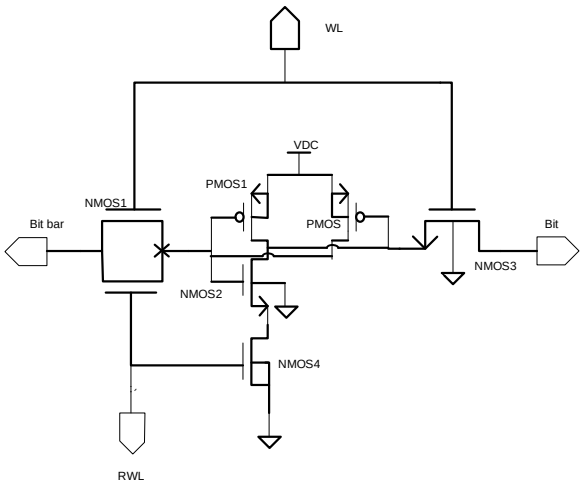

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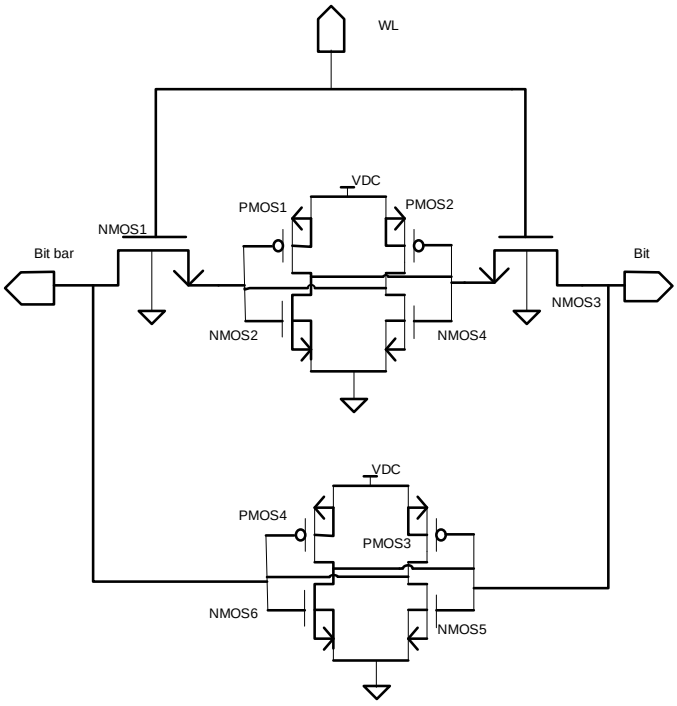

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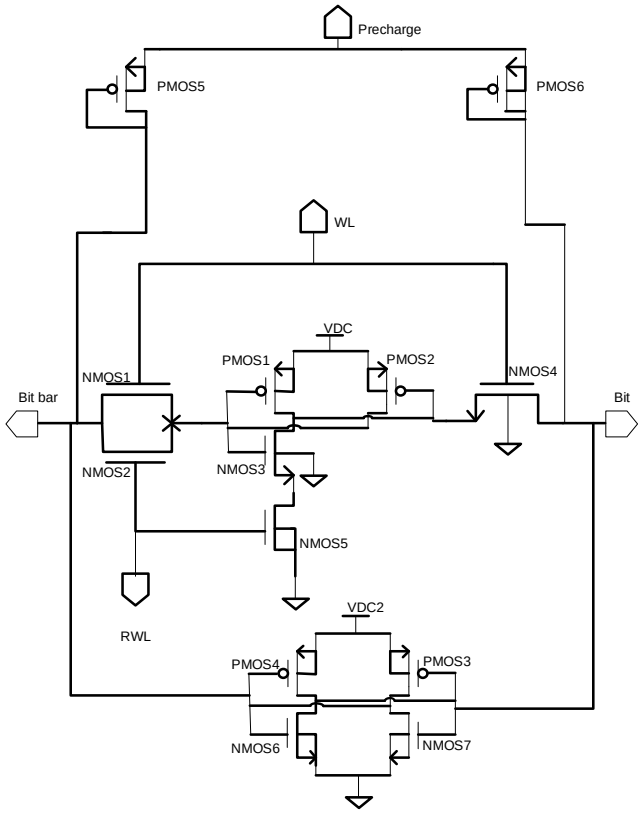

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Figure 2. CMOS SRAM Cellsa) 6T SRAM cell, b) 7T SRAM cell, c) 6T SRAM cell with cross-coupled invertors d)7T SRAM cell with cross-coupled invertors.

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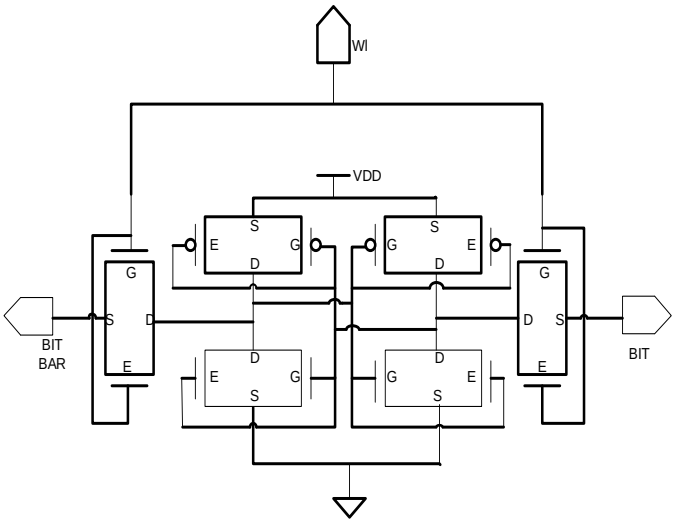
III. CMOS SRAM CELLS

Figure 2 shows the 6T and 7T structures of the CMOS based SRAM cells. The small rise in *Word-line* enables the NMOS pass transistors on the both sides and passes the *bit*-line and *bit bar* line data into the latch. The latch is formed by two cross-coupled invertors. When the word line is kept at logic zero, it disconnects the latch from the bit and bit bar line. And, the data remains latched inside the SRAM cell. The invertors help in reinforcing the status of the output data, and it will be so as long as the memory cells are provided with the supply. For reading the data from the SRAM with low power and good speed performance, the pre-recharging done on the bit and bit bar lines is an important step. During pre-charging, same voltage, viz. $V_{dd}/2$ is maintained for both the bit line and bit bar line, where $V_{dd}$is the power supply voltage. During the pre-charging process ,the SRAM latch remains separated from the pass transistors. And when the pre-charging is completed, and when the data read operation takes place, the small difference between the voltage values between the bit line and bit bar line is sensed and amplified by enabling the sense amplifier.

In this paper, the use of two different sense amplifiers, namely, the current sense amplifier and the voltage sense amplifier are presented. However, the current sense amplifier is found to be more preferable than the voltage sense amplifier because of its improved performance[4].

The 7T SRAM cell structure comprises of individual read line and write line as shown in Figure 1.The 7T structure has improved performance in terms of write time and margin, read SNM compared to the other existing SRAM cell structures[1].Furthermore, the 7T cell provides improved performance without any considerable increase in the chip area. As shown in Figure 1, the active word line enables the NMOS1 and NMOS4 transistors, which passes the bit line and bit bar line data in to the memory cell. Unlike the 6T SRAM cell, in 7T structure only three transistors are used in the latch. During the read operation, the high read line along with the sense amplifier provides a discharging path to ground through the device NMOS5. This discharge causes a voltage difference between the bit line and the bit bar line which is sensed and amplified by the sense amplifier and the memory cell is read with more precision.



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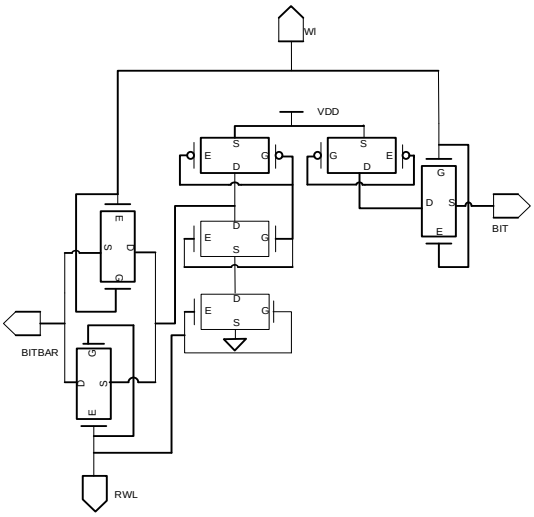

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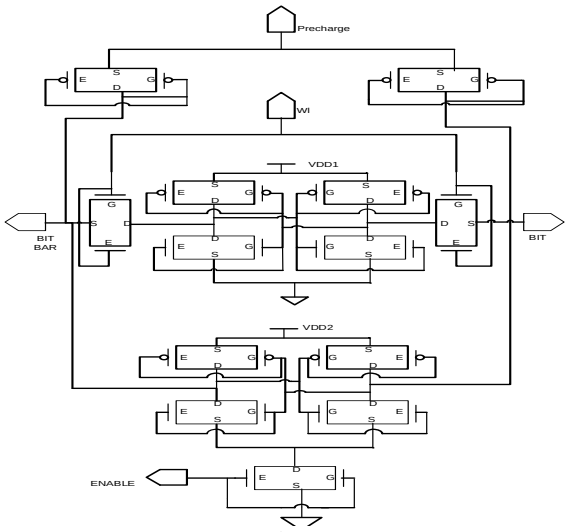

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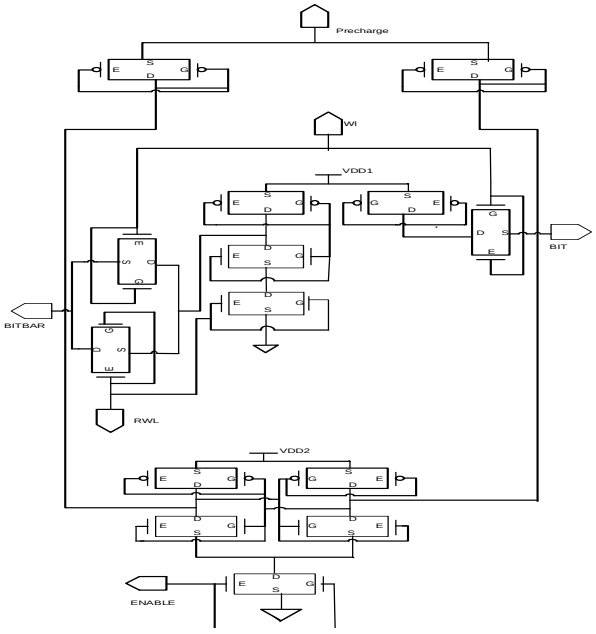

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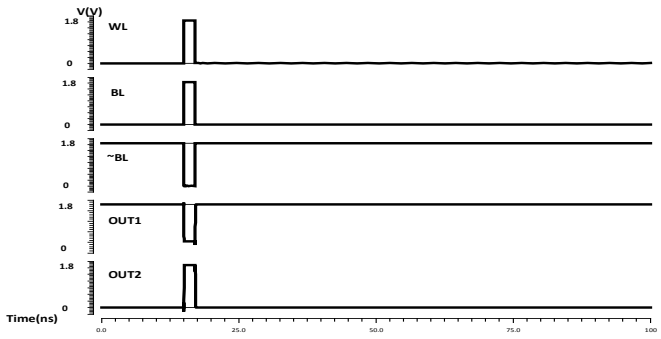
Figure 3. FinFET SRAM Cells a) 6T SRAM cell, b) 7T SRAM cell, c) 6T SRAM cell with cross-coupled invertors d)7T SRAM cell with cross-coupled invertors.

IV. FinFET SRAM Cells

The structure and operation of the CMOS SRAM cell have been described earlier. The use of the CMOS devices in the SRAM structure makes it vulnerable for more leakage current and the short channels effects. Figure 2 presents the structure of 6T and 7T based SRAM cells using double gate configuration FinFET. To get a perfect read and write values, transistor sizing has been done. Generally, high threshold voltage is maintained for the PMOS devices, and for NMOS devices comparatively lower threshold value is maintained. The Write and Read operations are carried out in the similar manner as described in previous section. The structure for the FinFET based 6T and 7T SRAM cells and read circuits with FinFET current sense amplifier are shown in Figure 3.



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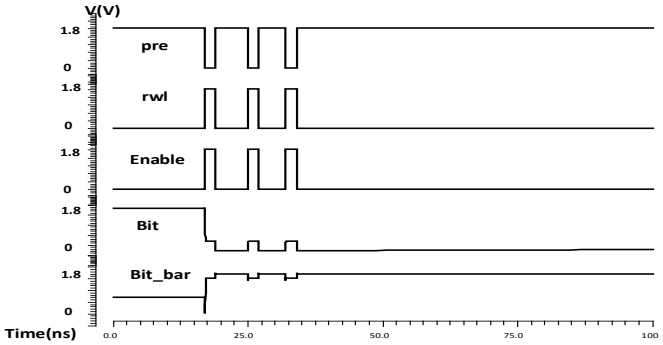

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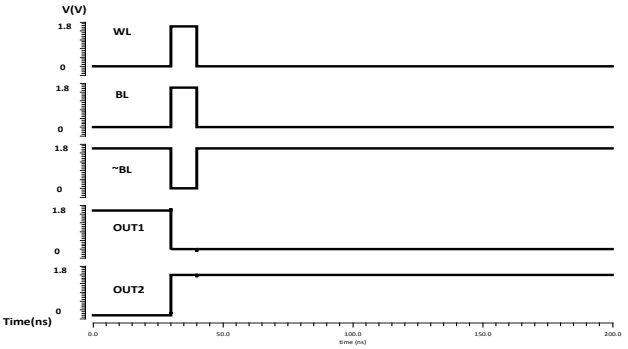

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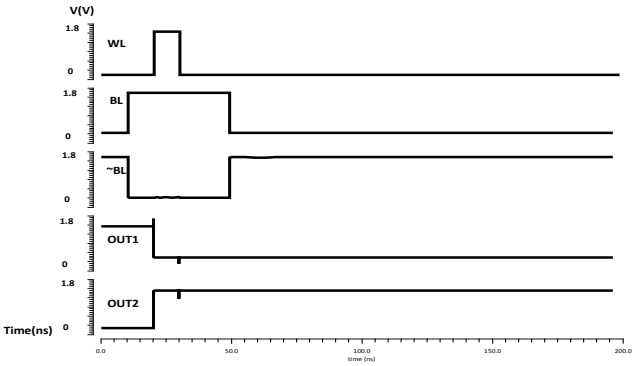

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Figure 4. Simulation results for 7T SRAM cell.

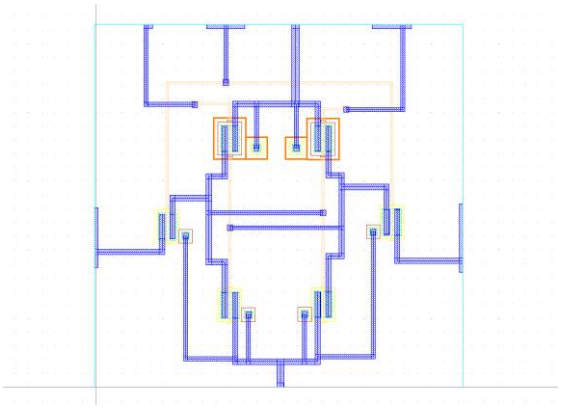
a) Write operation (CMOS 180nm) b) Read operation(CMOS 180nm)c) Write operation (CMOS 32nm) d) Write operation (FinFET 32nm)

V. Simulation Results

Figure 4 shows the simulation results obtained by write and read operation of 7T SRAM cell in Cadence Virtuoso tool. The 7T structure provides better write margins compared to the other SRAM cells [1]. The FinFET based SRAM cell yields more efficient write operation as compared to other CMOS SRAMs. Because FinFET causes less leakage current which switch the device faster [2]. By providing a short word line pulse, data in bit line and bit bar line can be written in to the latch. Short word line pulse prevents killing of the bit. Once data is written in the SRAM cell, it retains the data as

long as the power supply is provided to the cell. This is shown in Figure 3(d), with the process of reading the data consequently 3 times by enabling the sense amplifier. Before reading the data pre-recharging pulse should be provided to create voltage difference between bit line and bit bar line.

The simulations for the write and read operations have been carried out using the extracted netlist. Table 1 summarizes the results. Supply voltage of 1.8 volts, 0.9 volts has been used for 180nm and 32nm technology node respectively.



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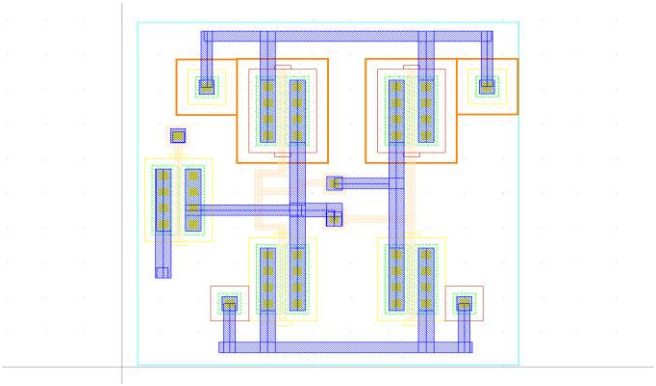

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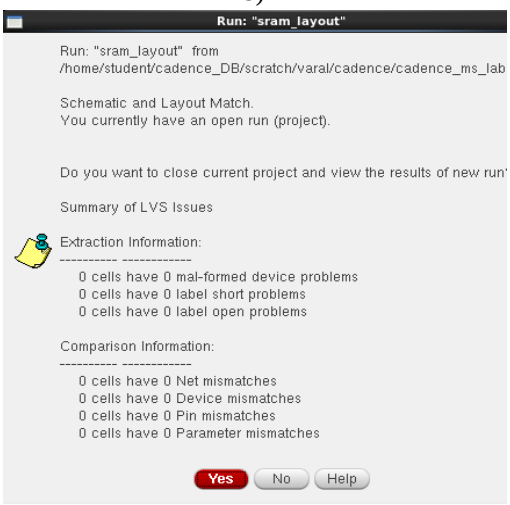

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Figure 5. Layouts of SRAM Cells (CMOS 180nm) a) 6T SRAM cellb) 7T SRAM cell. c) LVS Report

Figure 5 shows the layout designs of the 6T and 7T CMOS SRAM structures using 180nm technology node. Standard design rules for 180nm technology are followed for drawing the layout of structures. The DRC (Design Rule Check) and the LVS (Layout Verses Schematic) checks of these layouts are carried out and verified using Assura tool from Cadence platform. In figure 5(c), snapshot of LVS report given by Assura tool. In LVS check, layout connections, nets, cells, devices are matched with the schematic of the circuit.

VI. Observation and Comparison

Table 1: Power Comparison

SRAM Cell	Power Comparisons		
	CMOS(180nm)	***CMOS(32nm)***	***FinFET(32nm)***
6T	37.9mWatts	1.27uWatts	0.344uWatts
7T	0.144mWatts	0.91uWatts	0.549nWatts

Table 1 shows the power dissipation of 6T and 7T structures of SRAM cells using CMOS technology (180nm and 32nm) and FinFET technology (32nm). The inferences from the results depict the fact that the power dissipation reduces as devices of lower technology nodes are employed. And, for the 32nm technology models, power dissipated in SRAM cell with the FinFET is much less as compared to CMOS SRAM cell of the same technology node.

VII. Conclusion

From the simulation results obtained from Cadence EDA tool, the power dissipation is calculated for the SRAM cells and it is also observed that the use of FinFET reduces the power dissipation in addition to the additional advantages. This shows that use of multi-gate FinFET devices over conventional CMOS devices helps the designers in realizing reduction in power dissipation of the IC chips.The32 nm FinFET 7T SRAM cell incurs 0.549nW of power dissipation which is much less than 0.91uW of CMOS SRAM of same technology node. Further, it is observed that the write time for the 7T SRAM structure is enhanced and it is less than that of the 6T SRAM structure. Power dissipation is also reduced by using 7T structure SRAM cell in place of 6T SRAM cell. Hence, it can be concluded that the FinFET proves better in terms of low power operating and robust SRAM cell designs. Further, new SRAM cell architecture with FinFET can be designed, which will be the future work of the team to provide more power reduction than the existing SRAM cells and enhanced memory read and write characteristics.

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