

# Design of Power Efficient and High Slew Rate Class AB OPAMP

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**Abstract-**The paper deals with aim to design an OPAMP of Class AB to achieve high power efficiency and slew rate. To have high slew rate the focus of the proposed work as high slew rate contributes to the fast and dynamic output response. Power efficiency is driving factor from MOORE'S law. A Push pull OPAMP with current replicating branch is used to achieve symmetrical wave with high slew rate. Adaptive biasing is another technique employed to increase the slew rate. According to the Moore's law, increase in power takes place in adaptive biasing due to increase in transistors, but the proposed circuit is best tradeoff between slew rate and power efficient factors. The existing work could only increase the slew rate by 4 to 5 times, but our proposed work increases it even further compared to the existing work, at the same time it results in decrease of power. In this work we are combining two techniques, namely adaptive biasing and current replicating branch which combine to result in better slew rate without increase in power. The proposed work is implemented with Cadence Virtuoso tool.

**Keywords:** Adaptive Biasing, Class AB OPAMP, Current Replicating branch, Slew Rate.

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## I. INTRODUCTION

In conventional two stage OPAMP as shown in Fig.1, slew rate increases with moderate increase in power dissipation. Its last stage is push-pull configuration to achieve high voltage swing. Its disadvantage is one of the OPAMP transistor present below input stage acts as current sink due to this, there is no current path to output during negative cycle. Hence, current is unevenly distributed in positive and negative cycles. The applied input voltages are 1.8 V to non inverting and -0.625 V to the inverting input as shown in Fig.2. The Operating frequency of both the inputs is 100K Hz. The average power consumption is 17.34  $\mu$ W and slew rate is about 149 V/s. The circuit is implemented in 180nm Technology node.

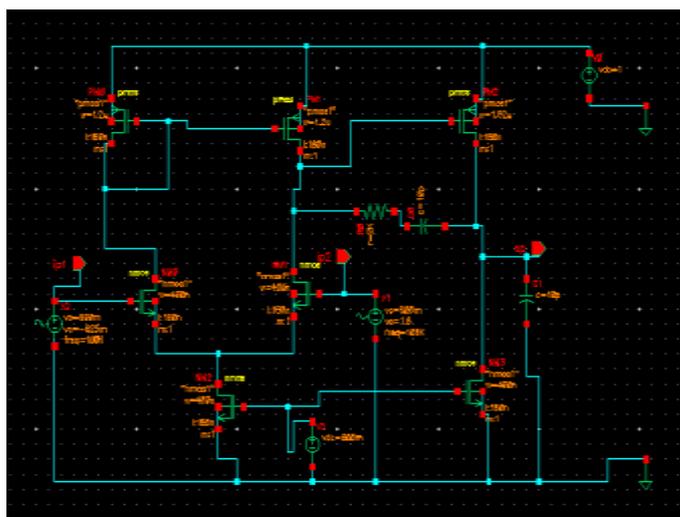


Fig 1 Class AB OPAMP.

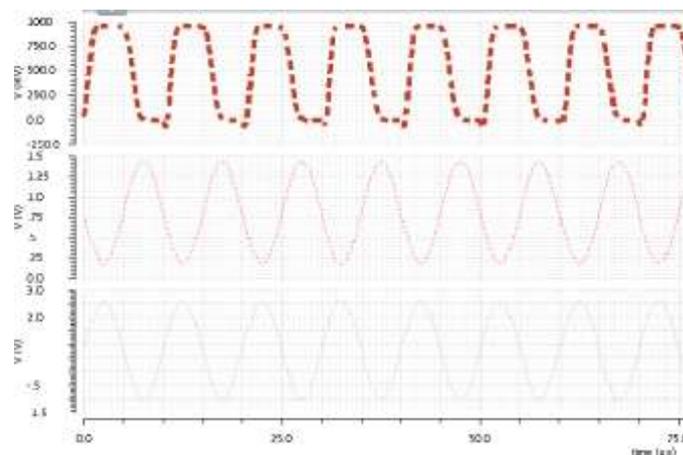


Fig 2 Output of Class AB OPAMP.

## Conventional OPAMP with R-C branch

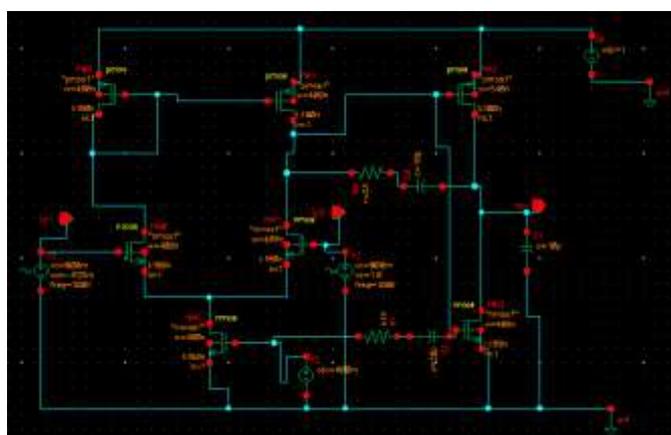


Fig3. OPAMP with R-C branch

Conventional OPAMP with R-C branch technique overcomes the drawback of previous circuit in which the output response is uneven during positive and negative cycles. This technique helps in

improving the symmetry of output response. The slew rate and power dissipation of this circuit has better values compared to earlier circuit. But this arrangement comes with a drawback of miller effect as the frequency increases, its operation becomes ineffective. The average power consumed is  $12.07 \mu\text{W}$ , where as the slew rate is about  $13.96 \text{ KV/s}$ . Power consumption and slew rate of the circuit shows big improvement over the conventional OPAMP circuit. The response shown in Fig.4, shows the output wave having symmetric positive and negative cycle. This output when compared to the output of earlier circuit has better symmetric positive and negative cycles. The applied input to inverting and non-inverting inputs are  $-0.625 \text{ V}$  and  $1.8 \text{ V}$  respectively. The operating frequency of the both inputs is  $100 \text{ KHz}$ .

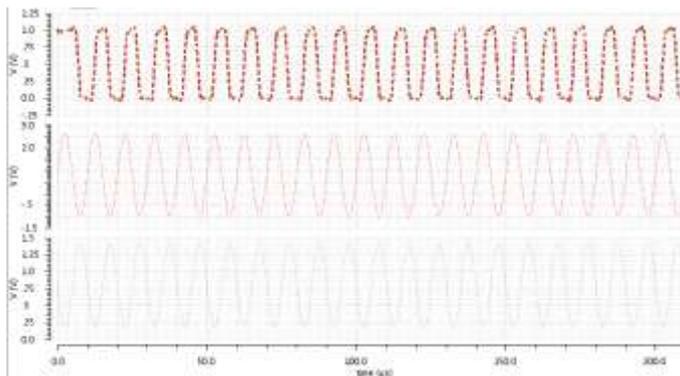


Fig.4 OPAMP with R-C branch.

#### Pushpull OPAMP with Current Replicating branch:

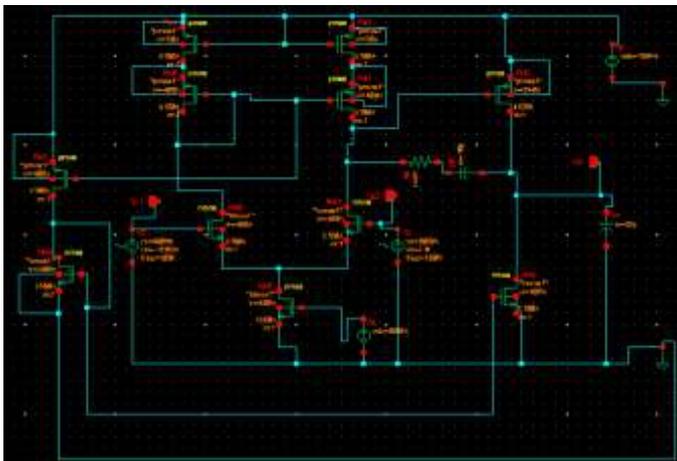


Fig5. OPAMP with Current Replicating branch and Adaptive biasing.

The conventional opamp with r-c branch circuit has draw back of miller effect in order to reduce it we are using push pull OPAMP with current replicating branch. By using Current replicating branches we can generate required bias voltage at the gate of output transistor, other advantage is increase in slew rate. But disadvantage of this technique is increase in power consumption as shown in Fig 5. Number of transistors have increased due to which power consumption too increases in accordance with Moore's law.

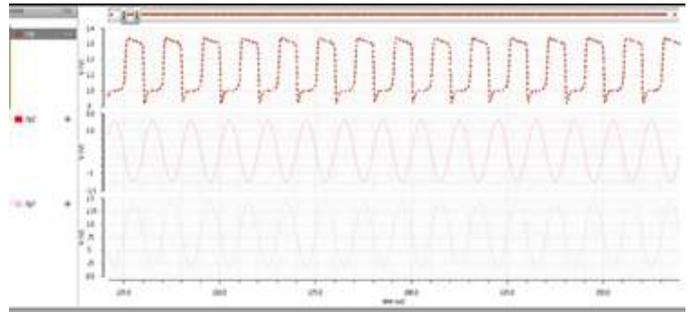


Fig6. Output of OPAMP with Current Replicating branch and Adaptive biasing.

The slew rate of OPAMP with Current Replicating branch and Adaptive biasing is  $24.31 \text{ kV/s}$  which is more  $74.14\%$  compared to conventional OPAMP with r-c branch technique. The average power is around  $16.22 \mu\text{W}$  which is highest among all the circuits presented in the paper.

#### Proposed Paper

By using current replicating branch we have eliminated the miller effect and by using adaptive biasing we have increased the slew rate. But due to adaptive biasing power consumption has increased. Hence in order to reduce number of transistors the proposed circuit is designed in such a manner that the number of transistors are reduced.

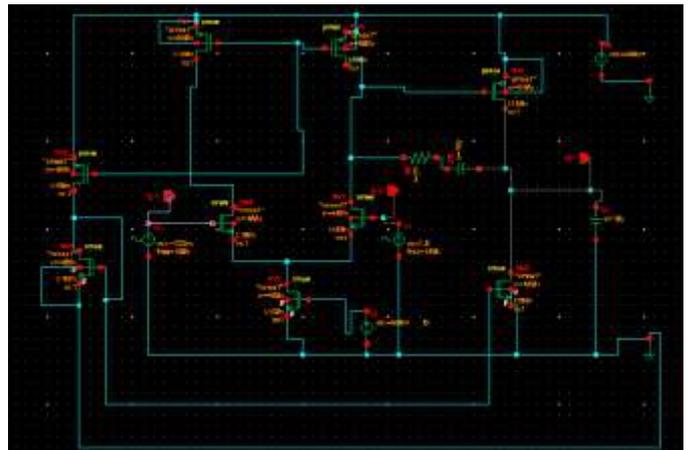


Fig 7. Proposed Circuit

The transistors in Adaptive biasing are operated in triode region due to which it provides high resistance region which results in large current due to high voltage swing. In the absence of current replicating branch the output in positive cycle was mainly contributed by PMOS, but in the proposed circuit the current replicating branch provides current path to output in negative cycle. Hence a symmetric wave is obtained in both positive and negative cycles. The biasing voltage is taken from current replicating branch which results in increased slew rate, with little increase in power. The slew rate is  $110 \text{ kV/S}$  and power consumed is  $12.4 \mu\text{W}$ . The powerful combination of Current replicating branch and adaptive biasing results in high slew rate as evident in Fig 8. Where Output of Proposed circuit, has sharp rising and falling edges.

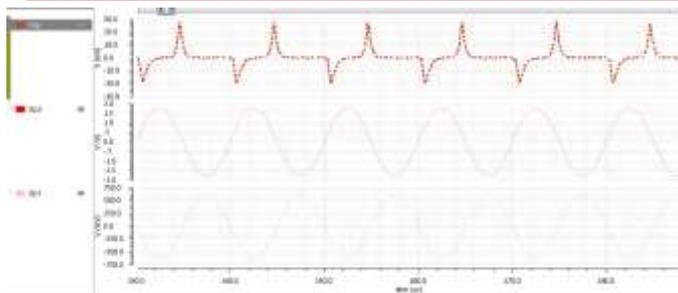


Fig 8. Ouput of Proposed Circuit.

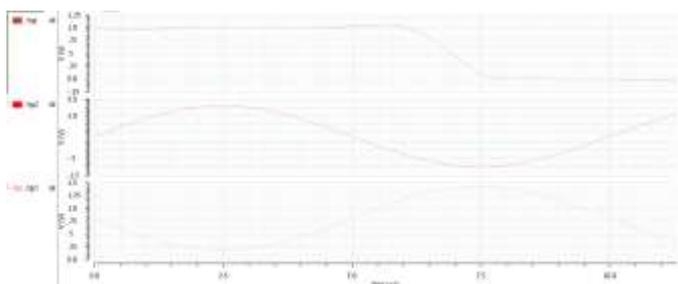


Fig 9. Part of output illustrating the OPAMP behavior of the circuit.

As shown in Fig 9. Part of Output shows three waveforms in which the lower two waves are inputs and uppermost wave is the output, The Differential OPAMP amplifies the difference between the inputs, as shown in the above Fig 9. When inputs are moving away from each other the output increases and output decreases as the inputs move closer towards each other, this illustrates that the proposed circuit works as Differential OPAMP.

**Results and Discussion.**

In Conventional OPAMP slew rate is least and power consumption is highest among Conventional RC branch, Push pull with current replicating branch and proposed circuit. Conventional RC branch has second best power consumption value after proposed circuit and its slew rate is less than both circuits, Push pull with current replicating branch and Proposed circuit. Push pull with current replicating branch circuit has higher power consumption compared to Conventional RC branch and Conventional RC branch its Slew rate is lower than then proposed circuit and higher than Conventional OPAMP and Conventional RC branch. The proposed circuit slew rate is 110.7k V/S which is very high compared to all the circuits and power consumption is second best value after conventional RC branch circuit hence proposed work has optimum combination of both power and slew rate, which is best compared to other circuits.

Table 1. Comparision of various Class AB OPAMP techniques.

Type of circuit	Conventional OPAMP	Conventional RC branch	Push pull with current replicating branch	Conventional RC branch
Slew rate (K V /S)	.149	13.96	24.31	110
Power consumed( $\mu$ W)	17.34	12.07	16.22	12.40

**CONCLUSION**

The adaptive biasing and current replicating branch in Proposed work shows optimum values of Slew rate and power consumption, as shown in comparison Table 1. Hence it is the best circuit.

**FUTURE SCOPE**

To obtain better values of slew rate and Power consumption by implementing circuit in 90nm, 45nm technology node and decrease the power consumption to least possible extent.

**REFERENCES**

- [1] Xiao Zhao, Huajun Fang and Jun Xu "A New low power symmetric folded cascode Amplifier by Recycling Current in 65nm CMOS Technology" IEEE, Sept, 2011.
- [2] Sushmita Baswa, Jaime Ramirez-Angulo, Antonio J Lopez-Martin and Ramaon G.Carvajal "A novel Family of Low Voltage Very Low Power Super Class AB OTAs with Significant Enhanced Slew rate and Bandwidth", IEEE 2004.
- [3] Mehdi Noormohammadi, Vahid Khojasteh Lazarjan, Khosrow HajSadeghi "New Operational Transconductance Ampilifer Using Current", IEEE Jan, 2012.
- [4] Antonio J Lopez-Martin, Sushmita Baswa, Jaime Ramirez-Angulo, and Ramaon G.Carvajal "Low-Voltage Super Class AB CMOS OTA Cells With Very high Slew Rate and Power Efficiency" IEEE Journal Of Solid State Circuits Vol 40, NO 5, May. 2005.
- [5] APisak Worapishet, John B. Huges and Chris Toumazou, Low Power High Frequency Class AB Two-Step Sampling Switched-Current], IEEE Transactions on Circuits and Sytems-II, Vol 50, No 9, Sept 2003.
- [6] Jaime Ramirez-Angulo, Antonio J Lopez-Martin and Ramaon G.Carvajal, Juan A Galan "A Free but Efficient Class AB Two stage operational Amplifier" IEEE, Feb, 2006.
- [7] Jaime Ramirez-Angulo, Antonio J Lopez-Martin and Ramaon G.Carvajal, Carlos Rubia-Marcos "Super Class AB OTAs with Adaptive Biasing and Dynamic output Current Scaling", IEEE Trnsactions on Circuits and Sytems-I, Vol 54, No 3, March 2007.
- [8] Chih-Wen Lu, Kuo-Jen Hsu" A Large -Swing High Driving Low-Power Class AB Buffer amplifier employing Adaptive Gain Error Amplifiers" International Carribbean Conference on Devices, Circuits and Systems, Apr 2006.
- [9] H. Daoud , S bennour, S.BenSalem, M.Loulou "Low Power SC CMFB folded cascode OTA OPTIMAZATION, IEEE, Apr, 2008.
- [10] Atefeh Salimi, Rasoul Dehghani, Abdolreza Nabavi "Design of a Rail-Rail, Low Output Impedance Class AB Power Amplifier for Envelope Tracking of Polar Modulators" International Conference on Advanced in Computational Tools for Engineering Applications(ACTEA), IEEE, Feb 2012.
- [11] Gaetano Palumbo and Salvatore Pennisi "Design Methodology and Advances in Nested-Miller Compensation"IEEE Transcations on Circuits and Sytems-1 Vol. 49, NO.7, July 2002
- [12] M.R.Valero, S.Celma, N.Medrano, B.Calvo, C.Azeona "An Ultra Low-Power Low-Voltage Class AB CMOS Fully Differential OpAmp"IEEE , July 2012.
- [13] Micheal Figueiredo, Rui Santos-Travares, Ediei Santin, Joao Ferreira, Guiomar Evans and Joao Goes "Two-Stage Fully Differential Inverter based Self-Biased CMOS Amplifier with high efficiency" IEEE Transcations on Circuits and Sytems-1 Vol. 58, NO.7, July 2011.
- [14] Fan You, S.H.K. Embabi and Edgar Sanchez-Sinencio"A1.5V Class AB output Buffer" IEEE Transcations on Circuits and System , 1996.
- [15] Chih-WenLU and Yen-Chung Huang "1.5V Large-Driving Class AB BUFFER Amplifier with quiescent current control" Electronics Letters, Vol.40, NO.1, Jan 2004.

- [16] Zushu Yan, Pui-in Mak, and Rui P. Martins “TWO-Stage Operational Amplifier”IEEE Circuits and Systems Magazine First quarter , 2011.
- [17] S BenSalem, M.Loulou, H. Daoud “Low Power SC CMFB folded cascode OTA OPTIMAZATION,IEEE, Apr, 2008.
- [18] Chi-Hung Lin and Mohammed Ismail “A Low –Voltage CMOS Rail-to-Rail Class- AB Input/Output Opamp with Slew arte and Settling Enhancement.” In Proc. IEEE Int. Symp. Circuits and Systems. Vol 1 , Jun 1998.

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