International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169
Volume: 2 Issue: 1 101 – 104

Testing of Analog and RF Circuits using Embedded Sensors

Shrikant Bhoyar,
Lecturer, RGCER, Nagpur
shrikantbhoyar08@gmail.com

Nilesh Chide,
Lecturer, RGCER,
Nagpur
chidenilesh@gmail.com

Ashwini Shende,
Lecturer, RGCER,
Nagpur
ashu.shende09@gmail.com

Avinash Mahule,
Lecturer, DBACER,
Nagpur
avinash.mahule11@yahoo.in

***Abstract*—** Testing of on-chip RF and microwave circuits has always been a challenge to the test engineers. Since the emergence of System-on-a-Chip (SoC), characterization and test development is time-consuming, they contribute to a significant part of the manufacturing cost. Moreover, test development of RF and microwave circuits requires years of experience and expertise. In this paper, we propose to use built-in-test in the form of specific sensors. Instead of testing the devices specifically for certain performance metrics, the output values of the sensors, which are usually DC or a very low frequency signal, can be used to get a quick and accurate estimate of the behavior of the device under test (DUT). For a relatively low-yielding process, which is usually the case for RF and microwave circuits, significant number of faulty devices can be identified without even performing the standard manufacturing test on the devices. Moreover, these sensors can also be used for on-line test. In this paper, we also propose an algorithm to optimally place the sensors at the output of a system-under-test and use the sensor output to get an estimate of the specifications of the system-under-test. Using this method, specifications can be estimated within an accuracy of ±3% of its actual value

***Index Terms*—** *Built-in-self test, Device under test*

*****

1. INTRODUCTION

In any semiconductor manufacturing process, test is an inseparable, probably one of the most essential parts of the whole procedure. Any semiconductor device that is produced is characterized and tested thoroughly for its performance metrics. Usually, a set of tests are sequentially performed on the device under test (DUT) and from the responses put out by the DUT, the device performance metrics, i.e. the specifications of interest are measured using a set of test programs. The device is classified as good, bad or marginal according to the obtained specification values. Finally, the good devices are separated out and sent to the market.

In the above described test procedure, the whole manufacturing process is sequential, where the design is first made, followed by the production of ICs and finally the performing tests. As is evident, any errors or omissions in the design or the fabrication process are detected after the test is completed. In case of complex designs viz. SoCs or SoPs, considerable revenue is lost in this procedure. Usually many ICs are also combined to construct a complete system. In such cases, it is a difficult task to identify the faulty IC(s). Moreover, test access is usually very limited for any individual IC. Therefore, to overcome this test problem, different methods are considered for test access.

In this paper, a novel method is proposed to address the above-mentioned problem using embedded sensors for test. It has been visualized as a built-in-test solution, where the sensors outputs will give the test engineer insight about the DUT performance. For a completely integrated system, this way will quickly diagnose the potential faults present in any specific IC. It has been shown that the specifications of the DUT can be predicted very accurately using these sensor outputs directly.

2. MOTIVATION

From the early days of semiconductor manufacturing, people have been trying to reduce the overall manufacturing cost. For this purpose, design engineers concentrated on accurate simulations, corner analyses and relaxing the guard bands to increase yield. In addition, considerable improvements have occurred in fabrication procedure, viz. better device characterization and modelling, using different substrates for higher speed, larger wafers for greater yield. In comparison, test procedures have remained at the same level as it was many years back. As a result, test engineers are challenged to test increasingly complicated parts. In some cases, it also becomes difficult to afford a better tester and thus, engineers resolve to use low-end testers. Due to the limited capabilities of the low-cost testers, pressure is laid on the test engineers to achieve accurate measurements using low-cost testers.

2.1 Why use sensors?

Until recently, test procedure was mostly based on applying a test waveform, capturing the response of the DUT accurately and finally analyzing the captured waveform to

obtain the specifications of the device. With increasing device speed and shrinkage in device dimensions, the speed of operation of silicon and other associated semiconductor devices has increased manifold during the last decade. At such speeds, sampling the response of the DUT to capture its output is near to impossible. As an example, an LNA operating for GSM systems, the nominal output signal level is at –30dBm at 1.8GHz. To sample the output at nyquist rate, an A/D converter operating at a minimum of 3.6 GHz is desired with a dynamic range of 60dB. This requires a resolution of at least 3.9nV for 8-bit output and 0.97nV for a 10-bit output, which are close to the noise floor. The design for such an ADC is a challenge by itself. Moreover, test access is very difficult for RF devices, as impedance matching for maximum power transfer is an important criterion for maintaining signal integrity at RF frequencies. Although various BIST schemes have been proposed in the past, both for analog as well as digital circuits, until now, there is no concrete way to test RF devices. To overcome these hindrances, we propose a new test methodology for RF and microwave circuits.

2.2 Proposed test method

In the method described in this paper, these problems are eliminated by putting the test on-chip. The tests are put in the form of sensors in the critical signal paths that need to be observed to determine the DUT performance. The output of the sensors is usually a DC or a very low frequency signal. This is a means to bring the expertise of designers and test engineers together and developing the test-plan at an early phase of production, i.e. design. This scheme has many advantages compared to the standard test approach:

1. As the tests are put on-chip, the signal is captured by the circuits on-chip and hence the problems related to matching the RF or microwave signal paths outside the IC are not present any more.
2. There is no need to sample the waveform to capture it; rather the signal characteristics can be directly extracted on-chip and output by the sensors. This need not be a very high speed output as in most cases, the output signal expected is periodic.
3. The sensor outputs can also be used for on-line test of the device. In cases where many devices are present with very limited test access, the outputs of the sensors can provide a quick estimate of the performance of any specific IC. This can be further extended as a built-in-test solution for larger systems, viz. SoCs and SoPs.
4. Finally, this method can be combined with alternate test approach to predict the specifications of interest without even performing specification tests. As the sensors, which are also on-chip, experience the process perturbations in the same way as the CUT, there is no need to perform calibration.
5.

3. TEST METHODOLOGY

In this work, the objective is to predict the specifications or the performance metrics of the DUT by observing the sensor outputs. Instead of performing the standard tests on the DUT, the sensor outputs are captured and used to predict the specifications of the DUT. This is not a test generation problem, rather a study to determine the feasibility of the proposed method. We assume that the test is already known in this case. In the proposed test methodology, the focus is on using sensors effectively for a fixed test stimulus applied to the DUT. The test framework uses the available measurements to determine where to place which sensor to get the best estimate of the performance metrics of the DUT.

3.1 Alternate test framework

In the alternate testing approach, the test specifications of the system-under-test are not measured directly using conventional methods. A different stimulus is used for test purposes. Using a training data set of specifications and the measurements, a nonlinear model is constructed. In essence, all the test specifications can be computed from the output measurements to a single applied test stimulus instead of having a different test setup for each specification measurement.

3.2 Test architecture

The sensors are used within the DUT, in the critical signal paths. The sensors tap onto the signal path and provide separate outputs, as shown in Figure 1.

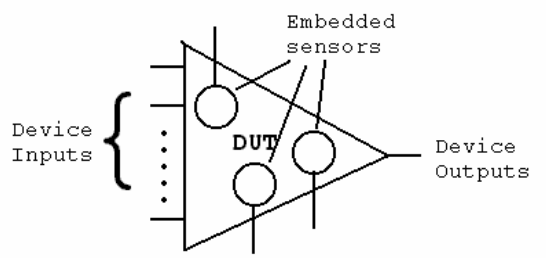

Figure 1 Sensors embedded in the DUT

In case of a typical RF receiver, the front-end usually consists of a LNA followed by a Mixer/Local Oscillator and finally a VGA, before the signal is fed to the baseband DSP processor. In most cases, viz. cellular telephone systems, the different parts of the circuit are on a single chip, except for the bulky passive components and filters (mostly SAW filters), which are put off-chip (Figure 2). Therefore, for such systems, there are only a few access points available, as indicated in Figure 2. In this paper, we have limited our observation to such access points only.

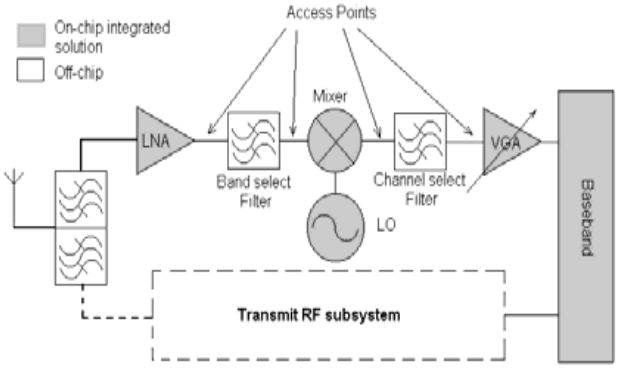

Figure 2 System test overview

As shown above, so far our scope is limited to placing the sensors at the available access points only. While more than one sensor can be put at any one of these access points, the issue of signal integrity and purity in terms of matching has to be kept in mind. As shown in Figure 3, the sensors are placed at these points and the sensor outputs are captured to predict the specifications of the individual blocks and the system as well. Moreover, as system integration gets more mature, the access points will not be available any more, as filters and other passive components will also be implemented on-chip. In such cases, there will be a need to put the sensors, which is the proposition in this paper

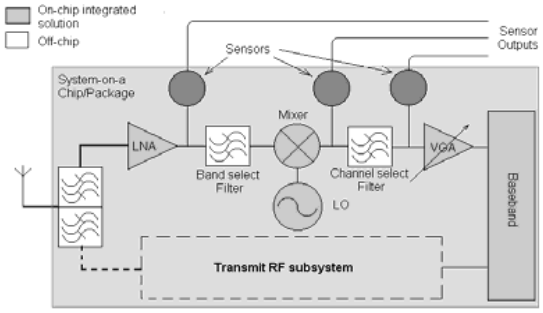

Figure 3. Sensors placed for system specification test

3.3 Algorithm for optimal placement of sensors

In this paper, a novel algorithm has been proposed to determine the optimal placement of a set of available sensors, and achieve the best prediction of specifications from the sensor measurements.

The algorithm starts with all the sensors put at the access nodes of the system-under-test. For a fixed, predetermined test stimulus, the strategy is to use minimum number of sensors in such a way that the prediction accuracy does not reduce considerably, or increases compared to the accuracy obtained with all sensors used. Assuming the sensors to be on-chip, they experience the process variations in the same way, as does the DUT. Thus, multiple instances of the DUT and the sensors are created by perturbing the process parameters, and the responses for each instance are captured. A preliminary analysis is performed to find out which of the specifications cannot be predicted with reasonable accuracy even with all the sensors present. After eliminating such specifications, a non-linear model relating the reduced set of specifications and measurements is constructed.

To reduce the measurement set, i.e. the number of sensors required, the measurements are checked if they bear sufficient linear correlation with the remaining specifications. The assumption here is that even though the relation between a measurement and a specification is non-linear, there exists a strong linear relationship between them. In case where there is not a strong correlation between the specification and a sensor measurement, the likelihood of predicting the specification using the specific measurement is low. So, the measurement having lowest correlation with all the specifications is eliminated from the list of measurements. Next, a non-linear model relating the rest of the measurements and specifications is built. The model is compared to the previous one to see if the prediction accuracy has improved or not, and accordingly the measurement is retained or removed from the measurement set. Proceeding in this way, the measurement set is reduced until no further gain in accuracy can be achieved. The core algorithm is shown in Figure 4.

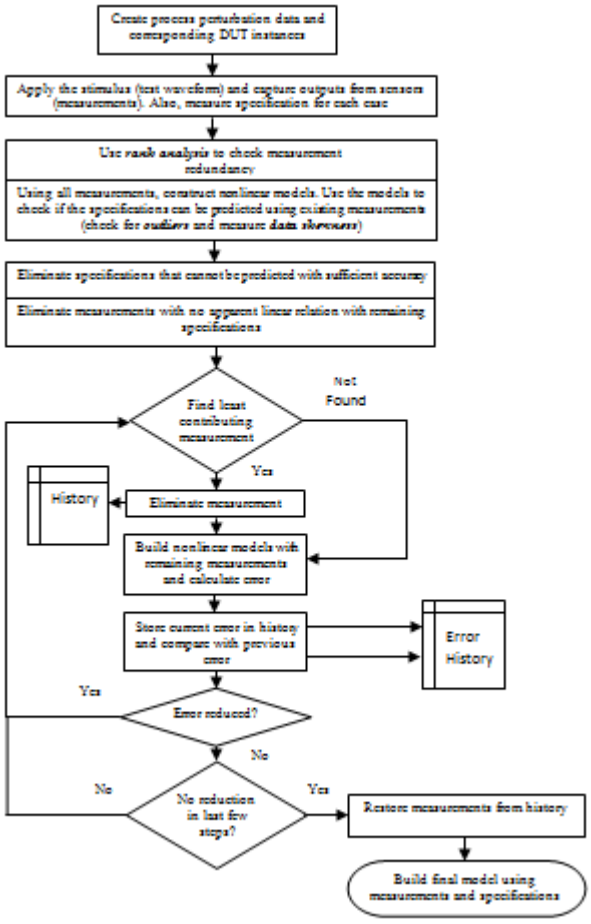

Figure 4. Flowchart

IV. CONCLUSION

In this paper, an algorithm is presented on how to place a set of available sensors at the outputs of a system under- test to get maximum accuracy in prediction of a set of target specifications. First, the concept was proved on a state-variable filter and was further extended to a wireless receiver sub-system. It was also observed that the error in prediction reduces when the sensor measurements are combined with the outputs of the system-under-test. This study proves that using sensors for specification measurement of RF and microwave is indeed the way to go. At higher frequencies, this approach can prove to be useful as a BIST solution to the RF test problem. At present, we are in the process of designing more sensors that can operate at RF frequencies.

REFERENCES

[1] M.Ehsanian, B.Kaminska, K.Arabi, "A new digital test approach for analog-to-digital converter testing"

[2] C.L.Wey, "Built-in self-test (BIST) structure for analog circuit fault diagnosis"

[3] Alan V.Oppenheim and Ronald W.Schafer, "Discrete-Time Signal Processing"

[4] J. H. Friedman, "Multivariate Adaptive Regression Splines", The Annals of Statistics, vol. 19, no. 1, 1991,

[5] Behzad Razavi, "RF Microelectronics"

[6] L.Carro, E.Cota, M.Lubaszewski, Y.Bertrand, F.Azais, M.Renovell, "TI-BIST: a temperature independent analog BIST for switched-capacitor filters"

[7] M.F.Toner, G.W.Roberts, "A BIST scheme for a SNR, gain tracking, and frequency response test of a sigma-delta ADC"

[8] A.A.Hatzopoulos, S.Siskos, J.M.Kontoleon, "A complete scheme of built-in self-tests (BIST) structure for fault diagnosis in analog circuits and systems"

[9] A.Walker, P.K.Lala, "A dual edge transition based BIST approach for passive analog circuits"

[10] J.Velasco-Medina, I.Rayane, M.Nicolaidis, , "AC/DC BIST for testing analog circuits"

[11] M.F.Toner, G.W.Roberts, "A frequency response, harmonic distortion, and intermodulation distortion test for BIST of a sigma-delta ADC"

[12] P.N.Variyam, A.Chatterjee, "Digital-compatible BIST for analog circuits using transient response sampling" A.C.Nacul, L.Carro, D.Janner, M.A.Lubaszewski, "BIST procedure for analog mixers in software radio"

[13] J.Velasco-Medina, I.Rayane, M.Nicolaidis, "On-line BIST for testing analog circuits" International Conference on Computer Design (ICCD), pp. 330 - 332,Oct. 1999.

[14] S.Khaled, B.Kaminska, B.Courtois, M.Lubaszewski, "Frequency-based BIST for analog circuit testing"

[15] C.L.Wey, S.Krishman, "Built-in self-test (BIST) structures for analog circuit fault diagnosis with current test data" IEEE Transactions on Instrumentation and Measurement, Volume 41, Issue 4.

[16] M.Negreiros, L.Carro, A.A.Susin, "Ultra low cost analog BIST using spectral analysis" VLSI Test Symposium.

[17] S.Dragic, I.Filanovsky, M.Margala, "Low-voltage analog current detector supporting at-speed BIST" *International Symposium on Circuits and Systems* (ISCAS), Volume 1,