Multiple Gate Silicon – On – Insulator MOSFET Technology

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***Abstract*—**This paper presents a review of the development of SOI – MOSFET from single gate device to multiple gate devices. The physical structure of Double and Triple gate SOI – MOSFET is discussed along with the operation, advantages and drawbacks. ment is a "live" template. The various components of your paper [title, text, heads, etc.] are already defined on the style sheet, as illustrated by the portions given in this document.

Keywords*-SOI – MOSFET, Fully depleted, Partially Depleted, DELTA, Trigate,*

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I. INTRODUCTION

The single gate Silicon – On – Insulator MOSFET (SOI MOSFET) is categorized into Partially Depleted (PD) and Fully Depleted (FD) structures [1]. The PD – SOI is affected by phenomenon generally called floating body effects, which are suppressed to certain extent in the FD – SOI. The floating body effects viz. Kink effect, single transistor latch phenomenon give undesirable behavior at high switching speeds. With continuous miniaturization of electronic components it became necessary to improve the current driving ability of device and simultaneously reduce floating body effects. This led to the development of SOI – MOSFET with multiple gate terminals.

II. DOUBLE GATE SOI –MOSFET

"Volume Inversion" [2] occurs in the Double Gate SOI devices when thin film of silicon is sandwiched between Gate oxide and buried oxide, and the bulk silicon substrate is used as secondary gate. The biasing of the secondary gate uniformly distributes of the field potential in the thin silicon film, resulting in volume inversion and increasing current drive, transconductance and carrier mobility.

The first fabricated Double gate SOI – MOSFET named Depleted Lean channel Transistor (DELTA) [3], shown in fig. 1 (a) and 1(b) was reported in 1989. In DELTA the channel is thin and vertical, unlike the flat horizontal channel in earlier devices and single Gate itself covers the channel from both sides.

The presence of Gate terminal on either side uniformly distributes potential along the channel giving DELTA better characteristics [4]. In Fig 1(b) black arrow indicates direction of Drain current.

The Gate All Around MOSFET (GAA – MOSFET) [5], shown in Fig 2(a), was the first planar double gate SOI – MOSFET.

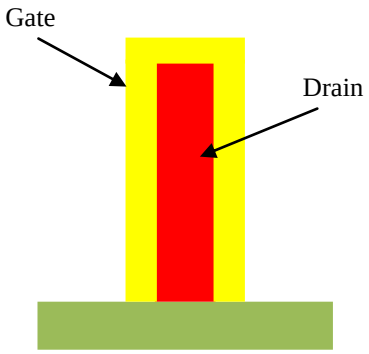

Fig. 1(a) Side view of double gate SOI – MOSFET DELTA

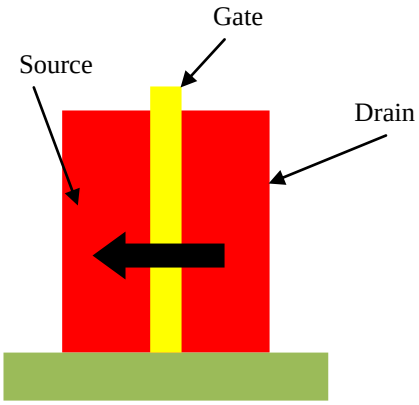

Fig. 1(b) Front view of double gate SOI – MOSFET DELTA

With Gate terminals at Top and Bottom of the channel as shown in fig 2(a), the effective width of Gate increases volume inversion resulting in higher current drive and transconductance [6], as compared to earlier bulk devices.

 ISSN: 2321-8169
1574 – 1576

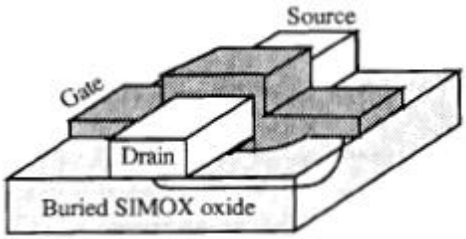

Fig. 2(a) Gate All Around SOI – MOSFET

. The width of depletion gets reduced, hence reducing the threshold voltage V_t described by the expression [7] below.

$$V_{t\,(p+\,-\,p+)} = V_{FBp} + 2\varphi_F + 0.5(1 + 4C_{Si}/\beta.Q_{Si})Q_{Si}(1/4C_{Si} + 1/C_{Ox}) + (1/\beta)\ln(4C_{Si}/\beta Q_{Si}) \quad (1)$$

where V_{FBp} is flat band voltage for p+ poly gate given by

$$(1/\beta) = k_B.T/q$$

$$V_{FBp+} = (1/\beta)\ln(N_{p+poly}/N_A)$$

$$\varphi_F = (1/\beta)\ln(N_A/N_i);\ Q_{Si} = q.N_A.t_{Si};$$

$$C_{Si} = \varepsilon_{Si}/t_{Si};\qquad C_{Ox} = \varepsilon_{Ox}/t_{Ox} \quad (2)$$

with k_B as Boltzmann constant and T is absolute temperature.

However for the planar double gate devices there was considerable difference in the threshold voltage V_t for MOSFET with p^+-p^+ polysilicon gate and MOSFET with n^+-n^+ polysilicon gate [8]. Hence to further improve the current drive for low voltage application, the structure with p^+ poly for top Gate terminal and n+ poly for lower Gate terminal as shown in fig. 2(b) was developed [9].

The difference of flat band voltages between n^+ and p^+ gates causes in a gradient distribution of potential hence forming inversion layers on the inside of respective gates. Due to which there is less difference between the threshold voltages of 2 types of device.

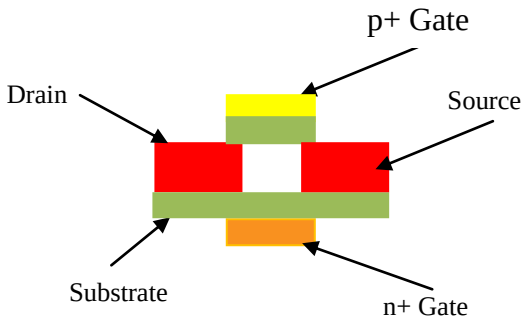

Fig. 2(b) p^+ - n^+ planar Double Gate SOI – MOSFET

III. Triple Gate SOI MOSFET

The Triple Gate SOI MOSFET named Quantum Wire SOI MOSFET [10] is logical development of the Double Gate SOI MOSFET. Its modified and improved versions are the Pi-Gate [11], and Omega-Gate [12] devices.

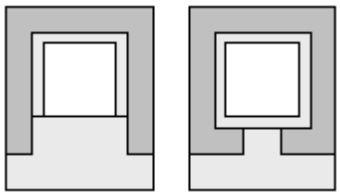

Fig. 3 Pi-Gate and Omega-Gate SOI – MOSFET

As shown in fig.3 these devices had the Gate extended into the buried oxide, giving rise to structure looking like Greek alphabets π and Ω, and hence the names.

IV. Conclusion

It is clearly evident from the foregoing discussion that with an increase in number of Gate terminals the performance of device has improved considerably. However considering the necessity for further reducing the device size, new technology processes or material characteristics will be required to be developed for improvement of performance at still lesser dimensions.

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