A REVIEW ON REDUCING JITTER AND POWER IN PHASE LOCKED LOOP

Meenakshi Tiwari[1], Himadri Singh Raghav[1] *(Member IEEE)*, Prof. B.P. Singh[2] *(Member IEEE)*
[1, 2] *Electronics and communication Engineering Department MITS (Deemed University)*
Lakshmangarh-332311, Dist. Sikar, Rajasthan, India
tiwari.meenakshi1@gmail.com, himadri.singh.raghav@gmail.com, bpsingh@ieee.org

Abstract*— *Jitter is extremely important in PLL based systems. The effects of jitter range from not having any effect on system operation to rendering the system completely non-functional. Reducing Jitter and power supply is one way to help to improve the system performance. This review will concentrate on jitter and power supply in PLL building blocks.

Keywords- - LOW POWER, LOW JITTER, PFD, PLL

*****

I. INTRODUCTION

An early description of PLL appeared in the papers by Appelton [1] in 1923 and de Bellescize [2] in 1932. In the late 1970's, the theoretical description of PLL was well established [3], [4], [5] but PLL did not achieve widespread use until much later because of the difficulty in realization. With the rapid development of integration circuits[IC's] in the 1970's, the applications of PLL were widely used in modern communication systems. Since, then PLL has made much progress and has turned its earlier professional use in high precision apparatuses into its current use in the applications of clock generation, time synchronization and clock multiplication.In PLL based system jitter is a big issue. Reducing jitter and power in phase lock loop is becoming essential for portable and battery operated compact electronic devices, which decreases the risk of reliability problems. In recent years, the design of low power and low jitter PLL for the different application has become one of the greatest challenges in high performance very large scale integration (VLSI) design. As a consequence, many techniques have been introduced to minimize the power and reduction in jitter of new VLSI circuits. We shall therefore, in the following paragraphs, discuss theoretical backgrounds and summarize all the accessible experimental results to provide the leading lines for the design of low-jitter and low-power PLL systems.

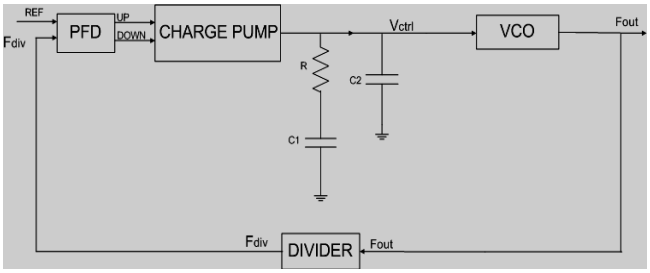

Fig. Basic components of PLL[6]

II. TECHNIQUE FOR REDUCING JITTER AND POWER SUPPLY

This section investigates the reduction of jitter and power supply in phase locked loop by various approaches.

A. JITTER IN PHASE FREQUENCY DETECTOR AND LOOP FILTER

Phase frequency detector is the first block of the PLL system, Abishek Mann. *et al.* [6], Redesigning of individual blocks like: Phase Frequency Detector to reduce area and static phase error, Voltage to Current converter to linearly increase the current input to the current controlled oscillator, Current Controlled Oscillator to reduce phase noise, amplitude distortion, area and power consumption, an additional feedback loop to increase the gain of the charge pump in a manner that linearizes the overall loop gain over wide bandwidth.In this paper a high speed low

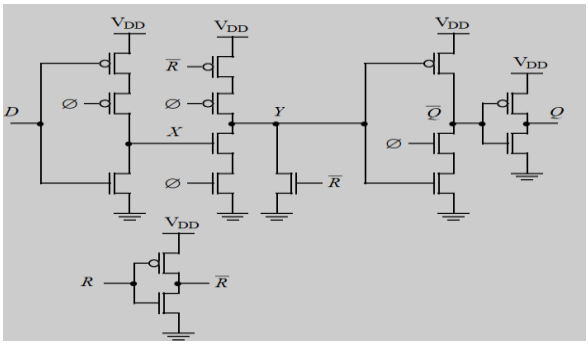

Fig. Implementation of TSPC D flip flop with low true Reset[6] power phase frequency detector is proposed using TSPC positive edge triggered D flip-flop with no extra circuits added.The operating range of this PFD upto 1GHZ with 1.8v power supply using 0.18um technology. The Proposed architecture reduces dead zone (less than 30ps), steady state error, area and power consumed. But here, Kruti P. Thakore et al. [7], proposed high speed phase frequency detector with charge pump and second order loop filter for low jitter and low power phase lock loop using 0.18µm CMOS technology with 1.2v power supply and 1GHz input frequency. The jitter of the proposed design is reduced only to 2ps and the total power consumption of the circuit is 22µwatt. The author presented a high speed phase frequency detector instead of traditional phase frequency detector which detects the phase and frequency difference between two inputs. High speed PFD detects both the edges of the PFD. Here the PFD is operated at 1GHZ frequency and the lock condition of the PFD with dead zone is shown [7]. Due to this dead zone problem at the output jitter will create and the sensitivity of the PFD is affected. In this case the sensitivity of the means the smallest difference the PFD can detect and produce at the output UP or DOWN signal. This led to the conclusion that the higher the sensitivity the better the PFD. Traditional PFD has very big dead zone and so the jitter. The power consumption of the traditional PFD is quit high. So, the author used high speed PFD with lower jitter and power.

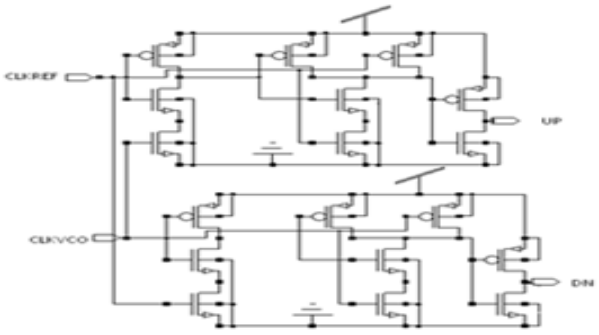

Fig. High speed Phase frequency detector [7]

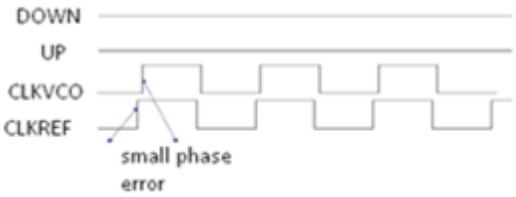

Fig. Dead Zone[7]

B. JITTER IN CHARGE PUMP

Reducing jitter caused by the transistor leakage compensation circuit technique, Kyung Ki Kim *et al.* [10], proposed a nanoscale CMOS PLL design using a 32nm CMOS technology is described, where low jitter performance is achieved using compensation circuits to reduce power supply noise effect on VCO output frequency and the leakage current in the charge pump. The proposed PLL with the compensation circuit blocks for leakage current and PSN[10]. The PLL in this paper includes the leakage compensator, the PSN compensator. The leakage compensator effectively improves the jitter performance of the conventional PLL in nanometer technology. The leakage compensation consists of two charge pump replicas and current mirrors. Using the UP/DN signals from the PFD and two bias voltages of charge pump, the leakage compensator senses the leakage current of the charge pump circuit and generates the same amount of current as the leakage current of the charge pump. However, the directions of the generated leakage current are opposite to those of the leakage current in the charge pump. That is how the leakage current of the charge pump is cancelled through the leakage compensator.The leakage compensator providing the PLL with better performance by reducing jitter. The proposed compensation uses a 0.9V power supply voltage and proposed PLL achieves an 88% jitter reduction at 440MHz output frequency and compared to the PLL

without leakage compensator and its output frequency drift is little to 20% power supply voltage variations.

C. JITTER IN VCO

Jonathan Cheung [11], author proposed a novel delay element to minimize the supply/substrate noise, as VCO is sensitive to this noise. He proposed a schematic diagram of the pseudo differential delay element with an auxiliary circuit shows two single ended inverters behave like one differential delay element. This single-ended delay element provides full-swing outputs without the need of additional buffers. The number of delay elements is only half that of the required phases, which the virtue of differential delay elements is. The power consumption of the VCO is substantially reduced and this compact and feasible circuit behaves as a differential circuit, and is thus immune to supply and substrate noise in itself. [9].

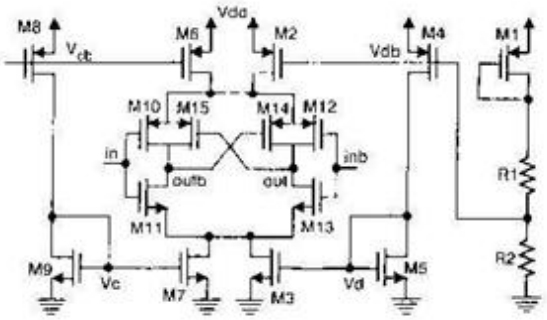

Fig. Pseudo differential delay element with auxiliary circuit [9] Nidhi Thakur [8], proposed a modified ring oscillator for reducing jiiter and power. Among many other oscillator topologies the ring oscillator is attractive for its high frequency, wide range of operation and small die size. A ring oscillator consists of multiple stages of delay cells. Delay cell can be design with differential pair and CMOS inverter. In this paper CMOS inverter is used as a delay cell [8]. In this a voltage control oscillator is designed and simulated in 50nm CMOS technology and the frequency of oscillation of the VCO is 2.6GHz and the center drain current of 64uA is used. Tuning range is of 72% and the jitter is of 39.8pS which is much better reults reported earlier. At 2.56 GHz the average power consumption is 0.064mW at 1V supply voltage which is also much lesser compared to 65nm and 180nm designs. The jitter for the circuit is 39.8pS.

CONCLUSION

This work presented an extensive analysis on Phase Locked Loop circuit design methodologies for reducing jitter and power supply. In Phase Locked Loop, reducing jitter and power supply is a major issue, it degrade the performance of the circuit. Several techniques have been proposed in the literature for reducing jitter and power supply to make PLL wide range, either by employing a VCO based on pseudo- differential delay elements, incorporating the merits of both single ended and differential-type VCOs ,by modified a ring oscillator having multiple stages of delay cells or by using high speed phase frequency detector with charge pump and loop filter and by taking the advantage of decoupling capacitor structure for reducing power supply noise. Although many methods have been proposed in Phase Locked Loop for Low Jitter and Low Power, many issues still exit and there are still many challenges need to be solved in the PLL systems.

TABLE : Results generated for power and jitter in phase locked loop blocks.

	Phase frequency detector	**Charge pump**	**Voltage controlled oscillator**
Operating voltage	***1.2v***	***0.9v***	***1v***
Technology	***180nm***	***32nm***	***50nm***
Power consumption	***22uW***	***-***	***0.064mW***
Jitter	***2ps***	***5ps***	***39.8ps***
Maximum frequency	***1GHZ***	***440MHZ***	***2.6GHZ***

REFFERENCES

[1] E.V. Appleton, “Automatic synchronization of triode oscillators”, in Proc. Cambridge Phil. Soc.,vol. 21, pt. 3rd,p. 231,1922-1923.

[2] H.de Bellescize,“La reception synchrone”,Onde Electr.,vol. 11,pp. 230-240. June 1932.

[3] A. Blanchard, “Phase Locked Loops:Application to Coherent Receiver Design.New York: Wiley,1976

[4] F.M. Gardner, Phase Lock Techniques, 2nd Ed. New York: Wiley, 1979.

[5] W.C. Lindsey and C.M.Chie, "A Survey of digital phase-locked loops",Proc. IEEE,vol. 69, pp. 410-431, Aprl. 1981.

[6] Abishek Mann,Amit karalkar,Lili He and Morris Jones, "The Design of A Low Power Low-Noise Phase Lock Loop",IEEE2010.

[7] Kruti P. Thakore,Harikrishna C. Parmar, Dr. N.M. Devashrayee, "High Speed PFD with Charge Pump and Loop Filter for Low Jitter and Low Power PLL",IJECT Vol.2,Issue 2,June2011.

[8] Nidhi Thakur, "Design of Low Power Low Jitter Ring Oscillator Using 50nm CMOS Technology",IJSER Vol.3,Issue 3,03 march 2012.

[9] S. Park, Y. Choi, S.G. Lee, Y.J.Jung, S.C. Park and W. Kim, "Low-jitter phase-locked loop based on pseudo-differential delay elements", Electronics Letters, Vol.37, No.11,May 2001.

[10] Kyung Ki Kim and Yong-Bin Kim, "A 32nm and 0.9v CMOS Phase-Locked Loop with Leakage Current and Power Supply Noise Compensation",march 2007.

[11] B. Razavi, .Design of Analog CMOS Integrated Circuits,. McGRAW-HILL, 2001.

[12] Jan M. Rabey, "Digital Integrated Circuits", second edition,2003.

I.