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Design and FPGA Implementation of Channelizer & Frequency Hopping for Advanced SATCOM System

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***Abstract*— Advanced satellite communication systems should be capable of preventing unauthorized access or exploitation of communication services by adversaries. This can be achieved by use of wideband multi-channel digital transceivers which employ channelizer to extract the channel of interest from digitized RF bands for further baseband processing. Various anti-jamming techniques like Frequency hopping are used to prevent the systems from intentional jamming by the hostile systems. This paper presents an efficient channelizer architecture which supports wideband as well as narrowband channels with programmable channel bandwidth followed by frequency hopping for the proposed SATCOM system. The target design is a flexible channelization unit which divides the incoming data links of 11 MHz bandwidth into two data links in granularity of 0.5 MHz depending upon user requirements. First link is further sub-channelized into two sub-links each having a bandwidth of 25 KHz that is frequency hopped at a user programmable rate with desired random sequence. The same channelizer can be well applicable in any software defined radio receiver platforms due to flexibility of the design. Proposed design is tested on target hardware Xilinx Virtex-IV FPGA xc4vsx35-10ff668. The design and implementation of the channelizer and frequency hopping technique are discussed in detail.**

Keywords-channelizer, frequency hopping, ddc, cic, fpga.

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I. INTRODUCTION

Satellite based communication system serves well for providing personal communication globally. These systems are prone to intentional jamming by the unauthorized systems. Hence, advanced satellite communication systems, which incorporate various anti-jamming techniques like frequency hopping to combat jamming, are required for applications requiring a robust communication free from any interception of communication signals by the jammer. These systems incorporate wideband multi-channel transceivers capable of supporting multiple channels per RF band. Typically a channelizer is used to extract the independent communication channels from digitized RF bands. There are mainly three predominant architectures available for channelization, namely Poly-phase FFT filter banks (PFFB), Frequency Domain Filtering and Digital Down Conversion (DDC) technique [1]. Although PFFB channelization technique is efficient in terms of computational complexity, it is limited to channel structures consisting of equally spaced channels. In general, number of channels must be equal to the decimation rate and sampling rate must be power of two times the baseband bandwidth. This technique is not well suited for transceivers supporting flexible channel architectures. Frequency Domain Filtering and Digital Down- Conversion (DDC) channelization techniques offer similar capability in terms of flexibility for any type of channel spacing and bandwidth but Frequency domain filtering approach makes use of FFT which are computation intensive. Also, mixing operation is performed on the block of data vs. continuous time processing which makes zero carrier offsets for individual block of data, creating a rotating phase offset between each block if the carrier cycle at the A/D sample rate is not an integer number of block size. Hence, DDC based channelization technique is employed for supporting flexible channel architectures for the proposed system. This paper will explain the design and FPGA implementation of a flexible channelization unit based on DDC technique which supports both wideband as well as narrowband channelization with programmable channel bandwidth followed by frequency hopping which is the most crucial elements in any advanced satellite communication systems. The flexibility incorporated in the design makes it also applicable for any wideband transceiver for software defined radio platform.

The remainder of this paper is outlined as follows. Section II discusses the system architecture and the frequency plan of proposed SATCOM system. In Section III, the design and implementation of the channelizer is described. Section IV, illustrates the design and implementation of frequency hopping technique. Section V shows the hardware test setup with specifications used in the design and analysis of results followed by Section VI which concludes the paper.

II. PROPOSED SYSTEM ARCHITECTURE

The basic block diagram for the proposed wideband satellite communication system is presented in Figure 1. It comprises RF Front-end (consists of antenna section for transmission & reception of RF signals, RF to IF down-converter for converting RF down to Intermediate Frequencies) and the digital subsystem for further digital signal processing.

In this paper, receiver side of onboard system is emphasized to show the capabilities of flexible channelizer which extracts the channel of interest from digitized RF bands for further baseband processing in FPGA. This process is reversed on the transmit side where individual channels are combined and retransmitted. A single channelization unit supports multiple channels which can be wideband or narrowband channels. The channelized narrowband signals are frequency hopped at user programmable rate depending upon the system specifications.

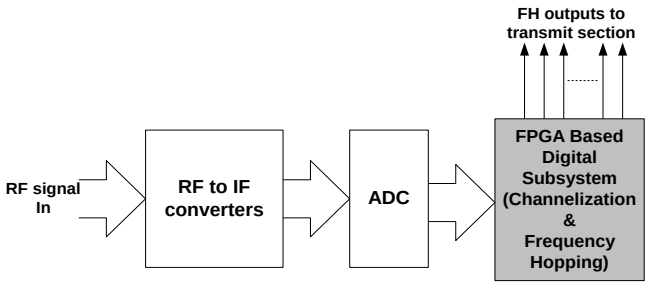

Figure 1: Basic block diagram of proposed SATCOM System

The flexible frequency plan for the proposed SATCOM system is presented in Figure 2 for hardware proof of concept (POC). Incoming data links occupies a total of 11 MHz bandwidth which is divided into two wideband channels in granules of 0.5 MHz depending upon the user requirements. These wideband channels are further sub-channelized into two narrowband channels in granules of 25 KHz which can reside anywhere inside a wideband channel.

Implementation of individual blocks of channelizer architecture in FPGA with the specifications as described in Table I is discussed in the next section.

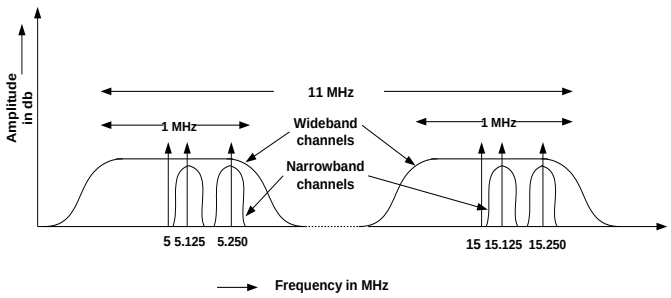

Figure 2: Frequency plan

TABLE I. SPECIFICATIONS OF TEST INPUTS

Parameter	Specifications
No. of Wideband Channels	2
No. of Narrowband Channels	2
Wideband Channel Center Frequencies (CH1,CH2)	5 MHz, 15 MHz
Narrowband Channel Center Frequencies (subCH1,subCH2)	5.125 MHz, 5.250 MHz
Wideband Channel BWs	1 MHz
Narrowband Channel BWs	25 KHz
Signal Power	-5 dBm

III. DESIGN OF CHANNELIZER USING DDC

The proposed channelizer architecture is based on the Digital Down Conversion (DDC) technique which is an integral part of any digital communication receiver. In this technique, the incoming digitized RF wideband signal is shifted from its carrier frequency down to baseband through mixing with a synthesized carrier at or near the carrier frequency of that signal. The resulting signal is then filtered and decimated to extract the channel of interest [2]. This technique reduces the amount of effort to a great extent for subsequent processing of the signal without loss of any information. Figure 3 illustrates the basic block diagram of a typical DDC.

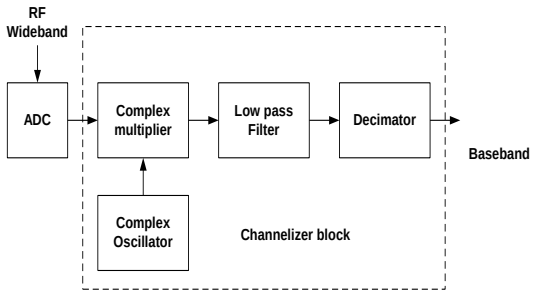

Figure 3: Basic DDC Architecture

The advantage of using DDC approach is the flexibility in choosing the carrier frequency and channel bandwidth.

The Cascaded Integrator Comb (CIC) filter is used instead of low pass FIR filter and decimator is proposed in channelizer architecture for extracting wideband channels as well as narrowband channels. CIC Filter inherently provides decimation in addition to low pass filtering so that the processing requirements for subsequent stages are relaxed. The filter bandwidth can be programmed to the user requirements by only changing the decimation factor. Post-filtering is done to compensate for the pass band droop. The advantage of CIC filter is that it supports multiplier less filter

architecture which reduces the hardware complexity in any FPGA based design.

Figure 4 shows the wideband and narrowband channelizer architecture utilizing DDC technique [2]. First, the wideband signal is filtered and decimated down to the desired channel bandwidth through wideband channelizer. The decimated signal is then passed to narrowband channelizer to extract the narrowband channel of interest. Although, both channelizers have similar architecture but narrowband channelizer works at a low processing rate than that of wideband channelizer.

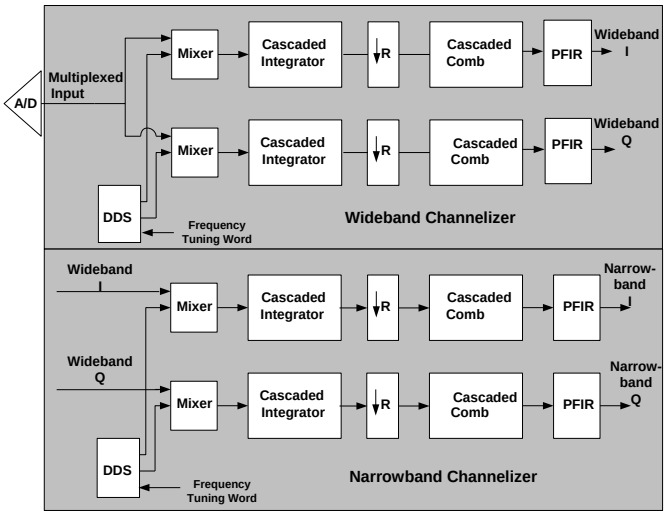

Figure 4: Wideband and Narrowband Channelizer Architecture using DDC Technique

A. *Implementation of Mixer*

The Mixer multiplies the multiplexed input data samples with the synthesized carriers at or near the carrier frequency of the channel of interest to bring the desired channel to the baseband level. The output of the mixer contains both the sum and difference frequency components at incoming sample frequency. The mixer used in this design is desired to run at the sample frequency of ADC for hardware proof of concept. The following Table II summarizes the mixer specifications**.**

TABLE II. MIXER SPECIFICATIONS

Parameter	**Specifications**
Input Data Bits	14 bits
Carrier Bits	10 bits
Sample Frequency of ADC	125 MHz
Center Frequency of CH1	5 MHz
Center Frequency of CH2	15 MHz
Center Frequency of subCH1	125 KHz
Center Frequency of subCH2	250 KHz

B. *Implementation of Direct Digital Synthesizer*

The Direct Digital Synthesizer (DDS) is designed to generate the sine and cosine carriers required to mix with the digitized multiplexed input data. The sine signal is used to generate the in Phase component while the cosine generates the quadrature component of the complex signal. The DDS has to be clocked at the sample frequency so that sine and cosine data are presented to the mixers at the same rate as that of input data. Figure 5 illustrates a typical DDS architecture. Quarter Wave Symmetry is utilized to reduce the size of Sine/Cosine lookup table for FPGA implementation to minimize no. of block memories. Phase dithering is employed to get better frequency response. Table III summarizes the DDS specifications for the frequency plan mentioned in Figure 2.

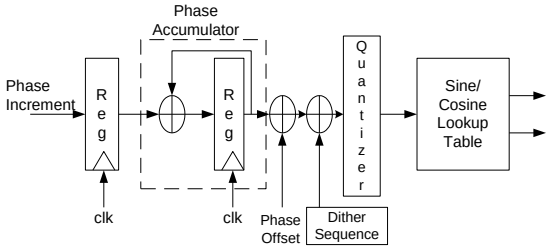

Figure 5: Architecture of DDS in FPGA

TABLE III. DDS SPECIFICATIONS

Parameter	**Specifications**
Sample Frequency	125 MHz
Phase Increment Word length	32 bits
Output Bit Width	10 bits
Carrier Frequency for CH1	5 MHz
Carrier Frequency for CH2	15 MHz
Carrier Frequency for subCH1	125 KHz
Carrier Frequency for subCH2	250 KHz

C. *Implementation of CIC and Post FIR filter*

In DDC architectures, two major functions namely low pass filtering and decimation are necessary for further signal processing. Low pass filtering is required immediately after Mixer to remove the unwanted signal frequencies that would arise due to mixing function and the decimation is essential for reducing the incoming sample rate to the minimum required to relax the signal processing requirements for subsequent stages.

CIC filter is an efficient way of performing decimation along with filtering. Figure 6 shows the CIC filter structure consisting of N cascaded integrator stages clocked at sample frequency f_s, followed by a rate change by a factor R, followed by N cascaded comb stages running at (f_s/R) where N is the number of stages or the filter order [3][4]. CIC filters are hardware efficient filter structures as they use only shifters and adders to perform the filtering function as shown in Figure 6.

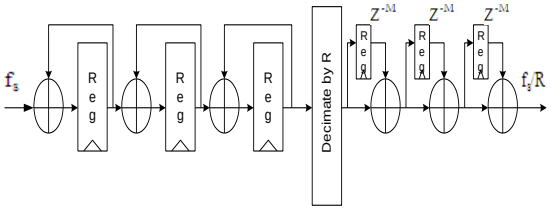

Figure 6: CIC Decimator Filter Architecture

The present filter has a frequency response given by

$$H(f) = [\sin(\pi fR)/\sin(\pi f)]^3 \quad \text{----- (eq.1)}$$

Where f is the normalized frequency relative to the input sample rate and R is decimation rate.

The filter passband bandwidth is controlled by the decimation factor R which can be user programmed to provide the flexible bandwidth. The filter parameters for the frequency plan mentioned in Figure 2 are described in Table IV.

TABLE IV. CIC FILTER SPECIFICATIONS

Parameter	Specifications
Input Sample Frequency	125 MHz
No. of Stages (N)	3
Differential Delay (M)	1
Rounding	Convergent

Post finite impulse response (PFIR) filter is required after the CIC filter stage to compensate for the passband droop. It can be single rate or multi-rate filter structures. The filter length for each filter ranges from 0 to 1024 taps. The coefficient precision may also be customized and ranges from 1 to 32 bits. The full-precision results are not passed between adjacent processing stages, bias-free convergent rounding is employed for this process.

As per the frequency plan in Figure 2, the wideband channel present at 5 MHz and 15 MHz are extracted through wideband channelizer and the narrowband channelizer filters out the narrowband channels present at 5.125MHz and 5.250 MHz each having 25 KHz bandwidth. The narrowband channels are then frequency hopped to user programmable rate.

IV. DESIGN OF FREQUENCY HOP UNIT

Advanced satellite communication system demands prevention from any jamming scenario. The hostile systems try to intercept the transmitted signal and disrupt the communication channel. Frequency hopping (FH) technique is an efficient anti-jamming technique employed in SATCOM systems as it is relatively easy to operate over large spectral bands [7].

Frequency Hopping indicates that transmitter and receiver change frequency rapidly in a defined pattern which is known to the transmitter and receiver. A pseudo-random code generator is used as a driver for a frequency synthesizer (DDS) at the transmitter to pseudo-randomly hop the carrier frequency of the narrowband signal extracted through the narrowband channelizer unit as shown in Figure 7.

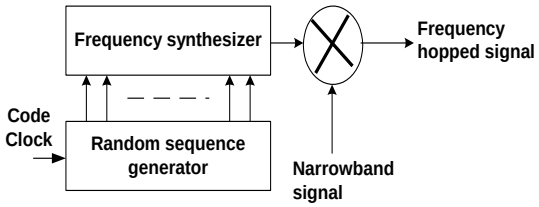

Figure 7: Frequency Hop Unit

The hopping code selection is very critical in any communication systems. It should have a large period, large seed and random appearance to provide design secrecy. It should possess large linear complexity so that jammer intervention is negligible. The minimum hopping rate is decided based upon the jammer location w.r.t. transmitter and receiver [5].

In this design, slow frequency hopping method is used where hop period is long with respect to a data bit period. Each narrowband channelizer output is frequency hopped as per the specifications mentioned in Table V.

TABLE V. SPECIFICATIONS FOR FREQUENCY HOP

Parameter	Specifications
Hop Rate	500 Hops/s
Input Channel Bandwidth	25kHz
Total Output Bandwidth	1000 kHz
No of Channels	2
Hopping Sequence	Programmable

V. RESULTS AND DISCUSSIONS

A Simulink model is developed for proof of concept of the proposed channelizer architecture with specifications mentioned in Table I. It consists of wideband transmitters generating two channels of 1MHz modulation bandwidth at 5MHz and 15MHz IF's. The combined channel output spectrum fed to the two channel receiver containing the proposed channelizer which extracts individual channels from the combined spectrum resulting in zero BER as shown in Figure8. Similar model is designed and tested for narrowband channelizer. Various design parameters are simulated using Simulink model so that hardware implementation becomes easier.

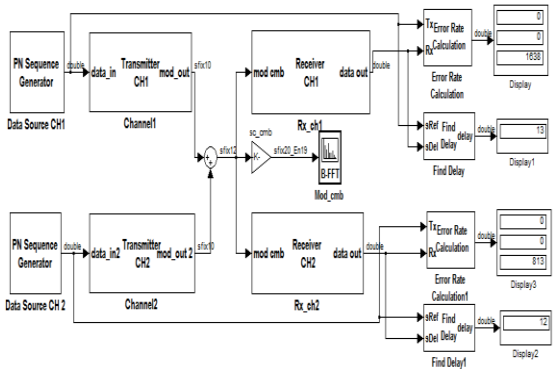

Figure 8: Channelizer Design in Simulink

The entire design is implemented using Verilog HDL 2001 without the use of any FPGA IP core so that the design becomes platform independent and portable to any FPGA like Xilinx or Actel. However, FPGA implementation is done using XilinxISE9.2i and functional simulation is carried out in Questa Sim 10.0b targeting Xilinx Virtex-4 FPGA xc4vsx35-10ff668 for hardware POC.

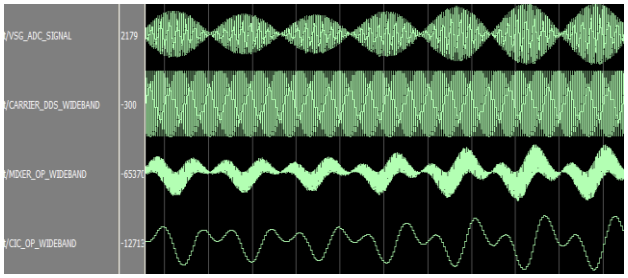

Figure 9: Functional Simulation Results for Wideband Channelizer

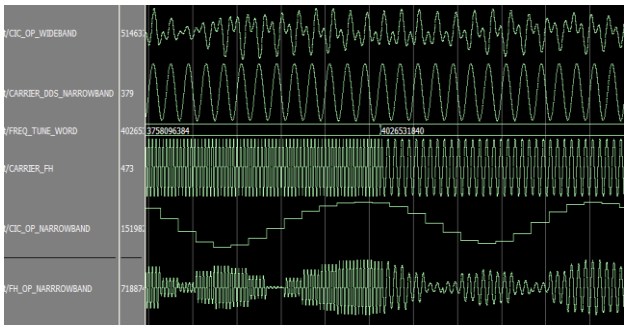

Figure 10: Functional Simulation Results for Narrowband Channelizer and FH

The Multichannel modulated signal as per frequency plan in Figure 2 generated from Vector Signal Generator (VSG) is passed through ADC of the FPGA based development board and the output is captured in Logic Analyzer. This data is stored in ROM of FPGA which is used as an input for simulation of the entire design. Results from Questa Sim are presented in Figure 9 and Figure 10 which show output signals from various stages of wideband and narrowband channelizers followed by FH unit. Both channelizers include synthesized carrier from DDS, Mixer output, CIC filter output followed by channelized output at baseband. FH unit includes frequency tuning word generated from PRBS generator and frequency hopped Narrowband signal output.

The hardware test setup is shown in Figure 11 which involves VSG for input signal generation and target FPGA board for processing of the signals. The channelizer and FH outputs from FPGA are passed through DAC of the board and results are observed using spectrum analyzer.

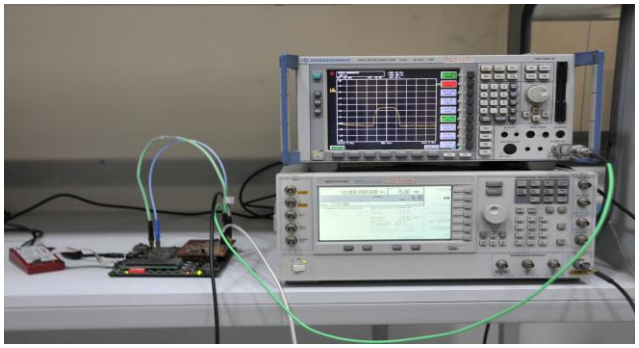

Figure 11 Hardware Test Setup

Figure 12 shows the multi-channel wideband spectrum containing two 1MHz bandwidth signals input to the channelizer which extracts the individual wideband channels. For better visualization and comparison, the extracted channel is frequency translated to the same center frequency as shown in Figure 13. The channelizer design is tested by varying input channel bandwidth to validate the flexibility of channel bandwidth. Figure 14 shows the channelizer output w.r.t. changing input channel bandwidth to 2 MHz. Narrowband signal is also generated from VSG as per the specifications mentioned in Table I and passed to the same channelizer which extracts the narrowband channel of 25 KHz bandwidth as shown in Figure 15.

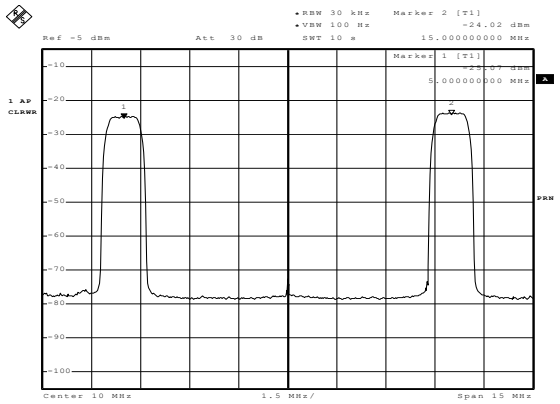

Figure 12: Multichannel Signal from VSG

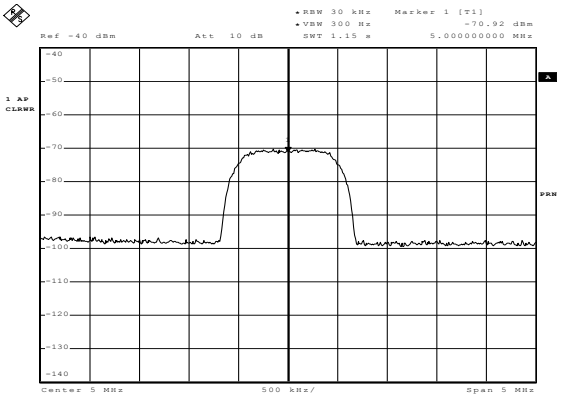

Figure13: Extracted 1 MHz Wideband Channel

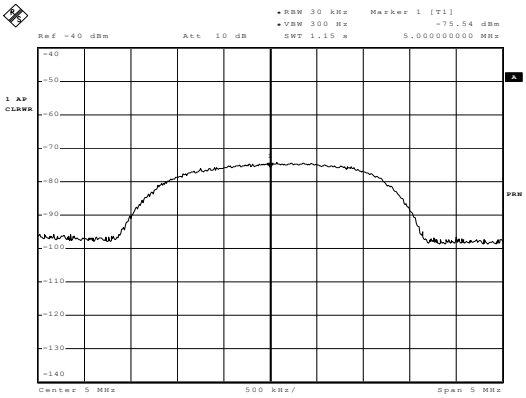

Figure14: Extracted 2 MHz Wideband Channel

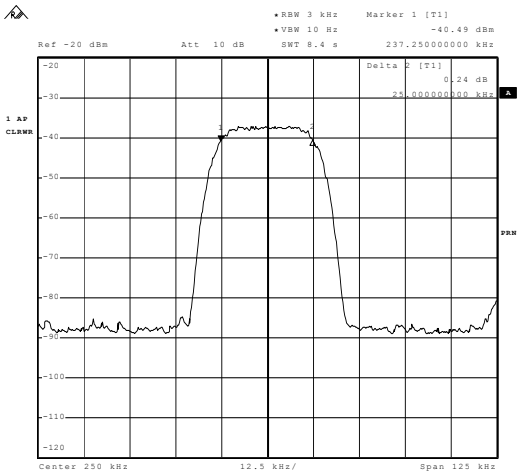

Figure15: Extracted 25 KHz Narrowband Channel

VI. CONCLUSION

A hardware efficient architecture of DDC based channelizer with frequency hopping applicable to advanced satellite communication system is presented in this paper. Channelization helps in extracting narrowband signal embedded in wideband signal in presence of interferer where Frequency hopping provides anti jamming margin for SATCOM systems. The same flexible channelizer architecture can also be applied to software defined radio platform. Proposed hardware architecture occupies only 13% area of total slices on target hardware Xilinx Virtex-IV FPGA xc4vsx35-10ff668. The design is made platform independent and can be ported on any target FPGA.

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