Implementation of Super-Capacitor on Multilevel Inverter .

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Abstract— This paper contains the response of Super-capacitor replacing battery as a source in Inverter and analysis of three level flying capacitor inverter topology. Multilevel Inverter are increasingly being used in medium and high power applications due to their advantages such as low power dissipation of power switches, low harmonic contents and switching redundancy. Super-capacitors have many advantages such as power density ,low impedance and good response of charging and discharging over battery. In two level Inverters, the applications of Super-capacitors as source likely to result into much better inverter output and provide a more acceptable topology, especially for portable futuristic systems. Description of future Super-capacitors (namely flexible, and suitable for integrated circuits)attracts the analysts further to recommend these for appropriate range of applications. Hardware result and MAT LAB-simulation is reported in this paper

Keywords- *Inverter, Super-capacitor, MAT LAB Simulation, Hardware.*

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I. INTRODUCTION

The preliminary studies on multilevel inverters (MLI) have been Performed using three-level inverter that has been proposed by Nabae. In the study, the third level has been constituted by using neutral point of DC line and the topology has been defined as diode clamped MLI (DC-MLI) [1,2]. In recent years, multilevel inverters have gained much attention in the application areas of medium voltage and high power owing to their various advantages such as lower common mode voltage, lower voltage stress on power switches, lower dv/dt ratio to supply lower harmonic contents in output voltage and current. Comparing two-level inverter topologies at the same power ratings, MLIs also have the advantages that the harmonic components of line-to-line voltages fed to load are reduced owing to its switching frequencies. The most common MLI topologies classified into three types are diode clamped MLI (DC-MLI), flying capacitor MLI (FC-MLI), and cascaded H-Bridge MLI (CHB-MLI). The hybrid and asymmetric hybrid inverter topologies have been developed according to the combination of existing MLI topologies or applying different DC bus levels respectively [4]. The basic topologies of MLIs are shown in Fig. 1. The recent applications of MLIs have a variety including induction machine and motor drives, active rectifiers, filters, interface of renewable energy sources, flexible AC transmission system (FACTS), and static compensators. The diode clamped inverters, particularly the three-level structure, have a wide popularity in motor drive applications besides other multilevel inverter topologies.

This paper deals with three level flying capacitor inverter topology with ultra-capacitor. Ultra-capacitors have many advantages such as power density and good response of charging and discharging over battery. In Inverters, the applications of ultra-capacitors are to result into much better inverter out acceptable topology

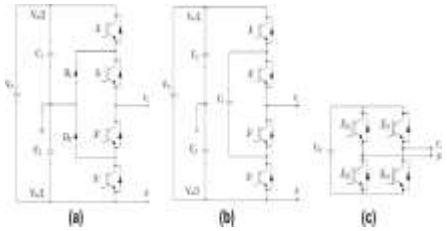

Fig. 1. Multilevel inverter topologies: (a) three-level DC-MLI, (b) three-level FC-MLI, (c) three-level CHB-MLI.

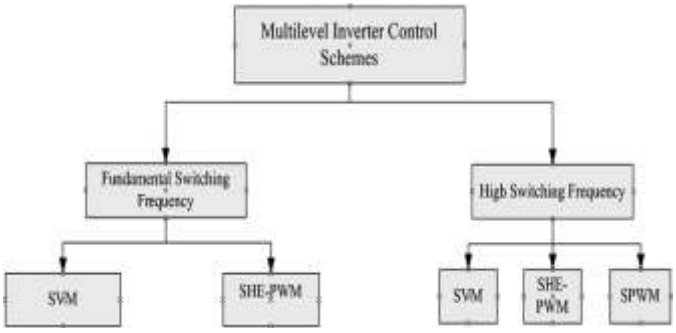

Fig. 2. Classification of multilevel inverter control schemes.

II. COMMON INVERTER TOPOLOGIES

Three major multilevel inverter structures which have been mostly applied in industrial applications have been emphasized as the diode clamped, the flying capacitor, and the cascaded Hbridge inverters with separate DC sources. In addition to this, various hybrid multilevel inverters have been developed by using the three basic types mentioned above.

Voltage source inverters (VSIs)are widely used in AC motor drives, AC uninterruptible power supplied (UPS), and AC power supplies with batteries, fuel cells, and active harmonic filters. VSI topologies are constituted in accord with power demand of application areas and output voltages are either single phase for power demands lower than 2 kV A or three-phase for power demands over 2 kV A as being used in household and Industrial loads.

The semi converter, half bridge and full bridge inverters were employed for high power applications in 1990s,

but recently many researchers have paid much attention to multilevel Inverters for high power and medium voltage applications[6]. Main three multilevel inverter topologies and hybrid models of these structures have been reviewed in the following part of the paper by demonstrating sample models and control strategies.

III. FLYING CAPACITOR MULTILEVEL INVERTER (FCMI)

FCMI involves in the usage of extra capacitor clamped to the power switches phase rail to provide the DC voltage level.This structure allows for the inverter to supply high capabilities especially during the power outages due to the redundancy in switching states provided

by the clamping Capacitor [3]. By assuming that the voltage rating for each of Capacitor applied in the circuit is equal with the switching devices, an m-Level of inverter will require a total of (m - 1) x (m - 2)/2 auxiliary capacitor per phase leg in addition to (m - 1) main DC bus capacitor [4]. It is different with DCMI which for m-Ievel of this type of inverter, it is only required (m - 1) Capacitors on the same voltage rating as the switching devices [3]. Thus, by taking m = 3 as an example for the number of thelevel in FCMI, it will give the number of auxiliary capacitor, $N_c = 2 \times 3 + 2 = 3$ Compared with DCMI that used N c = 2 in the circuit. Other than that, this type of multilevel inverter also provides the switching combination redundancy that I very useful for the voltage level balancing.

IV. DESIGN AND DEVELOPMENT OF FCMI SIMULATION MODEL

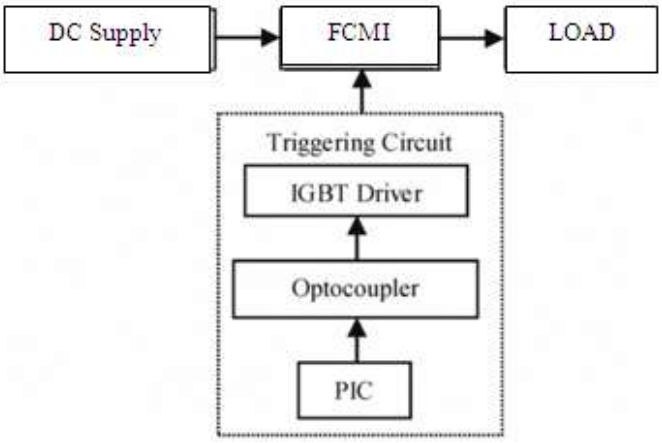

Fig.3.Block diagram of FCMI

The simulation model of three levels FCMI was developed using MATLAB/Simulink simulation software.Fig.3.shows the block diagram of single phase 3 level FCMI.

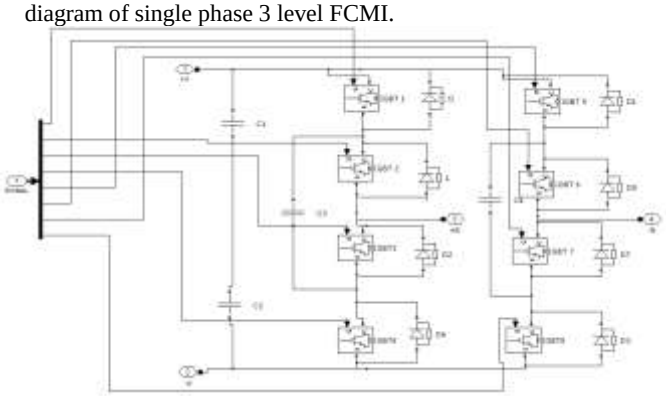

Fig.4Simulation model of the single phase three level FCMI

The simulation circuit of the FCMI is basically divided into three main parts. They are the triggering signal circuit, inverter circuit i.e. FCMI and also the load. The design of the single phase three level FCMI is shown as in Figure 4. This single phase three level FCMI has eight IGBTs, thus eight signals will be required for the operation. It has two DC link capacitors at the DC side, C 1 and C2. Capacitors C3 and C4 are the clamping capacitor that will provided the variation in DC voltage level. As the number of level is increased, the amount of DC link capacitor and clamping capacitor will also increased. One of the special feature of FCMI is it has several switching states combination for a certain value of output voltage level. Based on Zhang, Watkins and Shepherd (2002), by selecting suitable combination of switching states, all eight IGBTs can be switched on for the same duration, thus making the switching of power switches to be efficient [2]. Eight switching states have been chosen that will give the optimum switching time for all IGBTs and this are shown in Table 2. Each IGBT is switched on for half of the cycle, i.e. 1800 or 0.01 s and phase shifted 450 or 2.5ms among each other.

IGBT 1= $\overline{\text{IGBT 4}}$;	IGBT 2= $\overline{\text{IGBT 3}}$;	IGBT 5= $\overline{\text{IGBT 8}}$;	IGBT 6= $\overline{\text{IGBT 7}}$

TABLE.1. The switching of triggering circuit

By referring to Table 1, a relationship can be obtained among the IGBTs. It is found that one signal is the inverse of one another signal. This helps in reducing the number of switching signals to four, and the remaining four are the inverse. Thus only four signals are required to be generated by the PIC as shown in equation (A).

Equations:-

$$M_k = \frac{1}{(N-k)!} \times \prod_{n=0}^{N-k-1} (2N-n) \text{ for } 0 \le k < N \qquad (1)$$

where k defines the level number and equals 0 for the 0V level and N for the maximum voltage level in an N-cell inverter, thus

$$M_k = 1 \text{ for } k = N \qquad (2)$$

---------- (A)

There are only four independent switches. Setting (1) for when a switch is ON and (0) for when it is OFF.
more than one switching mode capable of the half DC voltage level (4 for +VDc/2 and 4 for -VDC/2)as in equation (2)

Equation for switching modes (Mk) for any voltage level

$$\frac{dV_{C1}}{dt} = \pm \frac{1}{C_1} i_0 \qquad (3)$$

and the load voltage

$V_O = V_{C1}$ or $V_{DC} - V_{C1}$

for discharging and charging , respectively.

$$\frac{di_o}{dt} = \frac{1}{L}(v_o - Ri_o)$$

(4)

In equation (3) and (4) the charging and discharging voltage and current with respect to the capacitors across DC link and to balance the clamped capacitor effecting load voltage are shown.

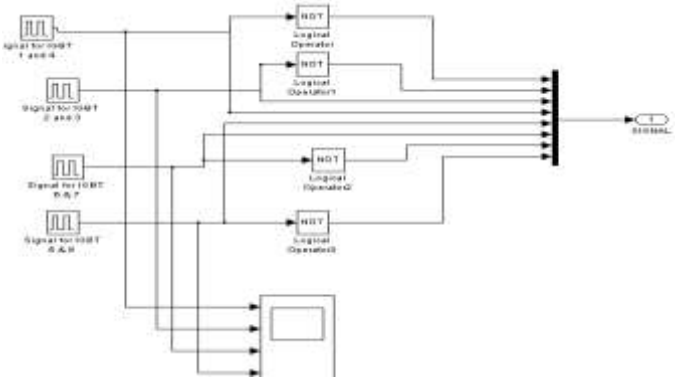

Fig. 5. Simulation model of triggering circuit.

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The simulation model of triggering circuit is shown in fig.5. The figure consists of signal triggering and NOT logical operator.

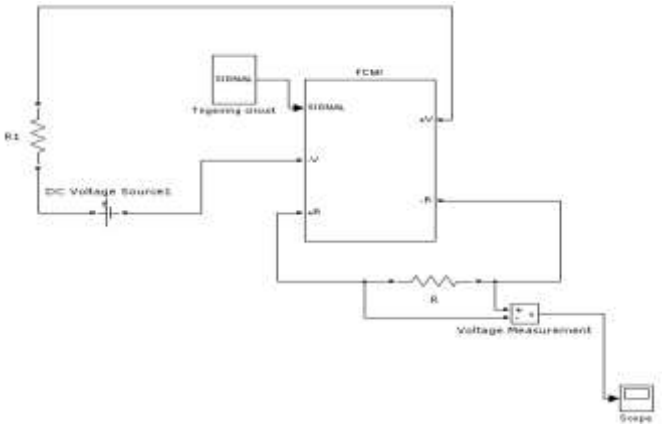

Fig.6.Complete model of Simulation Circuit of FCMI.

Considering the complete simulation model in fig.6 with the specification of Considering Vdc=12Volt, load Resistance =10 Ω, DC link Capacitor (C1, C2=0.01uFarad) with multiple switching triggering technique

A . *Inverter with Ultra capacitor.*

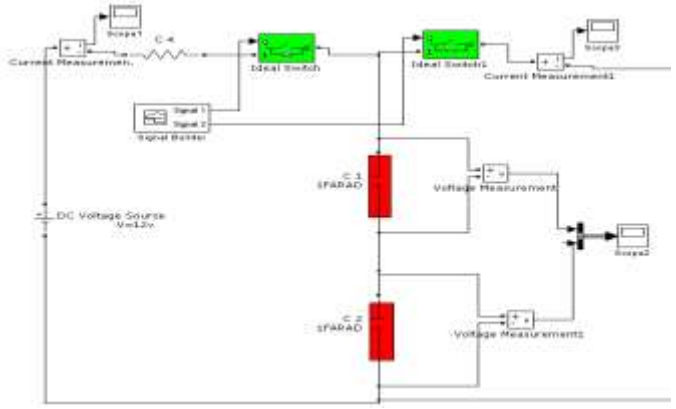

Fig.7. Circuit of FCMI with ultra capacitor

Considering the Fig.7 with the specification Vdc=12 Volt, load resistance = 10Ω, (C1, C2=1Farad).
The circuit consist of signal builder with respect to two ideal switches and two Super capacitorC1 & C2.As the signal builder provides the two signals where the first signal charges the Super capacitorC1 &C2 with respect to the battery voltage 12Volts with the help of ideal switch 1.
When the Super capacitorcharges to the full extent then the ideal switch 1 get off and with respect to the ideal switch 2 the Super capacitorC1 and C2 get discharge with respect to the resistive load of 24 Watt.

V. SIMULATION RESULT:-

Based on the timing diagram and by referring to Table 1, a relationship can be obtained among the IGBTs. It is found that one signal is the inverse of one another signal. This helps in reducing the number of switching signals to four, and the remaining four are the Inverse. As shown in fig.8 the triggering of IGBT 4, IGBT 3, IGBT 6, and IGBT 5 MATLAB software by applying the parameter of every 45(degree) or 2.5 ms as shown in fig.8.The output signals from PIC then passed optocoupler and IGBT drivers.As shown in fig.9. The Waveform of output voltage, VLL (V) with respect to the source input voltage of 100 V (dc).

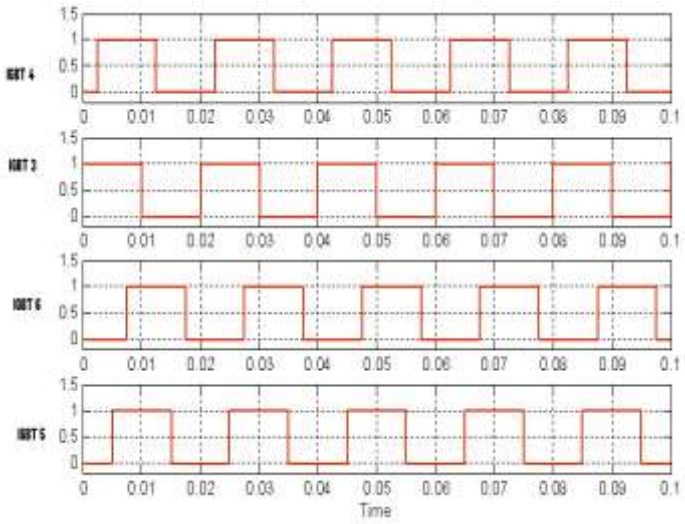

Fig.8.Timing diagram of triggering circuit for FCMI

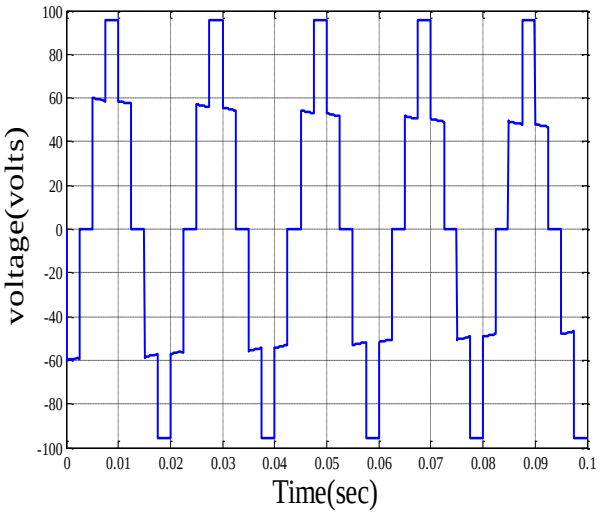

Fig.9.Waveform of output voltage,VLL(V) against time,t(s)

Fig.10.Super capacitor(C1, C2) charging and discharging with signal builder

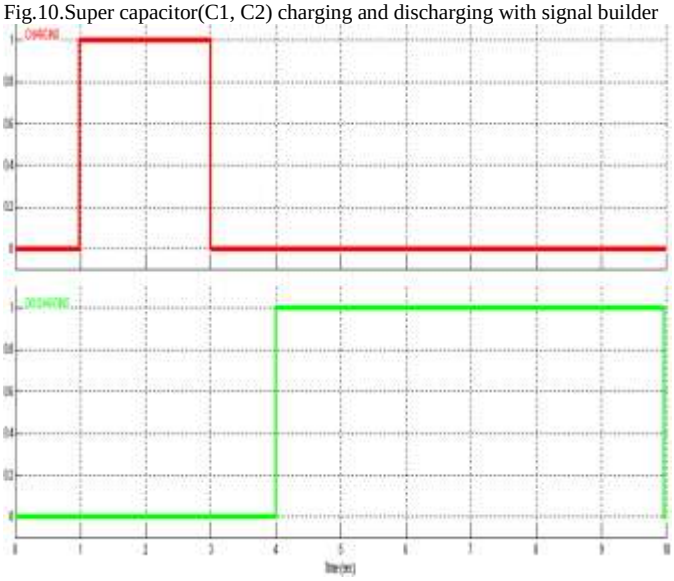

Fig.11 Super capacitordischarge through the resistive load.

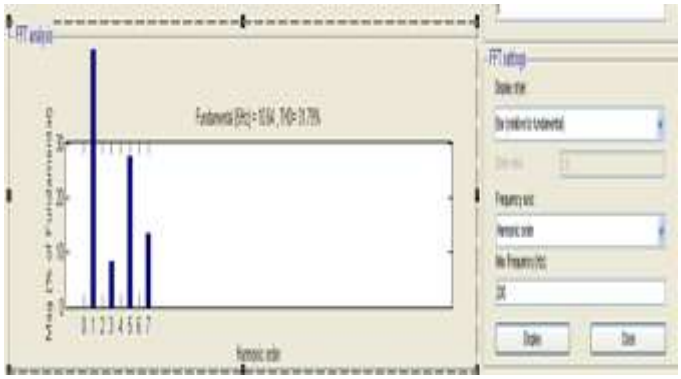

Fig.12. FFT Analysis of Simulation Circuit.

It is found from the FFT analysis that for output frequency of 5Hz,the total harmonic distortion(THD) is 31.79%.As the delay we have provided the delay in the ratio 30:70:60 :70:30 =200ms i.e.5Hz. In this After 30mS the pulse is going to released , and on for 70mS.

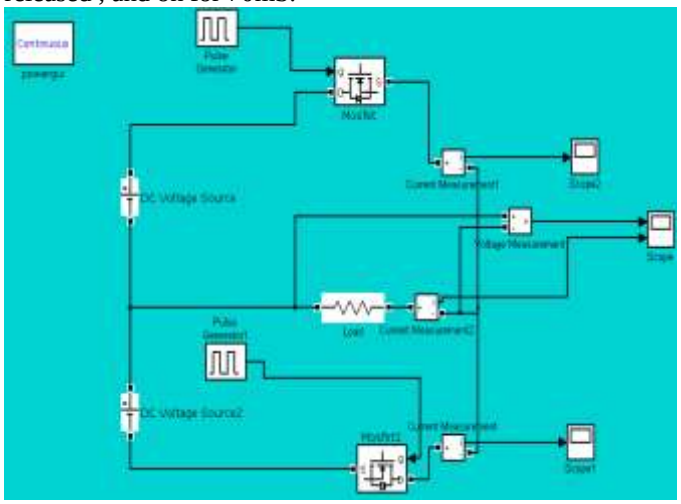

Fig.13. Simulation circuit of hardware with batteries.

In this the two battery is centre tapped as the circuit have consist two DC source i.e. battery (6 Volts, 4.5Ah), with the output frequency of 5Hz, load resistance of 2.2KΩ. The output load voltage across the positive half cycle and negative half cycle is (+ -6) Volt, and the output load current is 3 mA.

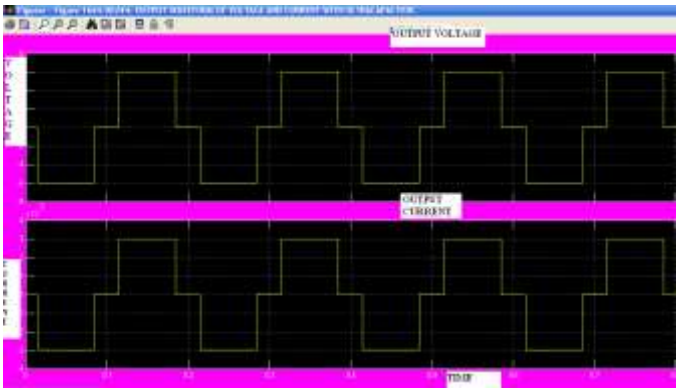

Fig.15. Output waveform of voltage and current with ultra capacitor**.**

In Fig15 the two Super capacitoris connected in centre tapped as the circuit have consist two Super capacitor(7.5 Volt,3.33 Farad), with the output frequency of 5Hz, load resistance of 2.2KΩ. The output load voltage across the positive half cycle and negative half cycle is (+ -6) Volt, and the output load current is 3 mA**.**

VI. HARDWARE CIRCUIT AND THE RESULTS.

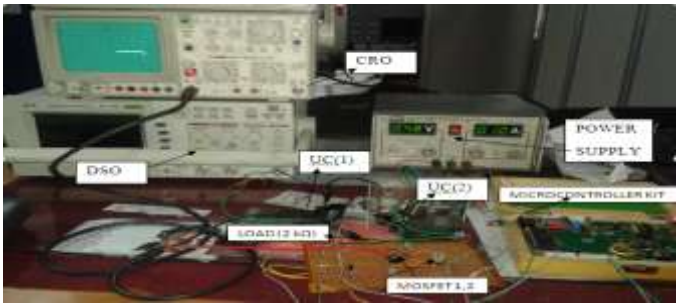

Fig.16. Hardware component with circuit Configuration.

A. *Hardware component and their ratings are given below*

System Component	**Specification**
Battery bank	6.7Vdc (6Vdc nominal)
Super capacitor bank	7.5 Vdc,3.33F
Power MOSFET IRF9540 (P MOSFET) IRF 744N (N channel MOSFET).	VDSS = -100V,RDS(on) = 0.117ID =23A,Vgs=10-23 V at 23C, VDSS = 450V,RDS(on) = 0.63ID =8.8A,Vgs=+-20 V at 23C
Microcontroller(8051)	+- 5 Vdc.
Load Resistance	2KΩ

Fig.17 system component and their specification.

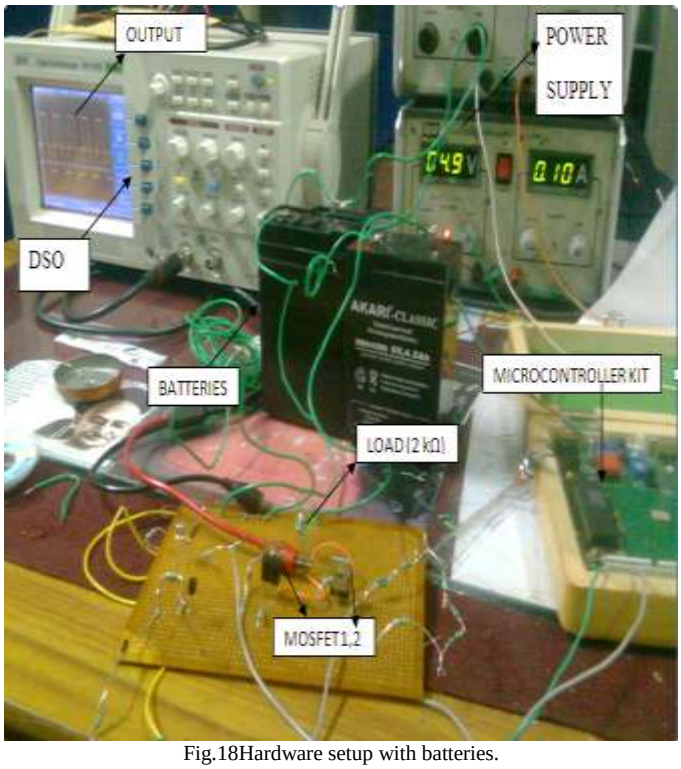

Fig.18Hardware setup with batteries.

In Fig.18. the two battery is centre tapped as the circuit have consist two DC source i.e. battery (6 Volts, 4.5Ah), with the output frequency of 5Hz, load resistance of 2.2KΩ.

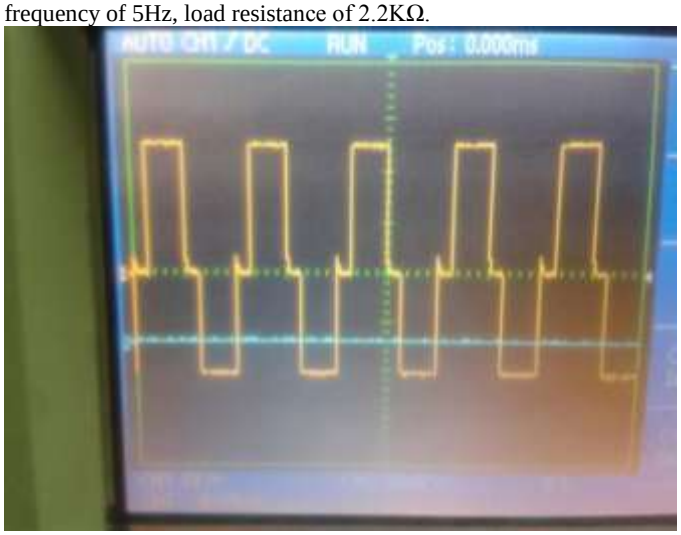

Fig.19 Hardware result with batteries.

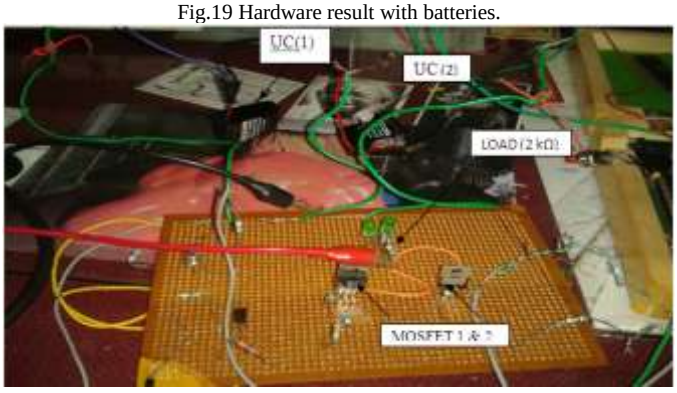

Fig. 20 Hardware setup with ultra Capacitor.

The output load voltage across the positive and negative half cycle is +2.5 and -2.2 Volt, and the output load current is 3 mA.

6.1 Reduction in load voltage with time:

Considering the load voltage across Super capacitorand to interpret the discharging operation with respect to time, we have found with hardware result

For 75% discharge of Super capacitor across the load resistance of 2kΩwith the average value of output voltage i.e. 2.2 volt, we have 2.2*0.75=1.65Volt. **it require approximately 3 minutes (Practically verified).**

B. *Calculation of performance with technical and Economical aspect:*

With respect to batteries of 6 Volt, 4.5Ah: 2*6*4.5=54 WattHr.

In terms of Joules:

54*3600=194.4KJoules.For approx 200KJoules with respect to the ultra capacitor, it is cost rupees 1500Rs**.**

VII. CONCLUSION.

From the results, we approach to the conclusion that if the battery is replaced by the charge Super capacitor then the output waveform with respect to the three level inverter gets much better inverter output and provide a more acceptable topology, especially for portable futuristic systems.

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