Investigations on ANPC Multilevel Inverter used for Even loss Balancing

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Abstract— This paper discusses even loss distribution among semiconductor devices by using Active Neutral Point Clamped (ANPC) multilevel inverter. The main drawback of the Neutral Point Clamped (NPC) inverter is the unequal loss distribution which limits the maximum output power. To overcome this drawback, switching state redundancy is required to evenly distribute the losses. The ANPC inverter which can overcome this drawback is discussed in this paper. This paper also discusses the comparative analysis of Three level NPC and ANPC Multilevel inverters for even loss distribution in semiconductor devices with the simulation results.

Keywords- *NPC,ANPC,Even loss Balancing.*

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I. INTRODUCTION

Multilevel inverters have made revolutionary changes in the utilization of power electronics in high voltage and high power applications [1]. The basic concept involves generating output AC waveforms from small voltage steps by using series connected capacitors or isolated DC sources [1]. The small voltage steps in the output voltage produce lower harmonic distortion, lower *dv/dt*, lower electromagnetic interference (EMI) and higher efficiency when compared with the conventional two level voltage source inverters [1].

The 3L-NPC (Figure.1) inverter is widely used in high power medium voltage applications [2] [3]. The major disadvantage of this topology is the unequal loss distribution among the switches. However it also generates unequal junction temperature distribution which confines the inverter maximum output power [4]. Moreover as the levels of the inverter increase the unequal switching of the semiconductor devices also increase and so the voltage unbalance between the DC link capacitors also increases.

The three level active neutral point clamped (3L-ANPC) inverter (Figureg.2) is an attractive topology which can overcome the unequal loss distribution problem of the 3L-NPC inverter and improve the power ability [5]. In 3L-ANPC inverter topology two auxiliary switches are added for the purpose of clamping instead of clamping diodes as in 3L-NPC. These auxiliary switches are introduced to ensure the equal voltage sharing between the main and auxiliary switches. Moreover in unlike NPC inverter, in ANPC inverter the DC link capacitor voltage will naturally balance under normal operation of inverter. This is because of increased switching redundancy due to adding the clamping switches instead of clamping diodes.

II. THREE LEVEL NEUTRAL POINT CLAMPED MULTILEVEL INVERTER

A single phase 3L-NPC is shown in Figure.1. where x represents the phase a, b or c. The switches (Sx1, Sx1'), (Sx2, Sx2') are the complimentary switching pairs. The output is taken with reference to the neutral point n. i.e. Voxn. Diodes Dx1 and Dx2 are the clamping diodes. Capacitors c1 and c2 are the DC link capacitors that will divide the input voltage Vdc equally. The switching sequence for producing three level output is shown in TABLE 1.

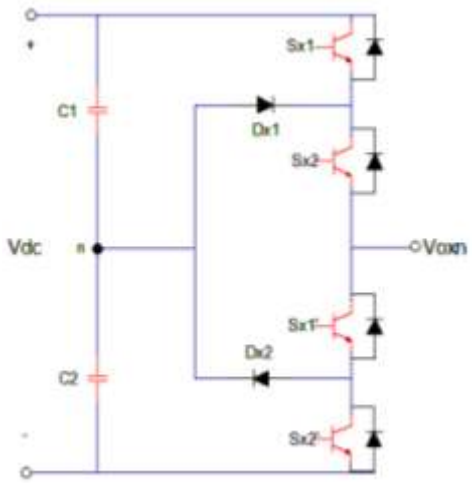

Figure 1 3L-NPC

For producing voltage level +Vdc/2 switches Sx1 and Sx2 are to be turned on and its complimentary switches will remain turned off at this time. So the upper DC link capacitor C1 will connect to the positive of the supply compared to the neutral point and across the load +Vdc/2 is obtained. For producing zero voltage level switches Sx2 and Sx1' are turned on. At this time the diodes Dx1 and Dx2 will carry the neutral point current. Ideally under the balance load condition the neutral point potential will be at zero. Hence zero output voltage level is achieved. For producing voltage level –Vdc/2 switches Sx1' and Sx2' are turned on. Now the lower capacitor will supply to the load but in the reverse direction and –Vdc/2 output voltage level is achieved.

TABLE 1 Switching States of 3L-NPC

Switches				Voltage Level
Sx1	**Sx2**	**Sx1'**	**Sx2'**	
1	1	0	0	**+Vdc/2**
0	1	1	0	**0**
0	0	1	1	**-Vdc/2**
1=ON, 0=OFF				

III. THREE LEVEL ACTIVE NEUTRAL POINT CLAMPED MULTILEVEL INVERTER

A single phase 3L-ANPC is shown in Figure 2. where x represents the phase a, b or c. It can be regarded as the combination of three two-level cells namely cell1, cell 2, and cell 3. Switches (Sx1, Sx1'), (Sx2, Sx2'), and (Sx3, Sx3') are complementary switch pairs of each cell.

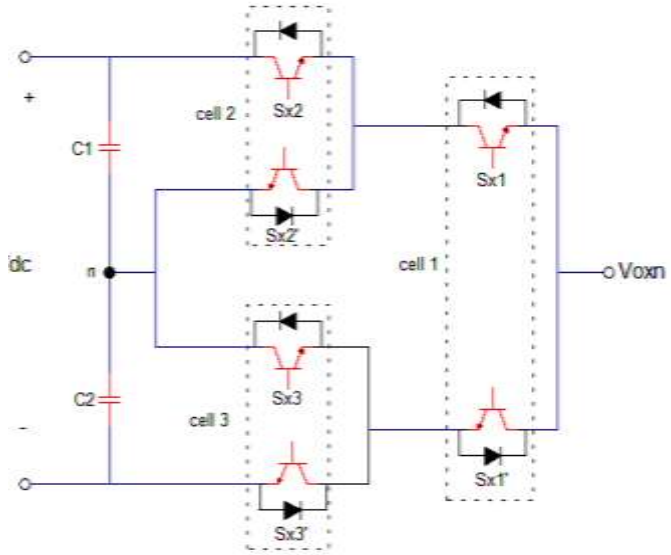

Figure 2 3L-ANPC

The output is taken with reference to the neutral point n. i.e. Voxn. The switching sequence for producing three level output voltage is shown in TABLE 2. For producing voltage level +Vdc/2 Sx1, Sx2 and Sx3 are turned on. Here Sx3 is on and ensures the equal voltage sharing between the off state switches i.e. Sx2' and Sx3'. For the zero voltage stage there are two redundant switching states with different current paths. The phase current flows through the upper path in both direction when Sx2', Sx1 and Sx3' are turned on. While through the lower path when Sx1', Sx2 and Sx3 are turned on. Neutral current only, will flow through both the paths in zero voltage state. The even distribution of switching losses in the 3L-ANPC inverter is achieved by selecting upper or lower current paths. For the voltage level –Vdc/2 switches Sx1', Sx3' and Sx2' are turned on. Here again the switch Sx2' ensures the equal voltage sharing between the Sx2 and Sx3.

TABLE 2 Switching States of 3L-ANPC

Switches						Voltage Level
Sx1	Sx2	Sx3	Sx1'	Sx2'	Sx3'	
1	1	1	0	0	0	**+Vdc/2**
1	1	0	0	0	1	**0**
0	1	1	1	0	0	**0**
0	0	0	1	1	1	**-Vdc/2**
1=ON, 0=OFF						

IV. COMPARATIVE ANALYSIS OF 3L-NPC AND 3L-ANPC MULTILEVEL INVERTER WITH SIMULATION RESULTS

The control strategy that is used in this paper for simulation is phase shifted carrier based pulse width modulation (PS-PWM) shown in Figure 3. The carrier signals for switches Sx1 and Sx2 are triangular waves that are phase shifted by 180º and the reference signal is 50Hz sinusoidal signal.

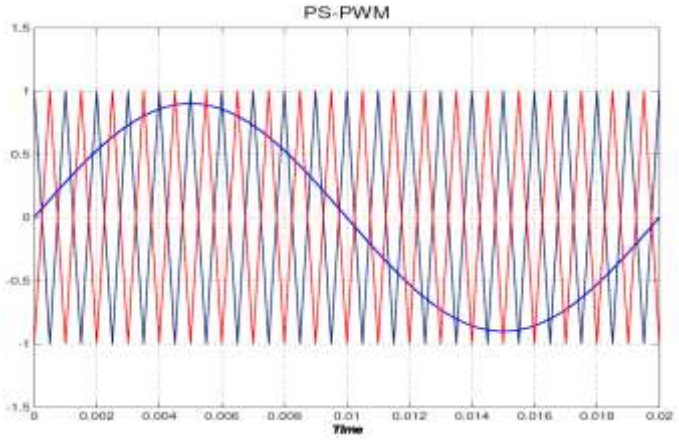

Figure 3 Phase Shifted PWM

The simulation results are shown in Figure 4 (a) & (b). Figure 4 (a) shows the results of voltage across the switches in 3L-NPC with RL load. From the waveforms it is clear that the voltage stresses are high in switches Sx2 and Sx1' compared to Sx1 and Sx2' i.e. middle switches in 3L-NPC. It will produce the uneven distribution of losses among the semiconductor devices. So, the switch rating for the middle two switches in NPC multilevel inverter should be higher than the upper and the lower switches to match the switching losses. The uneven distribution will also cause for unbalance in DC link capacitors for higher levels of the inverter.

Figure 4 (b) shows the results of voltage across the switches in 3L-ANPC with RL load. By comparison to 3L-NPC it is clear that the loss distribution among the semiconductor devices is even. So, the inverter maximum power can be achieved. It is also beneficial for higher levels of multilevel inverter in natural balancing of DC link capacitor because of the switching redundancy in active neutral point clamped multilevel inverter. However, this will cost extra switches instead of diodes. But the rating of switches can be reduced by even distribution of losses and the switches can be provided with the same ratings.

V. CONCLUSIONS

The active neutral point clamped multilevel inverter offer redundant switching states with the active clamping by providing switches instead of diodes as in NPC. These redundant switching states can be utilized to distribute the switching losses among the semiconductor devices and all the switches are operated at same carrier frequency. The balancing of losses allows to increase the output power or switching frequency of the inverter. The equal switching and balanced voltage sharing is also beneficial for DC link capacitor voltage balancing.

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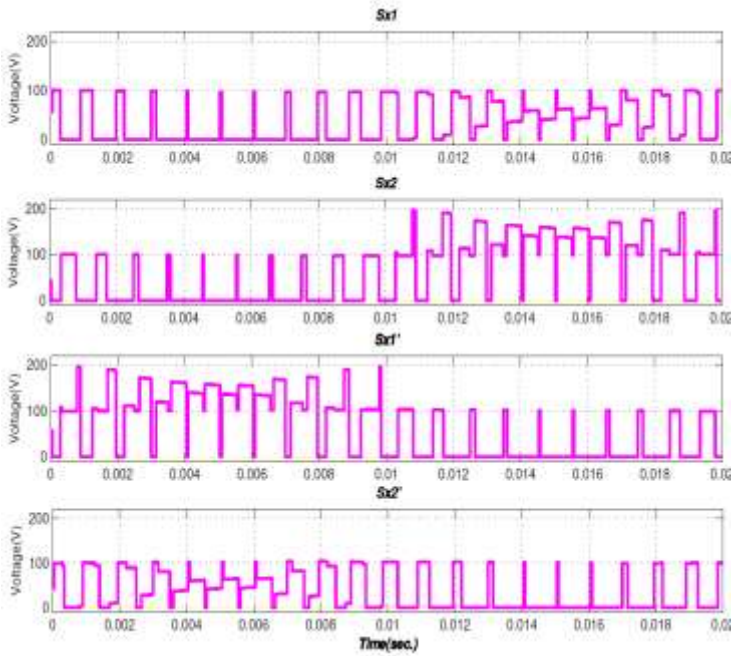

Figure 4(a) Voltage across Switch in 3L-NPC with PS-PWM

Figure 4(b) Voltage across Switch in 3L-ANPC with PS-PWM