International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169
Volume: 3 Issue: 2 110– 113

Co-Design of Efficient Low Power Successive Approximation Quaternary Analog to Digital Converter

Mayur Nannaware [1]
Department of Electronics and Communication Engineering
Abha Gaikwad-Patil College of Engineering
Nagpur, Maharashtra, India
e-mail:mayurnannaware215@gmail.com

Prof.Parag Jawarkar[2]
Department of Electronics and Communication Engineering
Abha Gaikwad-Patil College og Engineering
Nagpur, Maharashtra, India
e-mail:jawarkar@gmail.com

Abstract— An implementation of quaternary logic in varied application areas which is based with orientation of successive adder is been proposed in terms of flip-flops performed with higher speed, considerable power optimization and precise organized processing is obtained in CMOS based arrangements of flip-flop such that scaling of values preamble with single digit based quaternary addition with circuits using Analog to Digital Converters (ADCs). Energy efficiency in SAR based VLSI based processor is necessary and been performed in terms of quaternary flip-flop. There is an optimization of power with increase of threshold voltage values in terms of its redundancy of bits. Design of quaternary flip-flop based optimization and quantization of Micro-Core based SIMD processor to achieve minimum rescaled value of resolution in terms of power optimization. This estimation of quaternary flip-flop based optimized values and enhanced data-transfer resulting in higher speed with power reduced to 0.675µW CMOS simulation in corresponding to its CMOS based design implementation.
Keywords: *power optimization, CMOS, preamble, VLSI, SIMD, ADC, Micro-Core.*

*****

I. INTRODUCTION

As in terms of power dissipation in CMOS VLSI chips has been getting a serious problem in recent nanoscaling regime. Power density in VLSI chips is increased by k0.7, where k (> 1) is a device scaling factor, causing a doubling of the power dissipation every 6.5 years. It is assumed that the power dissipation in CMOS chips will increase steadily as a natural result of device scaling. From the viewpoint of the technology trend in special-purpose VLSI processors, its performance improvement is still strongly requested in multimedia-application fields. Especially, large-scaled parallel arithmetic operations must be performed in such VLSI processors. Hence, energy efficiency is one of the most important factors in the recent high-performance VLSI processors. In order to solve the above problem, energy-efficient multi-core SAR VLSI processors have been intensively developed in recent era. In such energy-efficient VLSI processors, it is important to enhance the performance of their processing elements themselves with maintaining less power dissipation.

On the other hand, it is known that one of the key circuit techniques for reducing power dissipation in a desired circuit is to use Adder parameters with multiple-valued current-mode circuitry. Since the use of the differential-pair ADC circuit makes input voltage swing small yet circuit driving capability high, the rescaled combination of multiple-valued current-mode circuitry and differential-pair circuitry enables to implement energy-efficient circuits with respect to DAC.

II. PROBLEM REVIEW

In terms of their processing elements (PE) based complexity to single digit based quaternary SAR based addition is been seen under power optimization with latch in build master for error quantization for comparing as well as storing [1] [2]. Though the reduction of errors is constrained to about 55 to 65% with reference to Micro-Core SIMD processor [2][3].

III. PROBLEM DIFINATION

As is considered to reduce the delay for the precision in processing of SIMD based processor it is required for Vertical (V-Channel) and Horizontal (H-Channel) [2] [5] [6] optimization with power optimization and increase in speed with respect to gates for various quaternary states. Providing low power with increased threshold voltage V_T as in terms $V_T >> P_{optimized}$ (reduced).

IV. PROBLEM ANALYSIS

There is a consideration of sates in terms of values having a symmetrical value in terms of its transition from absolute low< medium low< medium high< absolute high.

V. OBJECTIVES

Design of processing element using Quaternary differential logic [4]. Under this objective, different processing elements are designed for MP-SOC SIMD processor [3] [8] [9]. With reference to master latch and threshold detector the variation of power in terms of its optimized values is obtained from 1.0V to 3.0V which is pre-scaled from 0.39V to 0.49 V at 0.675µW for conversion under ADC level triggered.

VI. DESIGN ANALYSIS

As there is an implementation of basic gates for implementation of Quaternary D flip-flop provided for threshold detection [5] [10] referred to mater latch confined with its slave latch CMOS based output generator of V-Ch and H-Ch based CMOS [3] format as shown in reference to Figure 1 and Figure 2.

VII. METHODOLOGY

It has been seen as in CMOS based implementation from the master latch to slave latch [7] [12] [14] there is considerable increase in its threshold values such that $V_{T1}>V_{T2}>V_{T3}$ considerable speed is increased with respect to G output and G' inverted output thus, optimizing the power at a reduced rate [5] [16] as shown in reference to table below Table 1.

V_{IN}	$(Q_1\ Q_1')$	$(Q_2\ Q_2')$	$(G_2\ G_1)$
0	0,1	0,1	0,0
1	1,0	0,1	0,1
2	1,0	0,1	1,1
3	1,0	1,0	1,0

Table 1. Quaternary values with provided outputs (G1, G2)

When the MVs (Multi Valued) quaternary values are been considered in terms of its master latch and threshold detectors [8]with respect to latch inverter at 3.0 V with considerable clock pulse there is optimization [6] of time period as speed rate is been increased with respect to the Figure 3.

VIII. Tools Used

In terms of various simulations an integrated environment based with Tanner Tools is been used compatible with operating systems based on 32-bit Windows XP, Windows 7 with supported DOS environments.

IX. Features

1. Increased bus efficiency [17].
2. Less area with increased complexity.
3. Reduced chip area.
4. Higher radix -4 number system has redundancy [18].

X. Evaluation Result

Constrained with the respective dynamic values of MV contained in terms of PE [2][3] we consider that

P = V.R ……...Equation (i)

Then considering the relative values of power with accuracy of single bit addition for CMOS based values up to ± 0.06 to ± 0.04 as shown in table 2 depicted with Figure 4 below obtains the result of simulations 1 and 2. Thus, the dynamic resistance values obtained for the CMOS based quaternary logic is R_1 =3.2µΩ, R_2 =2.4µΩ and R_3 =1.4µΩ.

Threshold Voltage	Power
0.39 v	1.24 µW
0.45 v	1. 07 µW
0.49 v	0.675 µW

Table 2. Threshold Voltage vs. Power

XI. Conlusion and Future Scope

A high-performance PE using quaternary differential logic is proposed for a multi-core SIMD processor with successive addition is been obtained under ADC to DAC optimization initially shown in Figure 5. The rescaled combination of multiple-valued current-mode circuitry and differential-pair circuitry enables to implement energy-efficient circuit. In fact, the power dissipation and VLSI based MP-SOC counts of the proposed PE based MEs [5][6][9], respectively, under almost the same delay in comparison with those of the two-bit binary DAC CMOS implementation. By using multiple-valued current-mode logic, the complexity of wires would be reduced, which could result in higher-speed with reference to dynamic scaled data transfer.

References

[1] Hirokatsu Shirahama†, Akira Mochizuki†, Takahiro Hanyu†,Masami Nakajima and Kazutami Arimoto, "*Design of a Processing Element Based on Quaternary Differential Logic*",37th IEEE ISMVL 07.

[2] WU haixia, ZHONG Shunan, SUN Zhentao, QU Xiaonan, CHEN Yueyang, "*Design of Low-Power Quaternary Flip-Flop Based on Dynamic Source-coupled Logic*" IEEE 2011.

[3] V. V. Zhirnov, et al.,Emerging Research Logic Devices IEEE Circuits & Devices Magazine, pp.37-46.

[4] Akira Mochizuki, Takeshi Kitamura, Hirokatsu Shirahama and Takahiro Hanyu, "*Design of a Microprocessor Data path Using Four-Valued Differential-Pair Circuits*",IEEE ISMVL 06. A. Mochizuki, H. Shirahama, and T. Hanyu, "*Design of Low-Power Quaternary Flip-Flop Based on Dynamic Differential Logic*", IEICE Trans. Electron., vol.E89-C, no.11, pp.1591-1597, Nov. 2006.

[5] A. Jerraya, et al., Multiprocessor Systems-on-Chips, Computer, vol.38, no.7, pp.3640, July 2005.

[6] A. Mochizuki and T. Hanyu, "*A 1.88ns 54x54-bit Multiplier in 0.18µm CMOS Based on Multiple-Valued Differential-Pair Circuitry*," 2005 Symposium on VLSI Circuits, Digest of Technical Papers, 17-3,pp.264-267, June 2005.

[7] A. Mochizuki, T. Hanyu, and M. Kameyama, "*Design of a Low-Power Multiple Valued Integrated Circuit Based on Dynamic Source-Coupled Logic*", Journal of Multiple-Valued Logic and Soft Computing, vol.11,no.5-6, pp.481-498, 2005.

[8] Neha Umredkar , Dr. Prof. M. A. Gaikwad, Prof. D. R. Dandekar, "*Design of Low Power Quaternary Adders in Voltage Mode Multi-Valued Logic*", IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 3, Issue 1 (Sep. – Oct. 2013), PP 15-21

[9] *Algn Aditya, G.Rakesh Chowdary , J. Meenakshi, M.S.Vamsi Krishna* ―Implementation of Low power Successive Approximation ADC for MAV'S‖ IEEE International Conference on Signal Processing, Image Processing and Pattern Recognition 2013.

[10] *Md.Kareemoddin, A.Ashok Kumar, Dr. Syed Musthak Ahmed*, - "Design of low power SAR ADC in Biomedical Applications" International Journal of Advanced Research in Computer Engineering & Technology (IJARCET) Volume 2, Issue 7, July 2013

[11] *Brian P. Ginsburg and Anantha P. Chandrakasan*, "500-MS/s 5-bit ADC in 65nm CMOS With Split Capacitor Array DAC," IEEE J. Solid-State Circuits, vol. 42, no. 4, pp.739-747 , Apr. 2007.

[12] *Siamak Mortezapour, Edward K. F. Lee* ―A 1V 8-Bit Successive Approximation Register in standard CMOS process.IEEE VOL. 35, NO. 4, APRIL 2009.

[13] *Young-Kyun Cho, Young-Deuk Jeon, Jaewon Nam,Jong-Kee Kwon* ―A 9-bit 80 MS/sSuccessive Approximation Register Analo to Digital converter with a capacreduction Technique IEEETRANSACTIONS ON CIRCUITS AND57, NO. 7, JULY

2010. SYSTEMS—II: EXPRESS BRIEFS, VO57, NO. 7, JULY 2010.

[14] *Pieter J. A. Harpe, Cui Zhou, Yu Bi, Nick Groot* —A 26 µW 8 bit 10 MS/s Asynchronous SAR ADC for Low Energy Radios" IEEE JOURNAL OF SOLID STATE CIRCUITS, VOL. 46, NO. 7, JULY 2011.

[15] *Guan-Ying Huang, Soon-Jyh Chang, Chun- Cheng Liu, Ying-Zu Lin*-"A 1-µW 10-bit for Biomedical Applications" IEEE JOURNAL OF SOLID-STATE CIRCUITS,VOL.47, NO.11, NOVEMBER 2012.

[16] *Weibo Hu, Yen-Ting Liu, Tam Nguyen, DonaldY. C. Lie, Brian P. Ginsburg* –"An 8Bit Single-Ended Ultra-Low-Power SAR ADC With a Novel DAC Switching Method and a Counter-Based Digital Control Circuitry", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 60, NO. 7, JULY 2013.

[17] *Hur A. Hassan, Izhal Abdul Halin, Ishak Bin Aris , Mohd Khair Bin Hassan*-"Design of 8bit SAR-ADC CMOS",IEEE 2009.

[18] *Xiong Zhou, Qiang Li* –"A 160mV 670nW 8bit SAR ADC in 0.13µm CMOS" IEEE 2012.

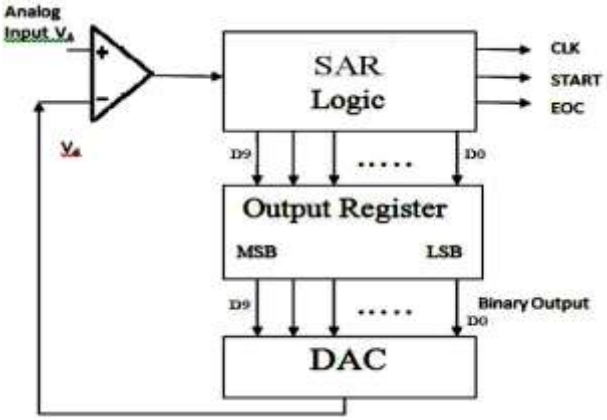

Figure 1. Block diagram of a SAR ADC

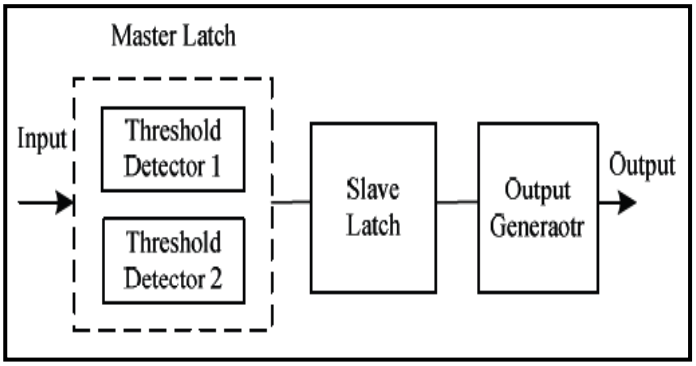

Figure 2. Quaternary D-flip flop

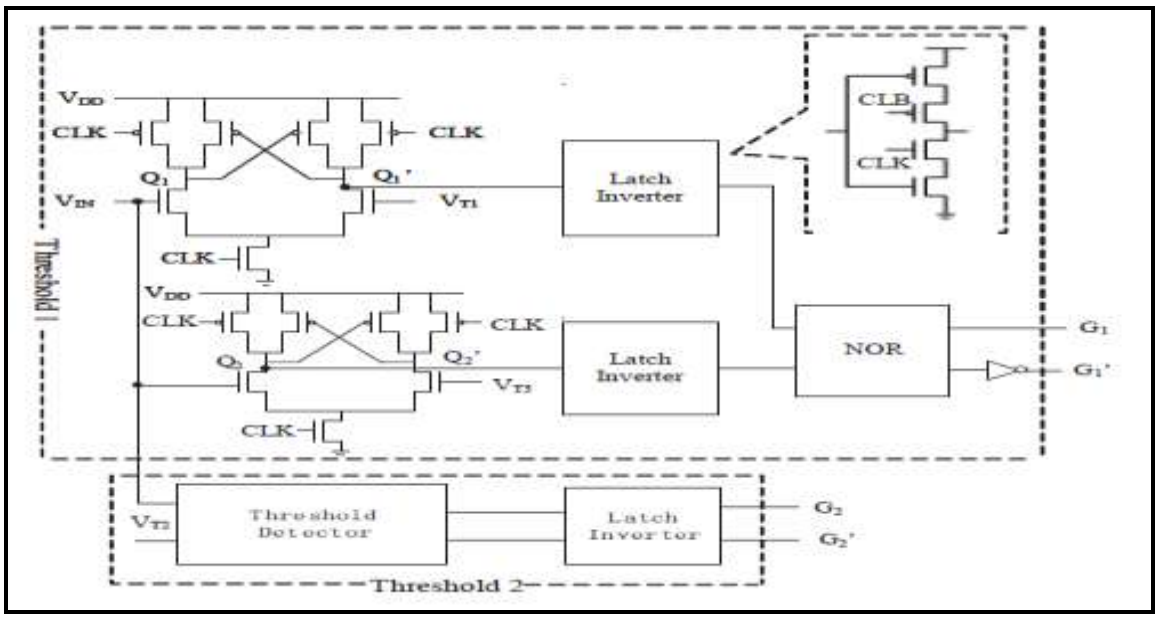

Figure 3. Block diagram of SAR based Master Latch

ISSN: 2321-8169
110– 113

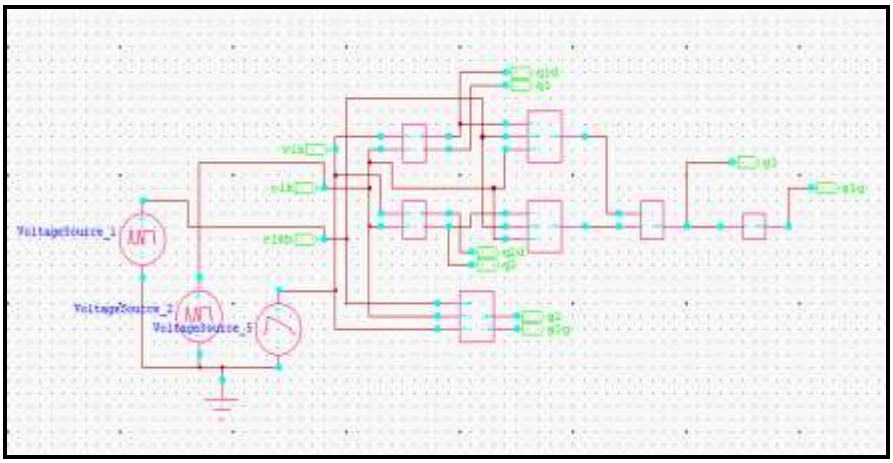

Figure 4. Schematic of SAR ADC- DAC based Master Latch

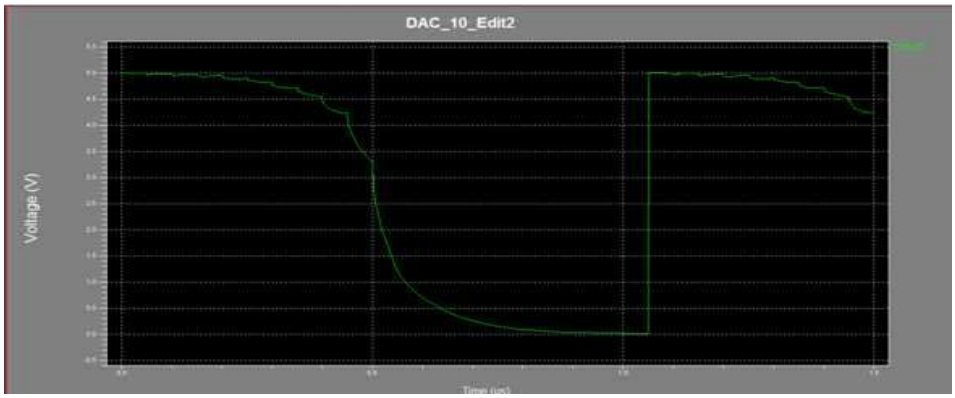

Figure 5. Obtained Initial Output of DAC