Survey Paper on Recursive Least Square Adaptive Filters Using Block DCD Approach

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Abstract—Due to the explosive growth of multimedia application and tremendous demands in Very Large Scale Integrated (VLSI), there is a need of high speed and low power digital filters for digital signal processing applications.Finite Impulse Response (FIR) filters are one of the most common components used in many real timeDigital Signal Processing (DSP) systems, wherein its response is obtained by convolving the input data samples with the desired unit sample response of the filter.

The proposed research paper deals with the survey on RLS adaptive filter using block DCD approach. This papermay help the system designer in designing the real time system on a reconfigurable platform like FPGA with significant reduction in area andpower consumption for high speed applications.

Keywords: - *RLS adaptive filter, Block DCD Approach, VHDL, Xilink ISE, ModelSim, FPGA kit.*

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I. INTRODUCTION

An adaptive filter is a computational device that attempt to model the relational device between two signals in real time environment in an iterative manner. Adaptive filter are often realize either as a set of program instruction running on an arithmetical processing device such as microprocessor or DSP (digital signal processor) chip or as set of logic operation implemented in FPGA or in semicustom or custom VLSI circuit however ignoring any error introduced by numerical precision effect. In this paper, the fundamental operation of an adaptive filter can be characterized independently of specific physical realization that it take. For this reason the proposed method focuses on survey of RLS adaptive filter with their specific realization in software and hardware.

The demand and popularity of portable electronics is driving designers make great efforts to achieve for small silicon area, higher speeds, and power dissipation and reliability. The proposed work deals with the design and performance analysis of Adaptive Filter in VLSI. Figure1 shows the basic concept of the adaptive filter which uses Least Mean Square Algorithm for minimizing the error.

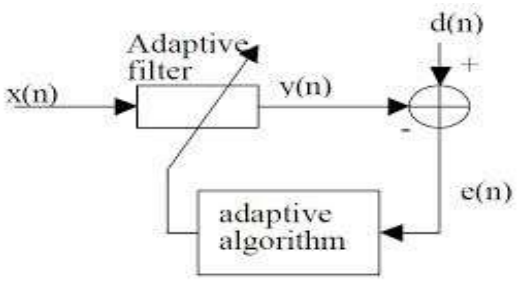

Figure 1: Generalized structure of adaptive filters

The disadvantage of LMS algorithm is that, it cannot meet the requirement of fast rate of convergence and minimum MSE. The best choice is to use the block recursive least squares (RLS) algorithm to overcome the above difficulty. Block Recursive Least Square-DCD (Dichotomous Coordinate Decent) algorithms are known to exhibit better performances and are one of the variants algorithm in which the updating of weights is done at block level and the error values are calculated at every clock cycle. The weights are updated once per every block data instead of updating on every clock cycle of input data. Also the error values are calculated at every clock cycle. Figure 2 Shows the generalized RLS adaptive filters in which u (n) are the input and y (n) is the output of the filter. d (n) desired response of Adaptive filter and the error is denoted by e(n).This error is the result of the difference between the actual filter output and desired output i.e. e(n) = y(n)-d(n) and it is called as estimation error. The aim of this filtration is to remove the estimation error. λ is step-size which is used for adaptation of the weight vector, the tap-weight vector *w(n)* and the tap-input vector *u(n)* is defined as follows

$$W(n) = [w_0(n), w1(n), \ldots, wn_{-1}(n)]^T$$

$$u(n) = [u(n), u(n-1), \ldots, u(n-N+1)]^T$$

$$k(n) = \frac{\lambda^{-1}P(n-1)u(n)}{1 + \lambda^{-1}u^H(n)P(n-1)u(n)}$$

$$\xi(n) = d(n) - \hat{w}(n-1)u(n)$$

$$\hat{w}(n) = \hat{w}(n-1) + k(n)\xi^*(n)$$

$$P(n) = \lambda^{-1}P(n-1) - \lambda^{-1}k(n)u^H(n)P(n-1).$$

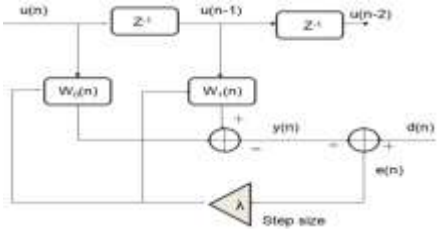

Figure 2:- RLS Adaptive filter

The Z-inverse is a delay element used for controlling the input of filter.whenever the first input is given to the filter u(n) at that time other input have stand-by condition then second input is given to filter that is u(n-1) and so on. The filter processes only one input signal at a time.The proposed dissertation paper deals with the survey on design of simple architecture for the implementation of a variant of Block DCD RLS-algorithm where the weight updating and error calculation are both calculated in block wise fashion.

II. Related Work

Adaptive filter forms the important basis for many real time digital signal processing applications. Many researchers have worked on adaptive filters for various diverse applications. The detail literature survey for the proposed dissertation is as follows:

In the paper by JafarSaniie et al., the author proposed the Hardware and Software Design for QR Decomposition Recursive Least Square Algorithm. An embedded hardware and software system was design and implemented for QR Decomposition Recursive Least Square (QRD-RLS) algorithm using given'srotation method for optimizing the area and power [1].

Dr. C. Vijay Kumar et al. presented the most important implementation of low power systolic base adaptive filter by deigning the RLS Adaptive Filter architecture using FPGA technology with clock getting. Systolic array architecture were used to reduce the circuit scale into half without impairing the processing speed and clock gating which results in the considerable reduction in power[2].

Md. Zulfiquar Ali et al., suggested the New Improved Recursive Least-Square Adaptive-Filtering Algorithms. In this papertwo new improved recursive least-squares adaptive-filtering algorithms, one with a variable forgetting factor and the other with a variable convergence factor are proposed. Optimal forgetting and convergence factors are obtained by minimizing the mean square of the noise-free a posterior error signal [3].

Cristian Stanciul et al. demonstratedthe Numerical Properties of the DCD-RLS Algorithm for Stereo Acoustic Echo Cancellation;Modern teleconferencing systems have been developed in recent years to use multiple acoustic channels (stereo communication). This feature improves the quality of Communication (e.g., in terms of spatial localization), but the classic problem of the acoustic echo cancellation becomes more complicated. In this context, the dichotomous coordinate descent (DCD) - recursive least-squares (RLS) algorithm can be an attractive choice for hardware implementation [5].

Another important workcarried out by Yuriy Zakharovt et al., in which Fast RLS algorithm using dichotomous coordinate descent iterations in this the Recursive Least Squares (RLS) adaptive filtering problem is expressed in terms of auxiliary normal equations with respect to increments of the filter weights. By applying this approach to the exponentially weighted case, a new structure of the RLS algorithm is derived. For solving the auxiliary equations, dichotomous coordinate descent (DCD) iterations with no explicit division and multiplication are used [8].

From the review of various papers, it is observed that the DCD algorithm is used for minimizing the iteration with greater speed and it can be very useful for Hardware implementation also. Existing methods is based on matrix inversion problem. However, the proposed method can be used to overcome the problem of matrix inversion by using Block DCD-RLS algorithm.

III. Conclusion

Adaptive filtering techniques can be used in many applications in different fields, such as wireless communication and channel equalization, noise cancelling, channel estimation.The serial implementation of the real-valued Block DCD algorithm will be the smallest hardware implementation and it is notable for smaller than any other methods requiring multiplication operations. However, the update rate will be limited as the residual vector will be required toupdate sequentially.

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