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FPGA Implementation of Efficient Edge Detection Using Canny Algorithm

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Abstract-- Edge detection is one of the most important stage in image processing. Performance of Canny edge detection algorithm is very good so Canny edge detection algorithm is widely used .This algorithm is very important algorithm . This paper presents FPGA implementation of efficient edge detection using Canny algorithm. This algorithm is very useful in Robotics field , image processing field and feature extraction. Its result is reduced memory requirement, decreased latency and delay produced in the algorithm. It is increased throughput with no loss in edge detection performance as compare to the original Canny algorithm. FPGA is basically   hardware architecture . FPGA is used in this paper and the architecture is synthesized on the Xilinx vertex-5 FPGA. The new algorithm uses a low complexity 8 –bin non-uniform gradient magnitude histogram to compute block based hysteresis threshold that one used by the Canny edge detection. Simulation is perform on the Modelsim and the results are presented to illustrate the performance of the proposed distributed Canny edge detector. In previous   paper the FPGA simulation results show that we can process a 512*512 image in 0.287ms at a clock rate of 100MHz., we will try to reduce this time delay in this paper.

Index Terms- *Canny edge detector distributed processing non-uniform quantization FPGA.*

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I. INTRODUCTION

The performance of the Canny edge detection algorithm is very good .Edge detection is provided the step for many image processing algorithm for example image segmentation, image enhancement and image video coding. Canny edge detection algorithms is implemented using software with advance in very large scale integration (VLSI) technology. Real time application used hardware implementationThis algorithm uses in image processing ,Robotics etc.

Preprocessing and post processing steps are used in Canny edge detection algorithm. It is more computationally complex as compare to the other algorithm such as Roberts Prewitt, Sobel algorithm. . The Canny edge detector is predominantly used in many real-world applications due to its ability to extract significant edges with good detection and good localization performance. This algorithm is very useful algorithm.
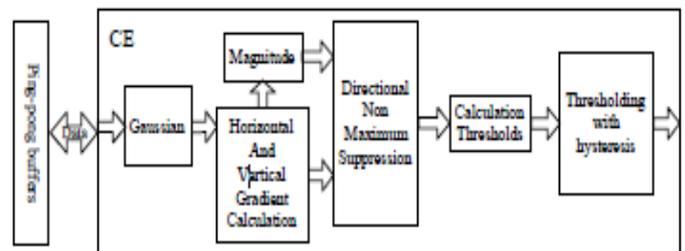
The Canny edge detection algorithm performs hysteresis thresholding which requisites computing high and low thresholds based on the entire image statistics .This places heavy requirements on memory and results in large latency hindering real-time implementation of the Canny edge detection algorithm.
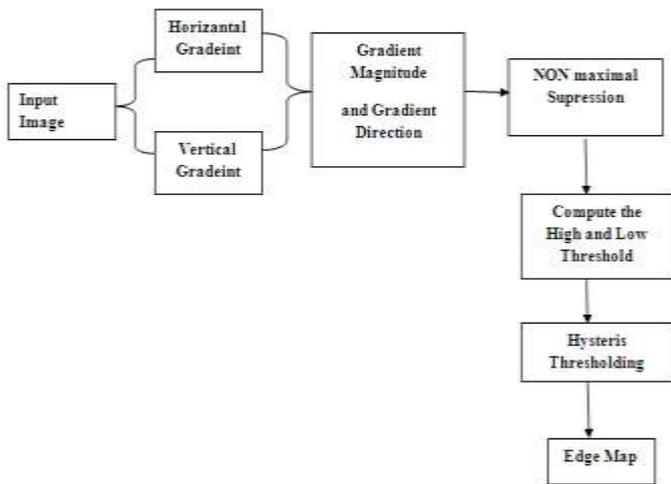
II. CANNY EDGE DETECTION ALGORITHM

Canny developed an approach to derive an optimal edge detector based on three criteria related to the detection performance. The model was based on a step edge corrupted by additive while Gaussian noise. The algorithm is mapped to onto a Xilinx Vertex-5 FPGA platform and tested using Model Sim, it is capable of supporting fast real-time edge detection for image and video with various special and temporal resolutions including full-HD content.   The original Canny algorithm consist of the following steps;

1.Smoothing the input image by Gaussian mask .The output smoothed image is denoted by l(x,y)

2.Calculating the horizontal gradient $Gx(x,y)$ and vertical gradient $Gy(x,y)$ at each pixel location by converting the image l(x,y) with partial derivatives of a2D Gaussian function.

3.Computing the gradient magnitude and direction at each pixel location.

4.Applying non-maximum suppression (NMS) to thin edges.

5.Computing the hysteresis high and low threshold based on the histogram of the magnitude of the gradients of the entire image.

Block diagram of the CE[compute engine]for the proposed distributed Canny edge algorithm

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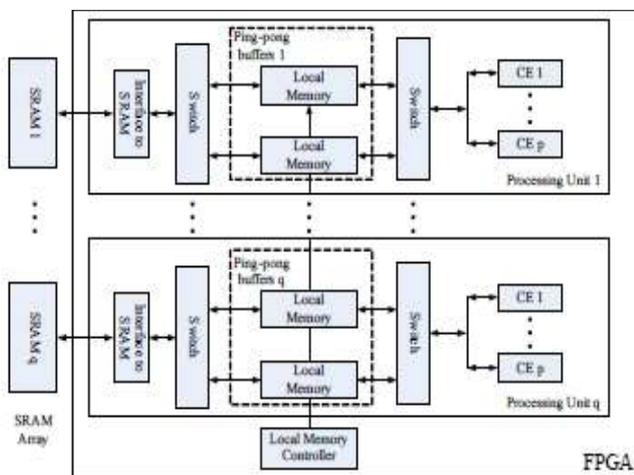Block diagram of the Canny edge detection algorithm

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Fig. The architecture of the proposed distributed Canny edge algorithm

III. LITRATURE SURVEY

Qian Xu, Chaitali Chakrabarti and Lina J. Karam, "A Distributed Canny edge detector and its implementation on FPGA". This paper describe the Canny edge detector and its implementation on FPGA.Edge detection is one of the key stages in image processing and object recognition. The Canny edge detector is one of the most widely-used edge detection algorithm due to its good performance. We present a distributed Canny edge detection algorithm that results in significantly reduced memory requirements, decreased latency . this results in a significant speed up without ssecrificing the edge detection performance. The computational cost of the proposed algorithm is very low compared to the original Canny edge detection algorithm.[1].

F. M. Alzahrani and T. Chen "A real-time edge detector algorithm and VLSI architecture, this paper present an absolute different mask (ADM) edge detection algorithm and its pipelined VLSI architecture for real time application .But the edge detector in offers a trade-off between precision cost and speed, and its capability to detect edges is not as good as the Canny algorithm. There is another set of work on Deriche filters that have been derived using Canny criteria. [2]

D .V . Rao and M.Venkatesan , "An efficient reconfigurable architecture and implementation of edge detection algorithm using Handle-C," the approach of this paper is to operates on two rows of pixel at a time ,this reduces the memory requirement at the expense of a decrease in the throughput .Further more it is known that the original Canny edge detection algorithm needs two adaptive image dependent high and low thresholds to remove false edges. However, the algorithm in just fixes high and low thresholds in order to overcome the dependency between the blocks which results in a decreased edge detection performance.[4]

S . Varadarajan , C. Chakrabarti, L. J. Karam, and J. M. Bauza, "A distributed psycho-visually motivated Canny edge detector ;" In this paper we proposed a new threshold selection algorithm based on the distributed of pixel gradients in a block of pixel to overcome the dependency between the blocks ,however in hysteresis thresholds calculation is based on a very finely and uniformly quantized 64 bit gradient magnitude histogram, Which is use in real time implementation.[5]

IV. PROPOSED TECHNIQUE

Distributed Canny edge detection algorithm is used in proposed paper .The Canny edge detection algorithm operates on the whole image and has a latency that is proportional to the size of the image . While performing the original Canny algorithm at the block level would speed up the operation ,it would result in lost of significant edges in high detailed regions and sedges in texture regions. Natural images consist of a mix of smooth region ,texture region and high detailed regions and such a mix of regions may not be available locally in every block of the entire image.. We proposed a distributed Canny edge detection algorithm, which removes the inherent dependency between the various blocks can be processed in parallel.

V. CONCLUSION

This paper present FPGA implementation of efficient edge detection using Canny algorithm .Performance of the Canny edge detection algorithm is very good so that's why it is widely used edge detection algorithm. We will decreased latency, reduced memory requirement and we will reduced delay also. We will use Xilinx vertex 5 software and test using Modelsim. This algorithm is very fast algorithm Canny edge detection algorithm shows very clear images and videos. .

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