A Review on System Level Behavioral Modeling and Post Simulation of Built-in-Self-Test of Sigma-Delta Modulator Analog-to-Digital Converter

Anil Kumar Sahu  
Assistant Professor, SSGI(FET), Bhilai  
anilsahu82@gmail.com

Dr. Vivek Kumar Chandra  
Associate Professor and Head (Electrical and Electronics Engineering)  
C.S.I.T. Durg (C.G)  
Vivekchandra1@rediffmail.com

Dr. G. R. Sinha  
Professor (Electronics and Telecommunication Engg.)  
& Associate Director, SSGI(FET), SSTC, Bhilai  
ganeshsinha2003@gmail.com

Abstract - This paper reported extensive study and research proposal of Post simulation and behavioral modeling of Second Order sigma-delta modulator BIST technique in which include non-ideality factor such as offset error and clock jitters. For the test of the digital parts, BIST techniques have been developed and are broadly implemented in current chips. BIST technique not only avoids depending on the off-chip automatic test equipment (ATE) and reduces the test cost but increases the controllability and observability of the circuit under test also that improves the fault coverage. Proposed work focus on implementation challenges of the BIST approach for the oversampling ADC circuit and demonstrate how to achieve high-precision on-chip analog stimuli by smaller hardware cost.

Keywords: BIST of Sigma-Delta Modulator ADC; Flow Diagram.

I. INTRODUCTION

In recent years, high-resolution analog-to-digital conversion based on sigma-delta (Σ-Δ) modulation has become common in many measurement applications including seismic, biomedical and harsh environment sensing. High demand of analog-to-digital converters (ADCs) in the market is due to the advantages of digital signal processing such as noise immunity and design automation, which are used in precision audio, high-definition video and micro-power medical devices, silicon condenser microphones. Oversampled sigma-delta modulation has gained much popularity in analog to digital conversion application for their good performance in low frequency, low consumption, low supply voltage and low silicon area occupation. However, it is necessary to have ADCs operating with very low power dissipation. Testing ADCs is mostly limited to conventional static and dynamic testing. Signal generator needs to generate a stimulus with resolution at least four times higher than that of the ADC under test in static test whereas in the case of dynamic testing, the test stimulus with known characteristics is applied to the ADC.

However, testing such high-precision ADCs requires high performance and expensive test-platforms, which further increases the test cost and final product as compared to all the kinds of ADCs. One promising solution to this problem is built-in-self-test (BIST) which utilizes on-chip resources to perform on-chip stimulus generation and response acquisition under the BIST approach. With the advent of complementary-metal-oxide-semiconductor (CMOS) technology, BIST using digital signal; processing has become a viable solution for analog mixed-signal.

II. A BRIEF REVIEW OF THE WORK ALREADY DONE IN THE FIELD

A number of research papers of various journals and conferences were studied and survey of existing literatures in the proposed area is reported below:

Now in this new era Implementation Higher order sigma-delta modulator design is possible in 65-nm CMOS for wireless code division multiplexing (WCDMA) applications[1]. For hardware reduction in digital delta-sigma modulators (DDSMs) The error masking strategy to be adopted with exploits knowledge of the shape of the noise floor since the positions of individual tones are typically unknown. area and power could be saved approximately by 40% with minimal degradation of the spectral performance of the modulator[2]. Performance of modulator is affected by non-idealities such as jitter shaping and quantization noise shaping designed by phase-based delta-sigma ADC which includes delay-locked-loop (DLL) [4]. The front-end integrator implementation also exhibits 25% less kT/C noise than conventional architectures. Mismatch shaping technique can also be combined with other schemes to create higher-order shaping and achieved greater accuracies[12].

Due to aggressive noise shaping and multi bit truncation, they can achieve high resolution even for low oversampling ratios [16]. Low-power continuous-time sigma-delta modulator circuit is widely adopted audio application [8]. its performance can be determined using only digital test stimulus; applied architecture does not need analog test stimuli, which is prone to distortion/noise while setting up the high-resolution modulator for testing. Simulation results show that this technique has been capable of accurately determining the performance of a second-order sigma–delta modulator ADC[10]. Efficient testing technique based on built-off self-test for differential analog and mixed-
signal circuits selected for individual device-under-test (DUT) specifications by resolving the imbalance problem using simple variable capacitors in loopback mode. The variable capacitor generates predefined imbalances to give different weights on the spectral loopback responses[11]. ADC’s dynamic performance from its tested integral non-linearity (INL) data, without requiring additional data acquisition or additional accurate sinusoidal sources. Memory and computation requirement is very small comparing to that in traditional spectral testing. When combined with a BIST approach for INL testing, this method offered a very low cost BIST solution to ADC dynamic performance testing [13].

(ORA) circuit for analog-to-digital converters (ADCs) built-in self-test (BIST) in which ADC static parameters, i.e., offset error, gain error, and nonlinearity errors, are directly obtained from the sine-wave histogram test. The appropriate approximations of the testing parameters reduce difficulties in designing the complete output response analyzer (ORA) circuit [14]. System-level integration including hardware and software of testing a fully integrated BIST wireless test platform and was first worked to exhibit the possibility of testing analog mixed signal (AMS) circuits[18]. Low-interference testing environment is the challenge for providing less noise to analog input of sigma-delta ADC. Upcoming novel built-in self-calibration technique for single-loop continuous time sigma-delta modulators which is using out-of-band test signal injection and digital cancellation, this technique provides an area efficient, highly digital calibration structure to counteract gain variations in the loop filter[15].

Built-In-Self-Test (BIST) techniques that consist of generating analogue test signals from digital test patterns (obtained via ΣΔ modulation) and converting the responses of the analogue modules into digital signatures that are compared with the expected ones. Limitation of this method is that the additional requirement of software environment to realize post low-cost output response analyzer (ORA) for the BIST Σ-Δ ADC based on the controlled sine wave fitting (CSWF) method and Each BIST step needs an accumulator to conduct the specified BIST function[9].

a low cost test method for the static and dynamic characterization of analog-to-digital converters. The method is suitable for implementation in a System on Chip (SoC) environment, as a built-in self test (BIST) solution [20]. In comparison to the traditional dynamic testing methodology, it required high-quality single/multi-tone signals that are difficult to generate to achieve the performance of ADC.

III. NOTEWORTHY CONTRIBUTION IN THE FIELD OF PROPOSED WORK

There are enough research contributions in the proposed area that have been reviewed and summarized in previous section. However, some significant contributions are reported here as noteworthy contribution.

1. Hardware accelerated emulation approach that enabled automated design and verification algorithms for sampled continuous time (CT) analog circuits, based on massive simulations, to become feasible for real time applications. Designed a new hybrid CT/DT SMASH sigma-delta modulator using double-sampling technique was employed in the second-stage which is a DT modulator operating at 200 MHz sampling rate and consuming 17 mW power from a single 1 V supply [3]. A test methodology using behavioral model of the ADC incorporating its key module level non idealties is matched with the response of the ADC under test by solving a nonlinear optimization problem that finds the best non-ideality parameters corresponding to the observed DUT test response. The multi-tone test stimulus is designed in such a way as to maximize the accuracy with which the model non-ideality parameters can be calculated from the observed test response using a genetic test stimulus optimization algorithm. For test response analysis, the digital pulse sequence at the output of the sigma-delta modulator is made externally observable and utilized as a test access point. The applied test method is fast and diagnosis is very accurate where conventional test with high-precision test source is unavailable.

Many work related to simulation and optimization of complex continuous-time (CT) circuits like sigma-delta modulators, which required large computation times when using only transistor-level analog simulators. At that time effective high-level system modelling should be considered in order to reduce the conception effort. More accuracy is expected when using high-level non-linear macro-models and VHDL based simulations [6]. The proposed model not only can be used for evaluating the digital stimulus candidates, but also can be applied to system-level simulations of the mixed-signal design with an embedded sigma-delta modulator [5]. Existing an alternative hybrid solution based on an initial low-cost wafer level screening test followed by a DSP based technique on marginal devices based on alternative DSP transforms. Relatively simple algorithms and cross-correlation techniques are used that can associate specific changes in the bit-stream pattern to key failure modes affecting dynamic performance parameters. A simplified supplementary DSP test for marginal devices is proposed that is less computationally intensive than FFT analysis [20].

The methodology could be used for production as well as for real time built-in self-tests and showed that a pseudorandom signal is a good option for a signal source and that test method leads to efficient and cost-effective testing that can also be used for real time built-in self-tests[12]. an analogue and mixed-signal BIST scheme which is suitable for detecting manufacturing defects in embedded linear macros[19]. The noteworthy contributions and existing literatures in the proposed area have major challenges that need to be addressed. Some of the major limitatons are:

1. Higher area overhead is used in different BIST approaches while performance testing of the modulators.
2. The simulation of CT modulators is more time consuming than that of their discrete-time counterparts due to the analog loop filter used in CT modulators.
3. The shaping capacity of the modulator noise within the signal bandwidth still needs improvement.
4. It is very difficult to design high-precision test source for sigma-delta modulator.
5. Non-ideal effects resulting from practical circuit of the add up in-band noise and distortion.
6. Appropriate selection of CMOS process technology can still help in reducing hardware complexity and power consumption of large bandwidth and high resolution of the modulator.
7. There is scope to reduce the cost of production of chips to allow the concept of BIST and minimize the testing time.

IV. BIST of Sigma-Delta Modulator Analog-to-Digital Converter

![Figure 1: Built-in-Self-Test of Sigma-Delta Modulator Analog-to-Digital Converter](image)

Proposed work will use BIST test for second order resetting sigma-delta modulator ADC and behavior modeling and post simulation of modulators will be done using the BIST approach, especially histogram BIST (HBIST). The method is more effective in terms of area overhead and power consumption. The overall BIST structure for sigma-delta modulator includes following components:

1. **Test pattern Generation**: This component of the BIST structure converts digitized waveforms into analog signals. A semi digital filter converts the digital values, memorized in the reference memory, to discrete analog levels. To generate the test stimulus signal, the stored digitized waveform is periodically applied to the modulator under test.

2. **Mux**: Multiplexer is switched between controlling function during the test mode and functional configuration during normal mode.

3. **Design under Test (DUT)**: DUT is basic testing block which is 2\textsuperscript{nd} order Sigma–Delta CT modulator of ADC. We need to introduce the nonlinearity model parameter of ADC to obtain the dynamic error such as effective number of bits (ENOB), total harmonic distortion (THD), SNR, etc.

4. **BIST controller**: The BIST controller is activated by the included boundary scan test access point (TAP) controller. Its activity is shown by a special output signal “test” and the functional pins enter an inactive state.

5. **Response analyzer**: This is used in evaluating the response of DUT analyzer to analyze the \textit{L}\textsuperscript{th} length window output modulator bit stream and its corresponding data stored in the reference memory in order to determine static and dynamic error.

V. FLOW DIAGRAM

Objectives of the proposed method and its implementation are:

1. To develop higher order accurate behavioral models of $\Delta \Sigma$ modulator non-idealities used as DUT in BIST approach.
2. To develop a low-cost test methodology for the dynamic specifications of high-precision $\Delta \Sigma$ ADCs using an optimized multi-tone signal.
3. To develop an algorithm for estimating the DUT dynamic specifications from the observed DUT response using model parameter estimation.
4. To improve the efficiency of testing high-resolution converters.
5. To reduce the price of production testing.

VI. EXPECTED OUTCOME OF THE PROPOSED WORK

With the implementation of proposed method, behavioral modeling and post simulation of BIST approaches of 2\textsuperscript{nd} order sigma-delta CT modulators. Resolution of modulators will be increased and also bandwidth is expected to increase. Smaller figure of merit, improved area overhead and reduced power consumption will be achieved. Performance analysis will be made in terms of static and dynamic parameters such as INL, differential nonlinearity (DNL) etc. and the work will be compared with existing noteworthy contributions. The proposed research work will be very useful in VLSI industries for their testing applications.

REFERENCES


