# Memristor
## The Fourth Fundamental Circuit Element

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***Abstract***-The need for new non volatile memory come into picture in order to carried out power efficient nano-computing to next higher level. The most dominant contender for next generation memory technology has found recently knowing as "The missing fundamental element", memristor. The many of researcher have shown their interest on the basis of interesting characteristics shown by it. This particular reviews the basic properties of memristor which describes mainly link between charge and flux linkage. This work particularly mentions memristor and its related mathematics which completes missing link between charge and flux linkage. Due to limited memory capacity and device density of integrated circuits, the memristor has potential advantages for the area of integrated circuits. This works deals with design aspects related to memristor memory read and write operation. This works also review LEON CHUA s arguments based on electromagnetic theory. Its VI characteristics are carried out by using PSPICE and MATLAB.

***Keywords***- *Memristor, Non volatile memory, Integrated circuit, Eletromagnetic theory*

## I. INTRODUCTION

Circuit element that store information without power source that represents valuable changes in electronics which allow low power computation and storage. With IC technology scaling, there exists great interest in searching new universal memories which replace today's SRAM, DRAM and non volatile memories such as flash memory [1].

Very recently, such a new device with pinched hysteresis loop found [2], which recognized as the real life realization of missing fourth circuit element, memristor whose existence was theoretically predicted by Leon Chua in 1971[2]. As a result of his work on non linear circuit elements, he made interesting observation. For traditional linear circuit, there are only three independent passive circuit elements: the resistor R, capacitor C and inductor L. The fundamental basic circuit elements, resistance, capacitance and inductance, describe the relations between fundamental electrical quantities: voltage, current, charge and flux [2]. Resistance relates voltage and current (dv=R.di), capacitance relates charge and voltage (dq=C.dv), and inductance relates flux and current (dØ=L.di), respectively. As shown in Fig. 1, Chua argued that there is a missing link between flux and charge (dØ=M.dq), which he called memristance M [3].

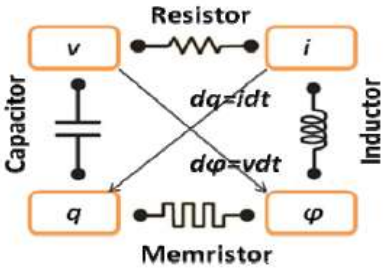



FIG.1: FOUR FUNDAMENTAL CIRCUIT ELEMENTS

If we consider memristor in linear case, it acts like simply resistor. However, if Ø-q relationship is nonlinear, the element is considered as memristance, which can be charge controlled.

$$M(q) = \frac{d\emptyset}{dq} \quad (1)$$

Similarly, q-Ø relationship is flux controlled it referred as memconductance.

$$Gm(\emptyset) = \frac{dq}{d\emptyset} \quad (2)$$

From the recent report, it has been found that if memristor is scaled down to 10nm or below memristor memories can achieve integration density of 100Gbits/cm$^2$, a few times higher than today's advanced flash memory technologies. In addition, the nonvolatile nature of memristor memory makes it an attractive candidate for the next-generation memory technology. As an emerging device, memristor have a very unique set of device characteristics, which have not been fully analyzed, particularly from a design point of view. In this paper, we are going to deal with basic memristor models and equations which are here capture the memristor behavior in a way related to memory operations and complete missing link between flux and charge.

## II. LITERATURE

### *A. Missing Link between flux and charge*

As memristance defined in equation (1) which also can be written as follows,

$$d\emptyset = Mdq \quad (3)$$

By integrating (3) and representing the right hand side as a function of electric charge (q), equation (4) is come into picture. Equation (4) represents the fact that the magnetic flux of the device (φ) is a function of the electric charge that has passed through the device.

$$\emptyset = f_M(q) \quad (4)$$

If equation (4) is differentiated with respect to time, equation (5) is realized.

$$\frac{d\emptyset}{dt} = \frac{df_M(q)}{dq}\frac{dq}{dt} \quad (5)$$

As we know the definition of voltage and current, the equation (5) can be written as follows:

$$v(t) = \frac{df_M(q)}{dq} i(t) \quad (6)$$

In simple way equation (6) can be represented as,

$$v(t) = M(q)i(t) \quad (7)$$

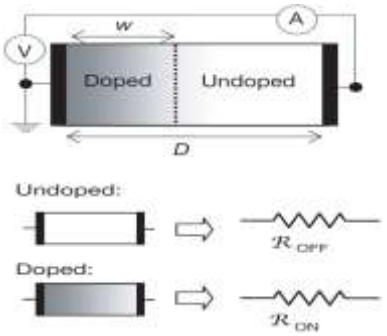
If we consider these devices have a memory of the charge that has passed through it, (7) can be expressed as (8), where, instead of charge, a state variable w represents the current memory state of the device.

$$v(t) = M(w)i(t) \quad (8)$$

Thus we can say that Chua's new circuit element have electrical resistance dependent on amount of charge flows through its terminals. Furthermore, device exhibit memory about its resistance which was in last active state, even though it not in use. Thus, we can say that Chua's new element memristor is combination memory and resistor.

B. *Basic Memristor models*

Fig. 2 shows basic physical structure of memristor and its equivalent circuit model. The device is generally consists of electrically switchable thin semiconductor film placed between two metal contacts. Thin semiconductor film contains doped and undoped region having total length D. The internal state variable w represents length of doped region. Generally doped region provides low resistance path while resistance of that undoped region is much higher. When an external voltage is applied across memristor, length w goes on changing because of the charged dopant drifting [3]. Hence, the device's total resistivity changes.



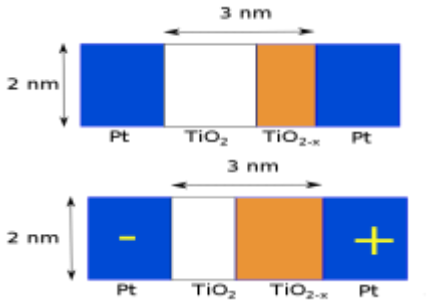




FIG.2: MEMRISTOR DEVICE STRUCTURE AND CIRCUIT MODEL

If the doped region extends to the full length D, that is w/D=1.0, the total resistivity of the device would be dominated by low resistivity region, with a value measured to be $R_{ON}$. Likewise, when the un-doped region extends to the full length D, i.e. w/D=0, the total resistance is denoted as $R_{OFF}$. Thus, the mathematical model for device resistance can be described as

$$R(w) = \left(R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right)\right) \quad (9)$$

From Fig.2, this arrangement simply appears as regular resistor but actually it is compound device made up of two resistors. However, with applied electric field dopant vacancies from doped region shifts towards undoped region which increases effective width of doped region at rate defined by equation

$$w(t) = \mu_V \frac{V_{ON}}{D} \quad (10)$$

Where $\mu_V$ is average ion mobility. Rearranging the equation (10) expressed in terms of current i (t) can be given by equation (11),

$$\frac{dw(t)}{dt} = \mu_V \frac{R_{ON}}{D} i(t) \quad (11)$$

If equation (11) is integrated with respect to time, we get equation (12).

$$w(t) = \mu_V \frac{R_{ON}}{D} q(t) \quad (12)$$

Assuming $R_{ON} << R_{OFF}$ and substituting equation (12) into (9), and comparing with equation (7) we can get equation (13) as follows

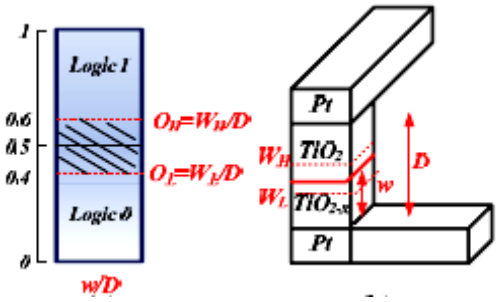
$$M(q) = R_{OFF}\left(1 - \frac{\mu_V R_{ON}}{D^2} q(t)\right) \quad (13)$$

From equation (13), it is clear that memristance effect is mainly charge dependent and magnitude of memristance effect is inversely proportional to square of the manufacturing device size (D). From this we can conclude that memristance effect is more effective at nanometer scale as compared to micrometer scale. This result especially highlights aspects related to given mechanism which are as follows, For given voltage electrical field is inversely proportional to distance over which it is to be applied. Hence in older, larger processes we were not able to

generate such high electric field strength due to this memristance effect is not observable at that time

## III. PROPOSED CIRCUIT DESIGN

In this section we are going to deal with read and write schemes for memristor memories and discuss circuit design issue associated read, write stabilities referred from [4].



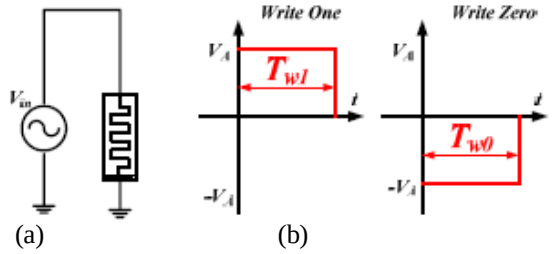

(A) (B)

FIG.3: (A) OUTPUT LEVELS (B) MEMRISTOR 3D NANO STRUCTURE [4]

### A. Output levels

Identical high and low output levels for memristor are w/D =1and w/D = 0.We can define a memristor is at a logic one and logic zero respectively when 0.5 < w/D < 1 and 0 < w/D < 0.5**.** In reality, to account for possible noise injections, a safety margin left for each logic output can be given as: $0 < w/D < O_L$ ($O_L = w_L/D \leq 0.5$) for logic zero, and $O_H \leq w/D \leq 1$ ($O_H = w_H/D > 0.5$) for logic one [4]. The region between $O_L \leq w/D \leq O_H$ is an unsafe that should be avoided for read/write data integrity [4].

### B. Memristor Memory Write Operation




(a) (b)

FIG.4: (A) MEMRISTOR WRITE OPERATION (B) WRITE SIGNAL PATTERNS [4]

To write logical value to memristor cell, a simple way is having as shown in Fig. 4(a). Consider memristor is at its initial stage where w(0)=0. We have to write logic one w(t)=D. consider positive square wave pulse having amplitude $V_A$ and time duration $T_{wl}$ in Fig. 4(b). We can express flux in terms of w (t) as [4],

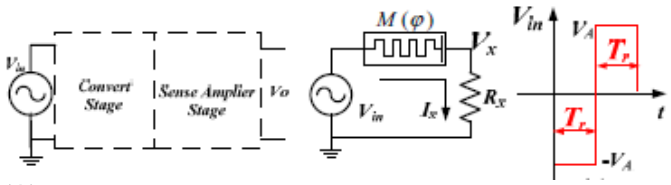
$$\emptyset(t) = \frac{\beta.D^2}{2\mu_V}\left[(1-\frac{w_o}{D})^2 - \left((1-\frac{w(t)}{D})^2\right)\right] \qquad (14)$$

Accordingly, for given $V_A$ time required to reach internal state D can be given as follows [4],

$$T_{wl,wo} \geq \frac{\emptyset_D}{V_A} \text{Where} \emptyset_D = \frac{\beta.D^2}{2\mu_V} \qquad (15)$$

Therefore, a pulse width larger than time Tw1 is able to guarantee the state to reach the ideal one and the pulse width Tw0 to write an ideal logic zero is also the same.

### C. Memristor Memory Read Operation




(A) (B) (C)

FIG.5 (A) READ OPERATION STAGES (B) CONVERT STAGE CIRCUIT (C) READ SIGNAL PATTERN [4]

The read operation is not as simple as that of write operation. In order to read the information of the internal state, we need to apply a voltage, which will read the memristor state successfully. If the mechanism is not well designed, the memristor state might be exceed beyond its safety margin as described in above section (A) related to output levels.

The proposed method for a read operation is in Fig. 5(a). It has two stages: convert stage and sense amplifier stage [4]. First focus on convert stage as shown in Fig. 5(b), let $V_{in}$ be the input voltage and $V_x$ be the voltage at node x. The purpose of adding a series resistor is to convert the memristor state into a voltage signal since the current through the memristor carries the memristor state information. The read pattern is defined in Fig. 4 (c). The output Vx can be described by voltage division [4]

$$v = \frac{R_x}{R_x + M(\emptyset_{in} - \emptyset_x)} \qquad (16)$$

Let the initial memristor state be an ideal logic zero, w (0) =0, which is at off state with resistance M (q) =Roff. The output Vx would be a voltage output of the divider consisting of Rx and Roff for the read operation. Rx needs to be properly designed to distinguish logic zero and one. Rx is set so the output level is half of Vin, when memristor state is at half of its length D. If Memristor state less than D/2 would result Vx below half of Vin. Similarly, output Vx higher than half of Vin represents memristor state is more than D/2. For that, Rx is designed to the following [4]:

$$R_x = \frac{R_{on} + R_{off}}{2} \qquad (17)$$

When memristor initially stores an ideal logic zero, M (q) = $R_{off}$, output $V_x$ is lower than half of Vin. When the memristor stores an ideal logic one, M (q) =Ron, output $V_x$ is greater than half of Vin. In this way, we can distinguish logic zero and logic one.

### D. Read Pulse Width Constraint

Important aspect regarding the read operation must be take into account is that after each read the memristor state can recover to a desired (original) high level but it cannot recover to

a desired (original) low logic level. Suppose memristor stored at $w_0$=0, the negative step pulse would not affect the state, but the positive pulse affects the state. Accordingly, the memristor state is no longer at required low level after a cycle of read. So we have to design the read process so that the read process would not move the state beyond the $O_L$ safety margin. Thus, read pulse width Tr should have a limit.

## IV. SPICE MODELING OF MEM-SYSTEM

The port and state equations for $n^{th}$ order memsystem can be given as follows respectively,

For current controlled mem-system,

$$V=M(q)\ (x, i, t) \quad (18)$$

$$x=f(x, i, t) \quad (19)$$

For voltage controlled mem-system,

$$i=G(\emptyset)\ (x, v, t) \quad (20)$$

$$x=f(x, v, t) \quad (21)$$

These are the starting points of spice modeling. The generel block diagram is as shown in fig.(6).

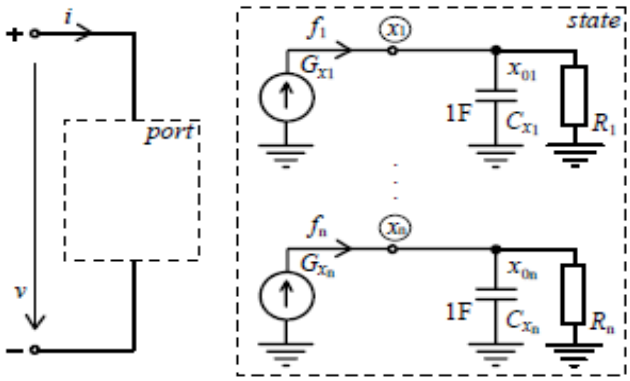
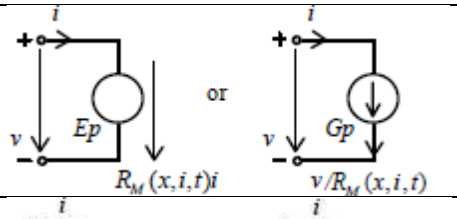
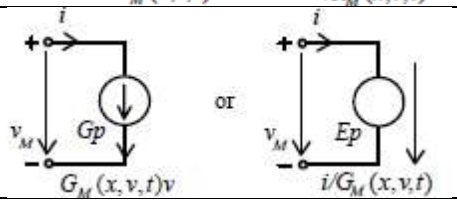



Fig. (6) General Block diagram of Spice model for $n^{th}$ order mem-system [5]

The "Port" block contain model of the system interact with its neighborhood via its terminal voltage and current. Since some of circuit variable contain variable parameter, such as Charge and flux, it is necessary to model them with respect to time integration of current and voltage. The corresponding integrators must be the part of the port as shown in the Fig. 6 and state equations are configured by utilizing n integrators as shown in Fig. 6. The integrators are implemented by using G-type current controlled source driving grounded 1- Farad capacitors [5]. The currents of G-type sources are modified by means of equations which describe the individual component $f_1$, $f_2$, ……, $f_n$ of vector function f of corresponding state equation. The nodal voltages $x_1$, $x_2$,..., $x_n$ represent numerical value of state variable $x_1$, $x_2$,..., $x_n$ [5].

TABLE NO I SPICE MODEL OF "PORT" SYSTEM [5]

| System Type | Spice Model Of "Port" System |
|---|---|
| Current Controlled Memristive System |  |
| Voltage controlled Memristive System |  |



## V. SIMULINK MODEL OF HP MEMRISTOR

While configuring simulink model of HP memristor, the following parameter must be taken into consideration with Fig. 2 as frame of reference.

Ron = 100 Ω, Roff = 16e4 Ω
$\mu_v$ = Dopant mobility = 1e-14 $m^2s^{-1}V^{-1}$
D = Width of thin TiO2 film of HP memristor
w = Length of doped region

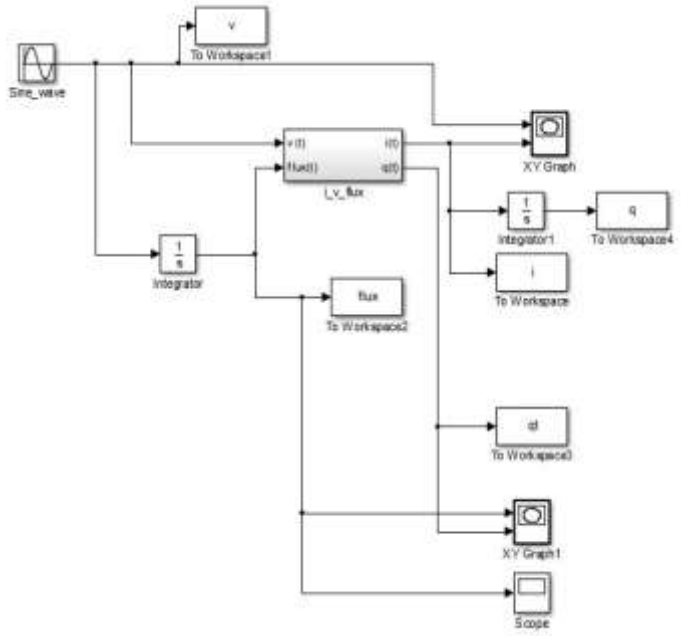
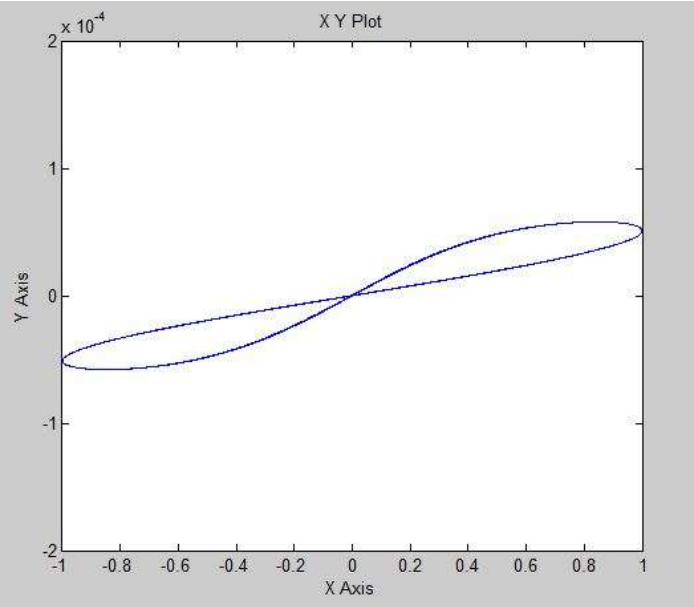



FIG. 7 SIMULINK MODEL OF HP MEMRISTOR

## VI. SIMULATION RESULTS




## VII. CONCLUSION

In this paper, we characterize the fundamental electrical properties of memristor. Derivations provide valuable design aspects and allow depth understanding of key design implications of memristor. In particular, we investigate the design of read and write circuits and analyze data integrity and noise tolerance issues referred from [4]. According to the recent report, density of memristor can go beyond 100Gbits/cm$^2$. Compared to the latest flash memories which typically have a density of 32Gbits/cm2, the memristor-based memories can be much more dense and compact. The switching power consumption for memristor can be 20 times smaller than flash memories. Memristor memories are also non-volatile, so computers can start without reboot. Thus, from this paper, we can provide a basis for understanding the key memristor device characteristics and exploring them for a range of applications. VI characteristics obtained from simulink model gives sense of memristor and by referring these characteristics we can predict memristor behavior in any circuit.

## REFERENCES

[1] Memory Technology for the Post CMOS Era, ITRS IEEE Circuits & Device, March/April 2005.
[2] L. O. Chua, “Memristor - The missing circuit element,” IEEE Trans. Circuit Theory, vol. CT-18, pp. 507 519, Sept. 1971
[3] D. B. Strukov, G. S. Snider, D. R. Stewart, R.S.Williams, “The missing memristor found,” *Nature* 453, 80–83(2008).
[4] Yenpo Ho, Garng M. Huang and Peng Li, “Nonvolatile Memristor Memory: “Device characteristics and Design implications” IEEE Conference on computer aided design digest of Technical papers (2009)
[5] Z. Biolek, D. Biolek, and V. Biolkov´a. SPICE model of memristor with nonlinear dopant drift, Radio engineering J., 18(2):211, 2009b