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Hamming Codes on SRAM Based FPGA for Space Applications

Prof. Mary Joseph, Ancy George
Dept. of ECE)MTech (EC)
MA College of EngineeringMA College of Engineering
Kothamagalam,KeralaKothamagalam, Kerala
maryjosephc@gmail.com, georgeancy21@gmail.com

Abstract--This paper discuss about the method for designing error tolerant systems in SRAM-based FPGAs. SRAM-based FPGAs are preferred in mission based critical space applications. But due to high radiation on the sensitive part of the circuits which introduces errors called Single Event Upset (SEU).Sometimes these types of errors results the permanent malfunction of the entire system. Different error detection techniques were used, of these highly preferred is Triple Modular Redundancy (TMR). Here proposes an error detection and correction method to protect the memories against the soft errors. The method is based on Hamming Codes in which parity bits are inserted on the data to be transmitted. Encoding and decoding of data which increases the security. This technique which provides multi bit error correction together with adjacent error detection. This is a promising technique with faster reconfiguration and high error tolerance.

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I. INTRODUCTION

Field Programmable Gate Arrays (FPGAs) are demanded for variety of applications. FPGAs are especially in spacecraft electronic applications because of its high flexibility in achieving multiple requirements in single platform and fast turnaround time. SRAM-based FPGAs are highly preferred and suited for remote missions because it can bere programmed by the user whenever necessary in avery short span of time. It offers the additional features gives in-orbit design changes, which improves the entire performance of the system and reduces the mission cost. Normally during the data transmission probability for occurring malfunction of the system due to errors are very high. For these different coding techniques were introduced. Code words generated for the data have message bits and check bits; these check bit will be different combination of the message bits to be transmitted.

Errors are mainly classified as Hard and Soft errors. Hard errors which cause the physical damage to the system and these errors are very difficult to correct. But soft errors can be defined as bit flips. By efficient error detection technique we can correct soft errors otherwise it results silent data corruption and finally the system failure. Techniques adopted for detecting errors proposed by scientist Richard W Hamming known as Hamming codes. These coding technique were introduced long years ago and they are still used different fields for error detection and thereby providing security for the data to be transmitted. Soft error can be described as when a radiation particleas a result of scientific experiments like protons, neutrons or alpha particle that it hits changes the logical value which means bit flip resulted. Bit flip which means the entire data got changed. Error Correction Codes (ECCs) for the datathat ranges from simple technique uses Hamming codes to more powerful and complex codes like Bose–Chaudhuri–Hocquenghem (BCH) codes . For any coding techniques if it is simple or complex, the data will be encoded when it is transmitted and decoded when received. So these encoding and decoding methods complexity directly affects the access time of required data. As a result of all these facts we should select simple coding technique to maintain the access time of data. So that they can be applicable for memories and protection for registers in digital circuits.

Different mitigation techniques have been proposed and adopted in order to avoid malfunctions in digital circuits. Creating immunity to errors in circuits is very important to avoid silent data corruption in the system. Dual and Triple module redundancy (TMR) are highly used in mission applications.TMR on which three copies of the same data is kept and depending upon the voting system the data is selected. TMR requires large memory which increases the cost. Configuration scrubbing is another technique on which periodical rewriting of the bits upon detecting errors. This method requires continuous access of external memory on which the original data is kept. So the time required for its working is high. While implementing any methods the access time, accuracy and correctness of data should give primary importance. In the case of space application when any of the radiation particle strikes on the data transmitted not only that individual bit but also the neighboring bits also get affected so it's very important to have an efficient technique to detect errors. In the field of space applications efficient error detection method is required because it's impossible that a replacement once launched. Hamming codes are very simple and the data to be transmitted is encoded such that parity bits in the position of powers of two and data bits on the remaining positions.

TABLE I

1	2	3	4	5	6	7	8
2^0	2^1	-	2^2	-	-	-	2^3
P1	P2	D3	P4	D5	D6	D7	P8

The table above describes about the basic Hamming code for 4bit data with that parity bits. These parity bits will be the XOR operations of data bits.

P1=data [3] ^ data [5] ^ data [7]

P2=data [3] ^ data [6] ^ data [7]

P4=data [3] ^ data [2] ^ data [1]

P8= data [3] ^ data [5] ^ data [6] ^ data [7] ^ P1^ P2 ^ P4

Hamming codes can be described in such a way that if 'n'is the size of the block.'p'is the number of parity bits,'y' the total number of bits in data content then if dmin is the minimum distance of the code. For any positive integer p≥3 then parameters:

$n = 2p - 1$

$y = n - p$

$d_{min} = 3$

The data can be entered in the matrix format and represented in row and column manner .Initial encoding is on that data converted into basic Hamming code format by inserting parity bits only on the powers of two positions.

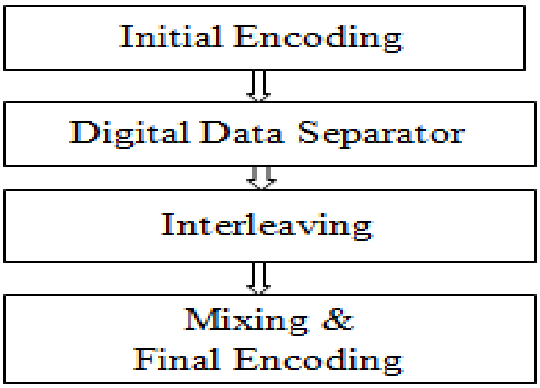

Fig1 Encoding steps

Digital data separator is second step of encoding on that the data and parity bits get separated. Interleaving is the method of data retrieval here has separate data and parity interleave on matrix transpose concept. Mixing is the final encoding step on which additional parity bits generated by XOR operations added to improve the security of data. To maximize the adjacency of bit combinations we reorder the bit by Selective bit placement strategy. Because the detection of adjacent errors are very difficult.

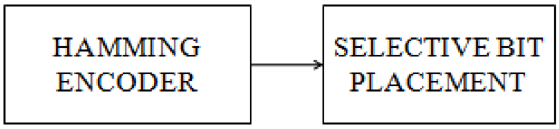

Fig 2 Encoding and Bit Placement

Consider an example for Selective bit placement for Hamming code (12, 8)

TABLEII

SELECTIVE BIT PLACEMENT											
1	2	3	4	5	6	7	8	9	10	11	12
1	12	2	3	6	8	7	9	4	10	5	11

Upon receiving encoded and bit placed data error check process will take place. Parity check matrix that is Lexicographic matix is used.

Lexicographic is the special parity matrix means the column gives the binary representation of value. Lexicographic matrix for Hamming code (12,8) is,

$$HLex = \begin{vmatrix} 000000011111 \\ 000111100001 \\ 011001100110 \\ 101010101010 \end{vmatrix}$$

The column of these matrix that represents binary value upto12. Standard bit placement positions are for different size of data bits. Current value of the code word get multiplied with the matrix and the product value hence generated is termed as Syndrome. If it results null vector which means no error occurred in data,otherwise it gives the binary representation of the position in which error generated. But if resulted syndrome that have higher than the value means adjacent error occured.

II.PROCEDURE:1) Code word selected

2) Adjacent error combinations of these codeword are then generated.

3) Multiplied with Lexicographic check matrix

4) Resulted syndrome higher than the bit position of code selected then find the position.

After these decode the code word into the original data that required.

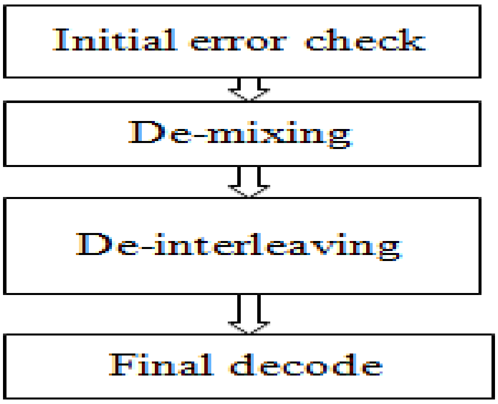

Fig3 Final Decoding

Then finally the information bits are decoded without silent data corruption.So while considering any of these mitigation techniques we should also dealt with the hardware implementation complexity. These hamming code technique on which even if large number of parity bits are generated but it includes on XOR operations. For parity bits we can provide buffer memory but it's less expensive. Similarly in the case of syndrome value generation also only XOR operations are included. These have less number of operations when compared with other methods adopted earlier. It provides faster reconfiguration with fewer spans of time. High system throughput is the other advantage because it's performed without stalling the entire system functionality. This method requires less implementation penalties with the existing FPGA system. Moreover it provides high tolerance. Since we adopting selective bit placement strategy adjacency of the data bits can be maximized. We can verify the functionally by using Hardware descriptive language. We will obtain the Register Transfer level of the entire system. Then apply the required test vectors for verifying the functionality. Hence this is very useful method in memory.

III. CONCLUSION

Here we discuss about Hamming codes in mission based critical space applications. This is simple method with very less number of operations when compared with other techniques adopted. Main advantages are that faster reconfiguration and less hardware implementation penalties. It results multibit error correction and adjacent error detection. So this is promising technique can surely be applied in space applications.

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